

EMIPAK 1B PressFit Power Module 600 V Double PFC MOSFET, 25 A



EMIPAK 1B
(package example)



RoHS
COMPLIANT

FEATURES

- E series Power MOSFET
- MOAT and SiC diode technology
- Exposed Al₂O₃ substrate with low thermal resistance
- Low input capacitance
- Low switching and conduction losses
- Ultra low gate charge Q_g
- Low internal inductances
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?999912

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

PRIMARY CHARACTERISTICS	
Q1 - Q4 MOSFET	
V _{DSS}	600 V
R _{DS(on)} typical at I _C = 25 A	59 mΩ
I _D at T _{SINK} = 37 °C	25 A
Da1 - Da2 DIODE	
V _{RRM}	1200 V
V _{FM} typical at 20 A	1.29 V
I _F at T _{SINK} = 83 °C	20 A
D1 - D4 SILICON CARBIDE CLAMP DIODE	
V _{RRM}	600 V
V _{FM} typical at 10 A	1.72 V
I _F at T _{SINK} = 62 °C	10 A
Package	EMIPAK 1B
Circuit configuration	Double interleaved bridgless PFC (4 x channels) with individual return diodes
Type	Modules - MOSFET

ABSOLUTE MAXIMUM RATINGS (T _J = 25 °C unless otherwise noted)				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T _J		150	°C
Storage temperature range	T _{Stg}		-40 to +150	
RMS isolation voltage	V _{ISOL}	T _J = 25 °C, all terminals shorted, f = 50 Hz, t = 1 s	3500	V
Q1 - Q4 MOSFET				
Drain to source voltage	V _{DSS}		600	V
Gate to source voltage	V _{GS}		± 20	
Pulsed drain current	I _{DM}	V _{GS} = 10 V	85	A
Continuous drain current	I _D	T _{SINK} = 25 °C	26	A
		T _{SINK} = 80 °C	20	
Power dissipation	P _D	T _{SINK} = 25 °C	104	W
		T _{SINK} = 80 °C	58	
Single pulse avalanche energy	E _{AS}	L = 10 mH, I _{AS} = 19 A, T _J = 25 °C	1800	mJ
Pulsed source current (body diode)	I _{SM}		85	A

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.



ABSOLUTE MAXIMUM RATINGS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)				
DA1 - DA2 DIODE				
Cathode to anode voltage	V_{RRM}		1200	V
Single pulse forward current	I_{FSM}		230	A
Diode continuous forward current	I_F	$T_{SINK} = 25\text{ }^\circ\text{C}$	29	A
		$T_{SINK} = 80\text{ }^\circ\text{C}$	21	
Power dissipation	P_D	$T_{SINK} = 25\text{ }^\circ\text{C}$	70	W
		$T_{SINK} = 80\text{ }^\circ\text{C}$	39	
D1 - D4 SILICON CARBIDE CLAMP DIODE				
Cathode to anode voltage	V_{RRM}		600	V
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, $T_J = 25\text{ }^\circ\text{C}$	80	A
Diode continuous forward current	I_F	$T_{SINK} = 25\text{ }^\circ\text{C}$	12	A
		$T_{SINK} = 80\text{ }^\circ\text{C}$	9	
Power dissipation	P_D	$T_{SINK} = 25\text{ }^\circ\text{C}$	38	W
		$T_{SINK} = 80\text{ }^\circ\text{C}$	21	

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Q1 - Q4 MOSFET						
Drain to source breakdown voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 500\text{ }\mu\text{A}$	600	-	-	m Ω
Drain to source on resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$	-	59	71	
		$V_{GS} = 10\text{ V}, I_D = 25\text{ A}, T_J = 150\text{ }^\circ\text{C}$	-	140	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.8	2.6	4.4	V
Temperature coefficient of threshold voltage	$\Delta V_{GS(th)}/\Delta T_J$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ (25 $^\circ\text{C}$ to 125 $^\circ\text{C}$)	-	-9.7	-	mV/ $^\circ\text{C}$
Forward transconductance	g_{fs}	$V_{DS} = 20\text{ V}, I_D = 25\text{ A}$	-	29	-	S
Transfer characteristics	V_{GS}	$V_{DS} = 20\text{ V}, I_D = 25\text{ A}$	-	5.1	-	V
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$	-	0.3	5	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	19	-	
Gate to source leakage current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 150	nA
Q1 - Q4 BODY DIODE						
Source-to-drain voltage drop	V_{SD}	$I_{SD} = 25\text{ A}, V_{GS} = 0\text{ V}$	-	0.9	1.32	V
Da1 - Da2 DIODE						
Forward voltage drop	V_{FM}	$I_F = 20\text{ A}$	-	1.29	1.90	V
		$I_F = 20\text{ A}, T_J = 150\text{ }^\circ\text{C}$	-	1.26	-	
Breakdown voltage	V_{BR}	$I_R = 500\text{ }\mu\text{A}$	1200	-	-	V
Reverse leakage current	I_{RM}	$V_R = 1200\text{ V}$	-	1.0	100	μA
		$V_R = 1200\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	900	-	
D1 - D4 SILICON CARBIDE CLAMP DIODE						
Forward voltage drop	V_{FM}	$I_F = 10\text{ A}$	-	1.72	1.98	V
		$I_F = 10\text{ A}, T_J = 150\text{ }^\circ\text{C}$	-	2.21	-	
Breakdown voltage	V_{BR}	$I_R = 500\text{ }\mu\text{A}$	600	-	-	V
Reverse leakage current	I_{RM}	$V_R = 600\text{ V}$	-	0.2	100	μA
		$V_R = 600\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	1.4	-	



SWITCHING CHARACTERISTICS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Q1 - Q4 MOSFET WITH D1 - D4 CLAMP DIODE						
Total gate charge (turn-on)	Q _g	I _D = 24 A V _{DS} = 480 V V _{GS} = 10 V	-	147	-	nC
Gate to source charge (turn-on)	Q _{gs}		-	36	-	
Gate to drain charge (turn-on)	Q _{gd}		-	60	-	
Turn-on delay time	t _{d(on)}	I _D = 25 A V _{DD} = 300 V V _{GS} = 10 V R _g = 4.7 Ω, L = 500 μH	-	82	-	ns
Rise time	t _r		-	23	-	
Turn-off delay time	t _{d(off)}		-	109	-	
Fall time	t _f		-	9	-	
Turn-on delay time	t _{d(on)}	I _D = 25 A V _{DD} = 300 V V _{GS} = 10 V R _g = 4.7 Ω, L = 500 μH, T _J = 125 °C	-	83	-	ns
Rise time	t _r		-	26	-	
Turn-off delay time	t _{d(off)}		-	111	-	
Fall time	t _f		-	22	-	
Input capacitance	C _{iss}	V _{GS} = 0 V V _{DS} = 100 V f = 1 MHz	-	4810	-	pF
Output capacitance	C _{oss}		-	230	-	
Reverse transfer capacitance	C _{rss}		-	5	-	
Reverse bias safe operating area	RBSOA	T _J = 150 °C, I _D = 50 A, V _{DD} = 400 V, V _P = 600 V, R _g = 4.7 Ω, V _{GS} = +10 / 0 V				
Q1 - Q4 BODY DIODE						
Diode reverse recovery time	t _{rr}	V _R = 30 V, T _J = 25 °C I _S = 30 A di/dt = 100 A/μs	-	500	-	ns
Diode reverse recovery current	I _{rr}		-	41	-	A
Diode reverse recovery charge	Q _{rr}		-	10.5	-	μC
D1 - D4 SILICON CARBIDE CLAMP DIODE						
Total capacitive charge	Q _C	V _R = 600 V I _F = 10 A di/dt = 500 A/μs	-	30	-	nC

INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Resistance	R ₂₅	T _C = 25 °C	5000	Ω
	R ₁₀₀	T _C = 100 °C	493 ± 5 %	
B-value	B _{25/50}	R ₂ = R ₂₅ exp. [B _{25/50} (1/T ₂ - 1/(298.15K))]	3375 ± 5 %	K
Maximum operating temperature			220	°C
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Q1 - Q4 MOSFET - Junction to sink thermal resistance (per switch) ⁽¹⁾	R _{thJS}	-	1.00	-	°C/W
Da1 - Da2 DIODE - Junction to sink thermal resistance (per diode) ⁽¹⁾		-	1.48	-	
D1 - D4 SILICON CARBIDE DIODE - Junction to sink thermal resistance (per diode) ⁽¹⁾		-	2.76	-	
Case to sink thermal resistance (per module) ⁽¹⁾		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	28	-	g

Note

⁽¹⁾ Mounting surface flat, smooth, and greased, λ_{grease} = 0.67 W/mK

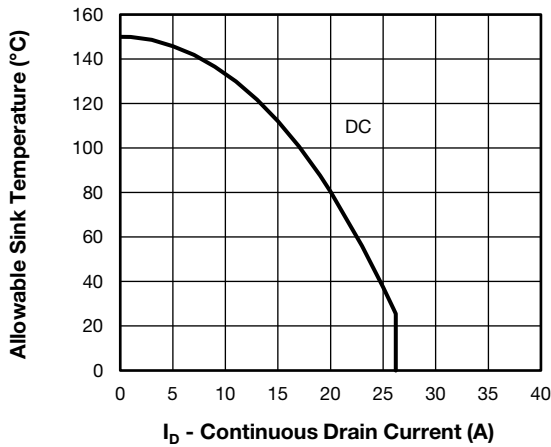


Fig. 1 - Maximum Continuous Drain Current vs. Sink Temperature

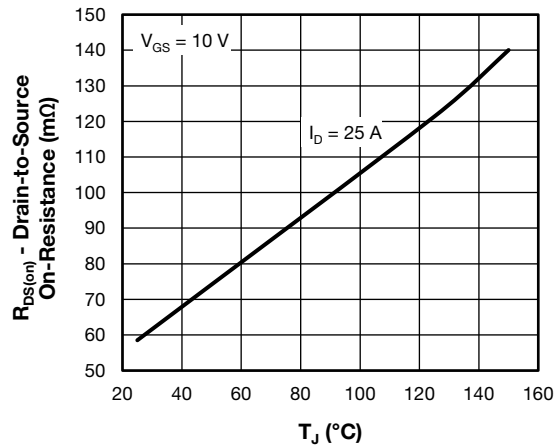


Fig. 4 - Typical Drain-to-Source On-Resistance vs. Temperature

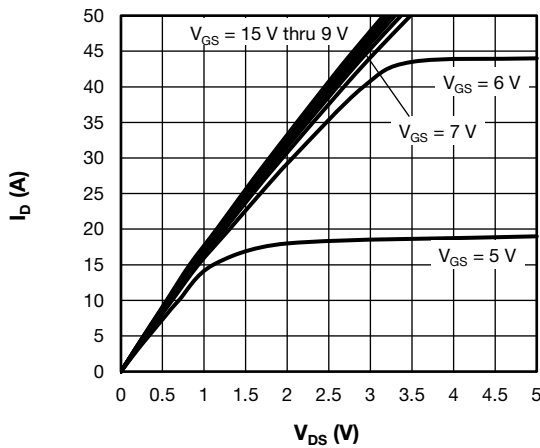


Fig. 2 - Typical Drain to Source Current Output Characteristics at $T_J = 25\text{ }^\circ\text{C}$

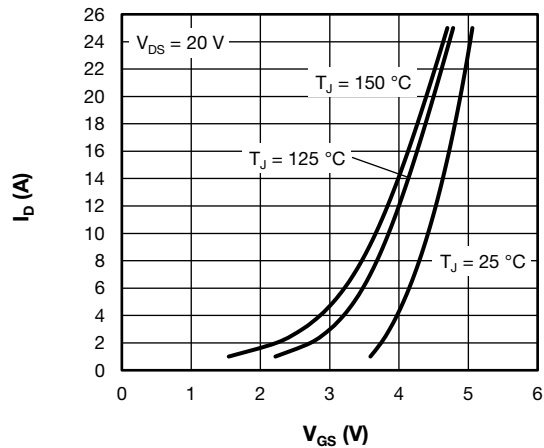


Fig. 5 - Typical Transfer Characteristics

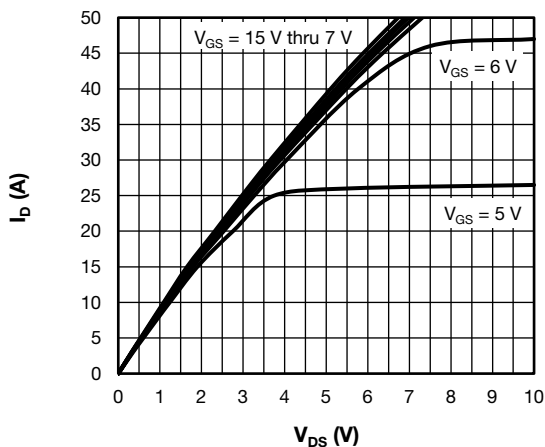


Fig. 3 - Typical Drain to Source Current Output Characteristics at $T_J = 125\text{ }^\circ\text{C}$

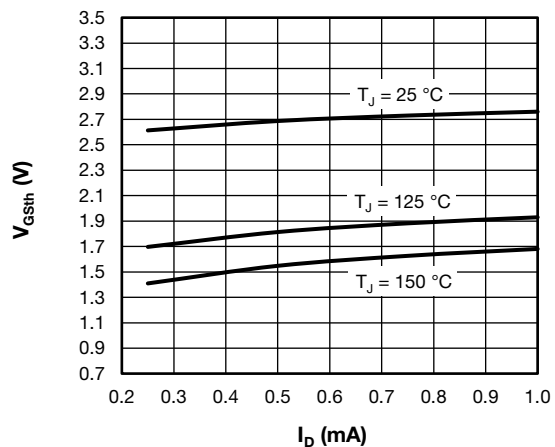


Fig. 6 - Typical Gate Threshold Voltage Characteristics

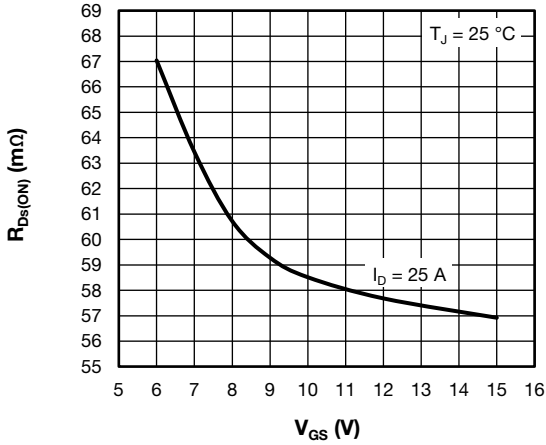


Fig. 7 - Typical Drain-State Resistance vs. Gate-to-Source Voltage

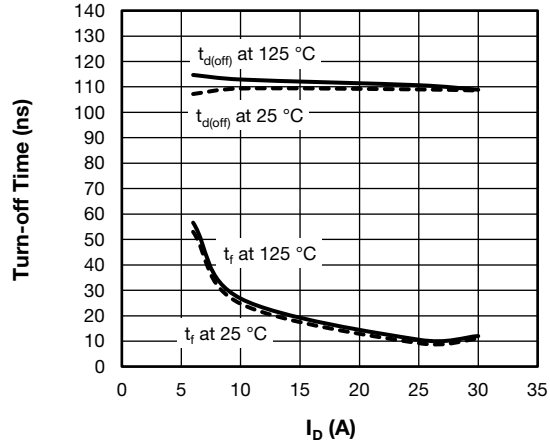


Fig. 10 - Typical Turn-off Switching Time vs. I_D
 $V_{DD} = 300\text{ V}$, $R_g = 4.7\Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

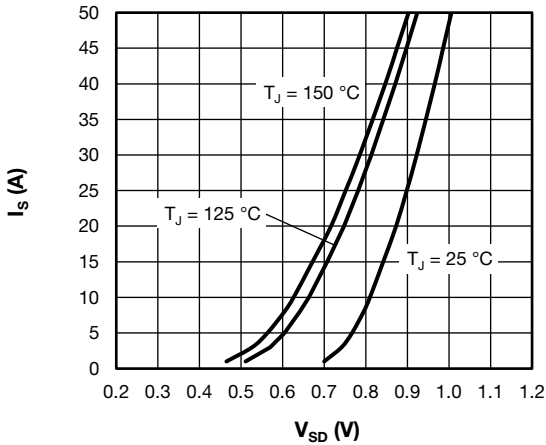


Fig. 8 - Typical Body Diode Source-to-Drain Current Characteristics

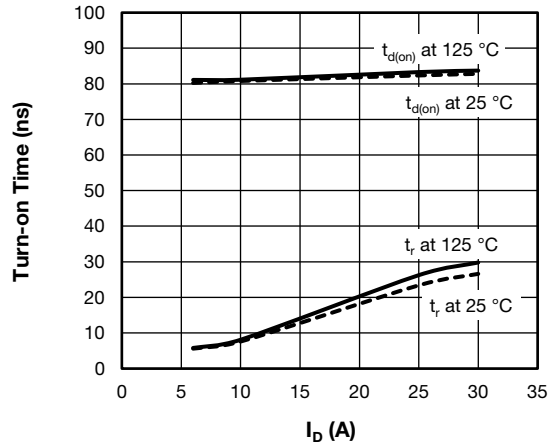


Fig. 11 - Typical Turn-on Switching Time vs. I_D
 $V_{DD} = 300\text{ V}$, $R_g = 4.7\Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

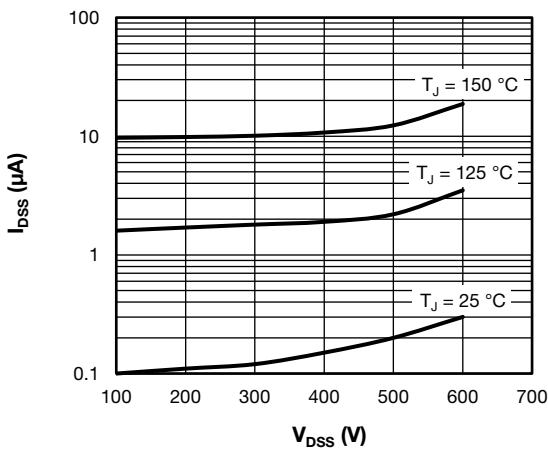


Fig. 9 - Typical Zero Gate Voltage Drain Current

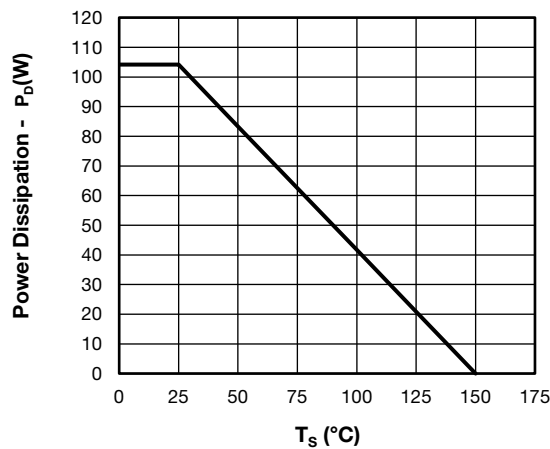


Fig. 12 - Power Dissipation Curve

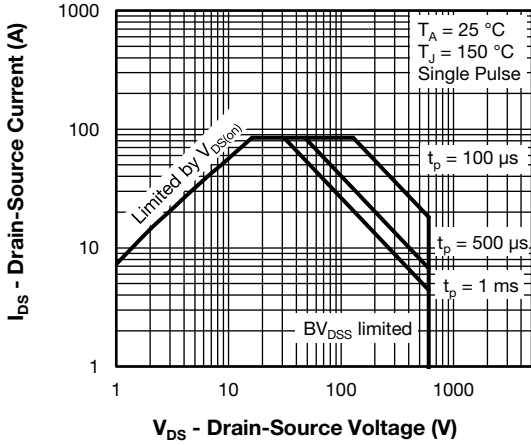


Fig. 13 - Safe Operating Area

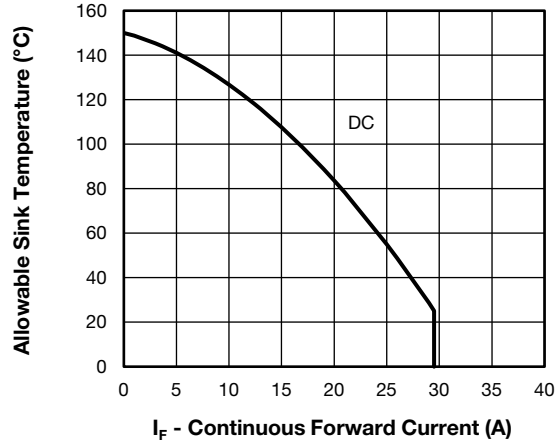


Fig. 16 - Maximum Da1-Da2 Diode Continuous Forward Current vs. Sink Temperature

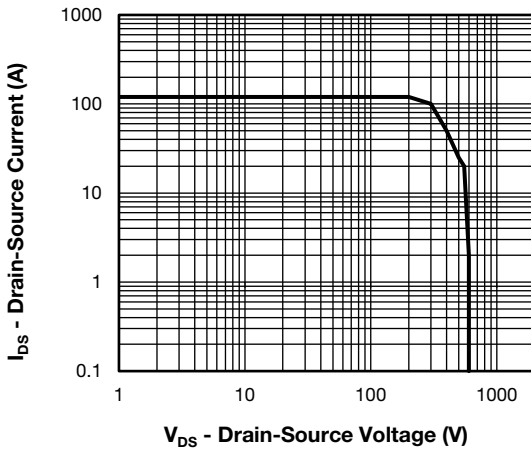


Fig. 14 - Reverse BIAS SOA

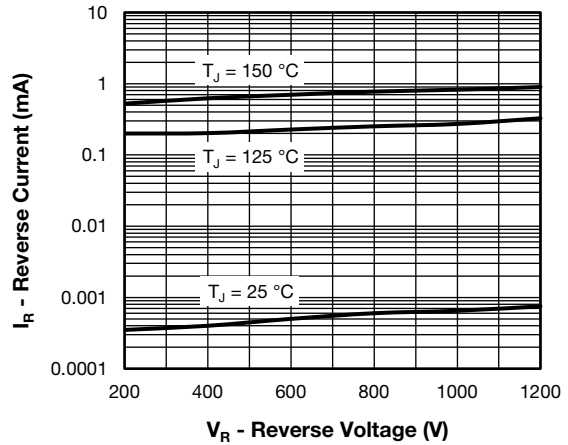


Fig. 17 - Typical Da1-Da2 Diode Reverse Leakage Current

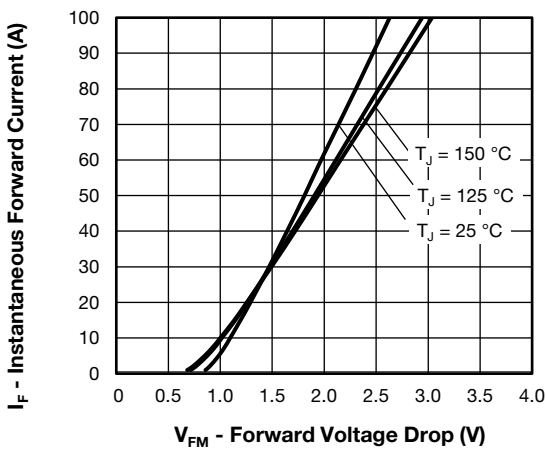


Fig. 15 - Typical Da1-Da2 Diode Forward Characteristics

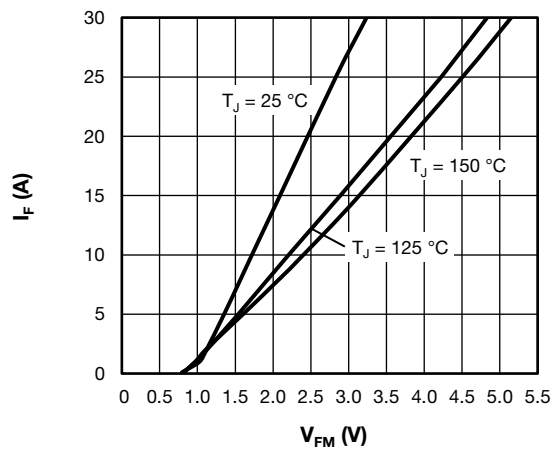


Fig. 18 - Typical D1-D4 Clamp Diode Forward Characteristics

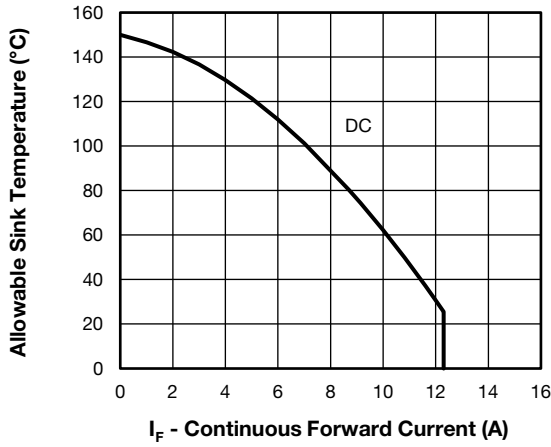


Fig. 19 - Maximum D1-D4 Clamp Diode Continuous Forward Current vs. Sink Temperature

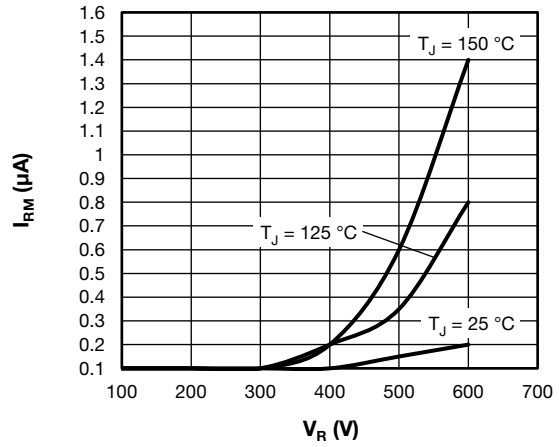


Fig. 20 - Typical D1-D4 Clamp Diode Reverse Leakage Current

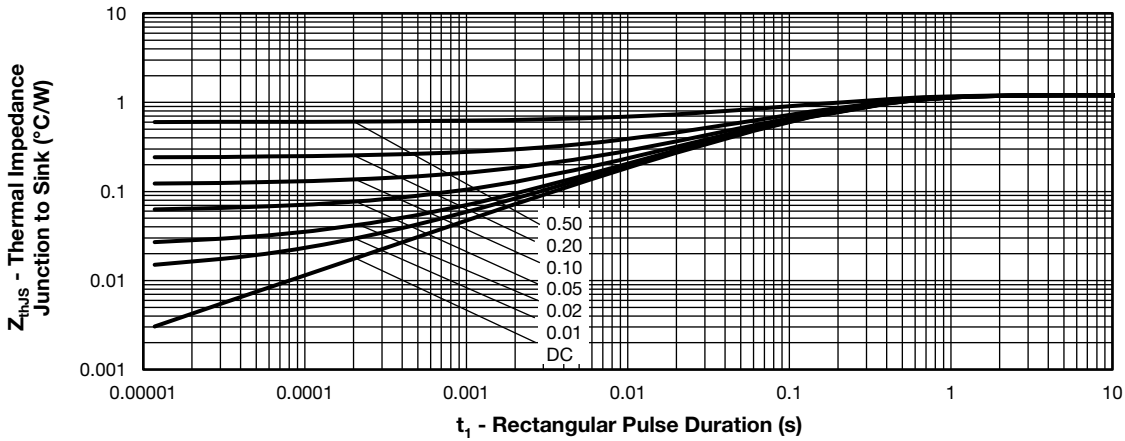


Fig. 21 - Maximum Thermal Impedance Z_{thJS} Characteristics - (Q1-Q4 MOSFET)

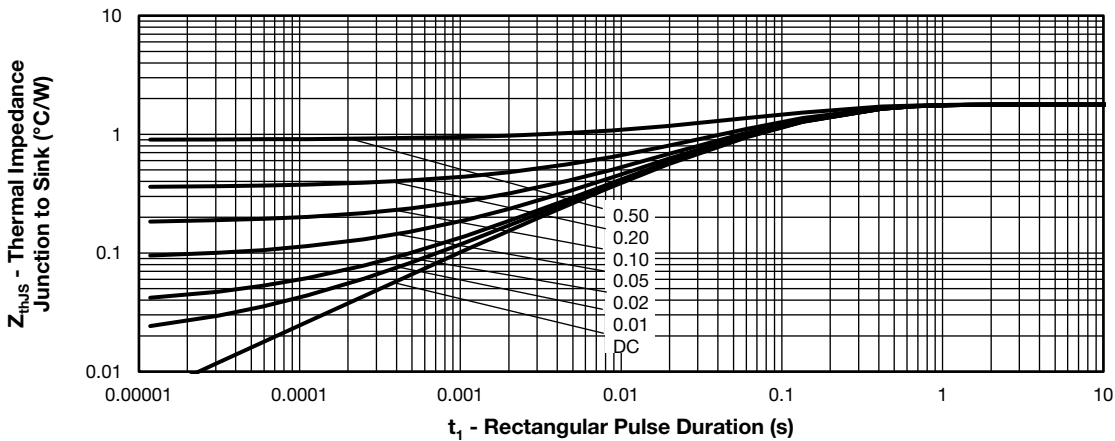


Fig. 22 - Maximum Thermal Impedance Z_{thJS} Characteristics - (Da1-Da2 Diode)

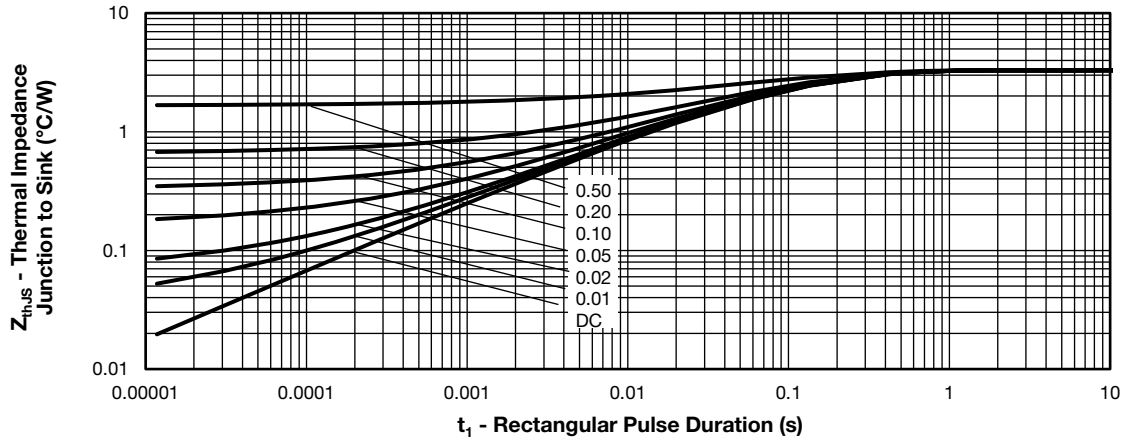


Fig. 23 - Maximum Thermal Impedance Z_{thJS} Characteristics - (D1-D4 Clamp Diode)

ORDERING INFORMATION TABLE

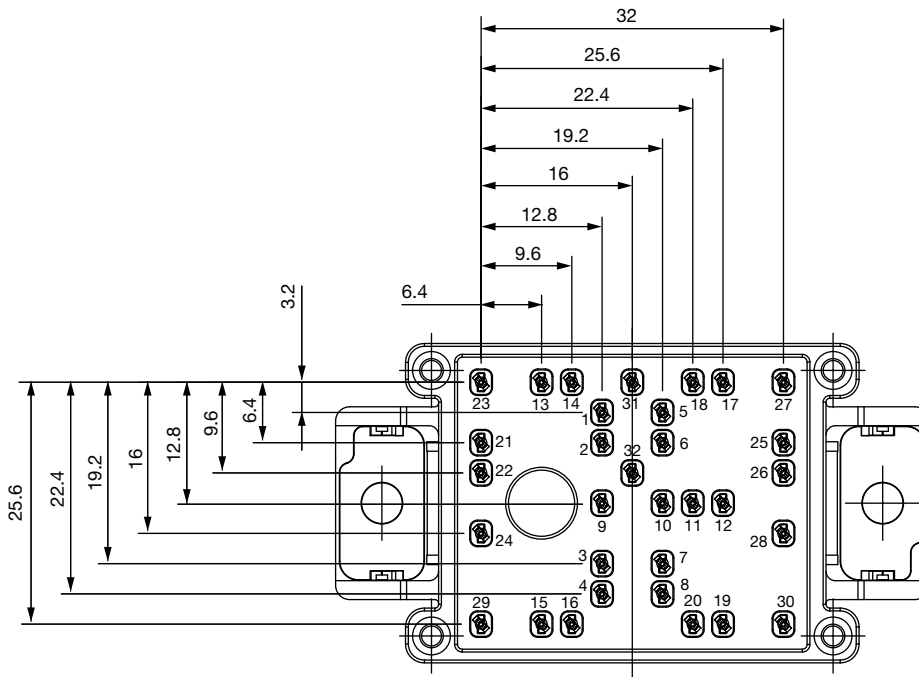
Device code	VS-	EN	Z	025	C	60	N
	①	②	③	④	⑤	⑥	⑦

- 1** - Vishay Semiconductors product
- 2** - Package indicator (EN = EMIPAK 1B)
- 3** - Circuit configuration (Z = Double interleaved bridgless PFC (4 x channels) with individual return diodes)
- 4** - Current rating (025 = 25 A)
- 5** - Switch die technology (C = PowerMOS)
- 6** - Voltage rating (60 = 600 V)
- 7** - Diode die technology



CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Double interleaved bridgless PFC (4 x channels) with individual return diodes	Z	

PACKAGE



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95558
Application Note	www.vishay.com/doc?95580



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