V385A

8-Bit LVDS Transmitter for Video

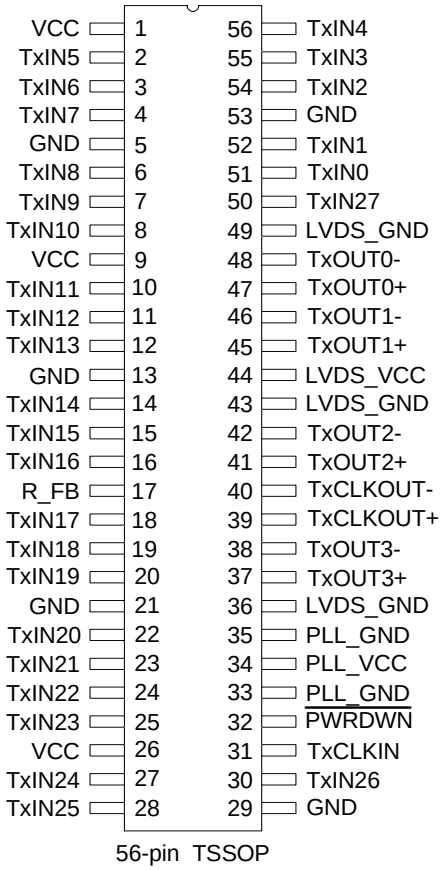
General Description

The V385A transmitter converts 28 bits of 3.3 V CMOS/TTL into 4 Low Voltage Differential Signaling (LVDS) data streams while the transmit clock input is transmitted in parallel with the data streams over a fifth LVDS link.

Compared to the V385, the V385A provides an extended clock frequency range of 12-90 MHz, rather than 20-85 MHz. Other performance improvements have been incorporated as well.

The V385A can be programmed for rising edge or falling edge clocks through pin R_FB.

Pin Assignment

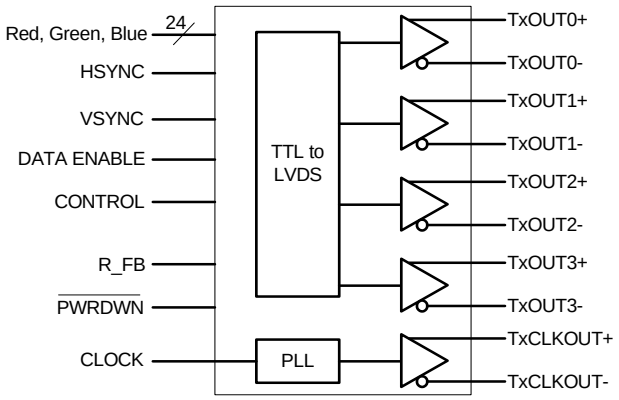


56-pin TSSOP

Features

- Extended clock frequency range of 12 to 90 MHz
- Convert 28 bits of 3.3 V CMOS/TTL into 4 LVDS streams
- Up to 2.52 Gbps throughput or 315 Megabytes/sec bandwidth
- Spread spectrum compatible
- Supports SD, HD and VGA graphics applications
- LVDS voltage swing of 350 mV for low EMI
- On-chip PLL requires no external components
- Single 3.3 V low-power CMOS design
- Operating temperature of -10 to +70°C
- Programmable rising or falling edge strobe
- Power-down control function
- Compatible with TIA/EIA-644 LVDS standards
- Packaged in a 56-pin TSSOP (Pb free available)
- Pin and function compatible with the National DS90C385, TI SN65LVDS93 and THine THC63LVDM83, but with extended clock frequency and operating temperature range

Block Diagram



Pin Descriptions

Pin	Pin Type	Pin Name	Pin Description/Name
1	Power	VCC	3.3V Power
2	CMOS/TTL	TxIN5	Parallel digital video input pins (TxIN0..27).
3	CMOS/TTL	TxIn6	Parallel digital video input pins (TxIN0..27).
4	CMOS/TTL	TxIn7	Parallel digital video input pins (TxIN0..27).
5	Ground	GND	Ground
6	CMOS/TTL	TxIN8	Parallel digital video input pins (TxIN0..27).
7	CMOS/TTL	TxIN9	Parallel digital video input pins (TxIN0..27).
8	CMOS/TTL	TxIN10	Parallel digital video input pins (TxIN0..27).
9	Power	VCC	3.3V Power
10	CMOS/TTL	TxIN11	Parallel digital video input pins (TxIN0..27).
11	CMOS/TTL	TxIN12	Parallel digital video input pins (TxIN0..27).
12	CMOS/TTL	TxIN13	Parallel digital video input pins (TxIN0..27).
13	Ground	GND	Ground
14	CMOS/TTL	TxIN14	Parallel digital video input pins (TxIN0..27).
15	CMOS/TTL	TxIN15	Parallel digital video input pins (TxIN0..27).
16	CMOS/TTL	TxIN16	Parallel digital video input pins (TxIN0..27).
17	CMOS/TTL	R_FB	Programmable strobe select input pin (R_FB). High = rising edge; Low = falling edge.
18	CMOS/TTL	TxIN17	Parallel digital video input pins (TxIN0..27).
19	CMOS/TTL	TxIN18	Parallel digital video input pins (TxIN0..27).
20	CMOS/TTL	TxIN19	Parallel digital video input pins (TxIN0..27).
21	Ground	GND	Ground
22	CMOS/TTL	TxIN20	Parallel digital video input pins (TxIN0..27).
23	CMOS/TTL	TxIN21	Parallel digital video input pins (TxIN0..27).
24	CMOS/TTL	TxIN22	Parallel digital video input pins (TxIN0..27).
25	CMOS/TTL	TxIN23	Parallel digital video input pins (TxIN0..27).
26	Power	VCC	3.3V Power
27	CMOS/TTL	TxIN24	Parallel digital video input pins (TxIN0..27).
28	CMOS/TTL	TxIN25	Parallel digital video input pins (TxIN0..27).
29	Ground	GND	Ground
30	CMOS/TTL	TxIN26	Parallel digital video input pins (TxIN0..27).
31	CMOS/TTL	TxCLKIN	Clock input (TxCLKIN)
32	CMOS/TTL	$\overline{\text{PWRDWN}}$	Active low. Powerdown tri-states outputs.
33	Ground	PLL_GND	Ground
34	Power	PLL_VCC	3.3V Power
35	Ground	PLL_GND	Ground
36	Ground	LVDS_GND	Ground

Pin	Pin Type	Pin Name	Pin Description/Name
37	LVDS	TxOUT3+	LVDS output (+)
38	LVDS	TxOUT3-	LVDS output (-)
39	LVDS	TxCLKOUT+	LVDS output (+)
40	LVDS	TxCLKOUT-	LVDS output (-)
41	LVDS	TxOUT2+	LVDS output (+)
42	LVDS	TxOUT2-	LVDS output (-)
43	Ground	LVDS_GND	Ground
44	Power	LVDS_VCC	3.3V Power
45	LVDS	TxOUT1+	LVDS output (+)
46	LVDS	TxOUT1-	LVDS output (-)
47	LVDS	TxOUT0+	LVDS output (+)
48	LVDS	TxOUT0-	LVDS output (-)
49	Ground	LVDS_GND	Ground
50	CMOS/TTL	TxIN27	Parallel digital video input pins (TxIN0..27).
51	CMOS/TTL	TxIn0	Parallel digital video input pins (TxIN0..27).
52	CMOS/TTL	TxIn1	Parallel digital video input pins (TxIN0..27).
53	Ground	GND	Ground
54	CMOS/TTL	TxIn2	Parallel digital video input pins (TxIN0..27).
55	CMOS/TTL	TxIn3	Parallel digital video input pins (TxIN0..27).
56	CMOS/TTL	TxIn4	Parallel digital video input pins (TxIN0..27).

External Components

The V385A requires no external components.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the V385A. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.3 V to +4 V
All Inputs and Outputs	-0.3 V to VCC+0.3 V
Electrostatic Discharge (EIAJ, 0Ω, 200 pF)	> 500 V
Ambient Operating Temperature	-10 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Maximum Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-10		+70	°C
Power Supply Voltage (measured in respect to GND)	3.0	3.3	3.6	V

Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature -10 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Freq.
CMOS/TTL DC Specifications							
Input High Voltage	V_{IH}		2.00		VCC	V	
Input Low Voltage	V_{IL}		GND		0.80	V	
Input Current	I_{IN}	GND<VIN<VCC			±10	µA	
Power-down Current	I_{PD}	No switching for input pins			10	µA	
LVDS DC Specifications							
Differential Output Voltage	V_{OD}	R_L = 100 ohms	250	345	450	mV	
Change in V_{OD} Between Complimentary Output States	ΔV_{OD}				35	mV	
Common Mode Voltage	V_{CM}		1.125	1.250	1.375	V	
Change in V_{CM} Between Complimentary Output States	ΔV_{CM}				35	mV	
Output Short Circuit Current	I_{OS}	V_{OD}=0V		3.5	5	mA	
Output Tri-State Current	I_{OZ}	Power Down#=0V		±1	±10	µA	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Freq.
Recommended Transmitter Input Characteristics							
TxCLK IN Transition Time	TCIT				5	ns	
TxCLK IN Period	TCIP		11.11	T	83.333	ns	
TxCLK IN High Time	TCIH		0.35T	0.5T	0.65T	ns	
TxCLK IN Low Time	TCIL		0.35T	0.5T	0.65T	ns	
TxIN Transition Time	TXIT		1.5		6	ns	
Transmitter Switching Characteristics							
LVDS Low-to-High Time	LLHT			0.75	1.4	ns	
LVDS High-to-Low Time	LHLT			0.75	1.4	ns	
Transmitter Output Pulse Position	TPPos0	Bit0	-0.2	0	0.2	ns	85 MHz
	TPPos1	Bit1	T/7-0.2	T/7	T/7+0.2	ns	85 MHz
	TPPos2	Bit2	2T/7-0.2	2T/7	2T/7+0.2	ns	85 MHz
	TPPos3	Bit3	3T/7-0.2	3T/7	3T/7+0.2	ns	85 MHz
	TPPos4	Bit4	4T/7-0.2	4T/7	4T/7+0.2	ns	85 MHz
	TPPos5	Bit5	5T/7-0.2	5T/7	5T/7+0.2	ns	85 MHz
	TPPos6	Bit6	6T/7-0.2	6T/7	6T/7+0.2	ns	85 MHz
Transmitter Phase Loop Set	TPLLS				10	ms	
TxIN Setup to TxCLK IN	TSTC		2.5			ns	
TxIN Hold to TxCLK IN	THTC		0.5			ns	
TxCLK IN to TxCLK OUT Delay	TCCD		10		30	ns	

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		84		°C/W
	θ_{JA}	1 m/s air flow		76		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			50		°C/W

AC Timing Diagrams

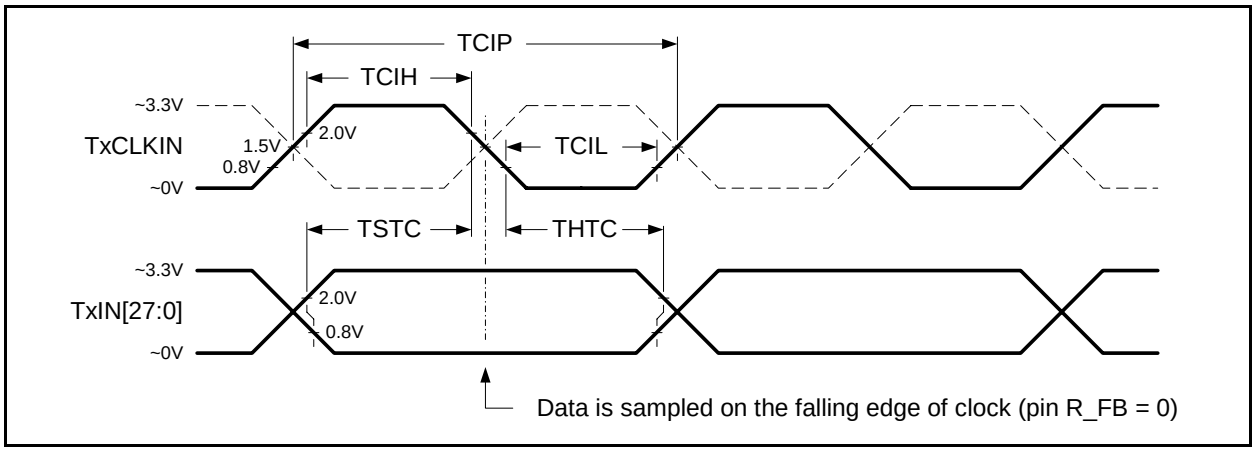


Figure AC1. Transmitter Setup/Hold and High/Low Times (Falling Edge Strobe or R_FB=0)

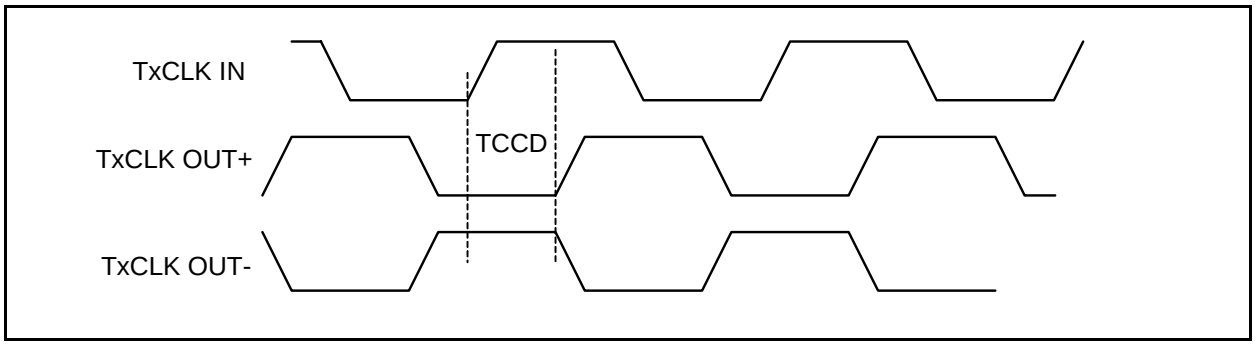


Figure AC2. Clock IN to Clock OUT Delay (Rising Edge Strobe or R_FB=1)

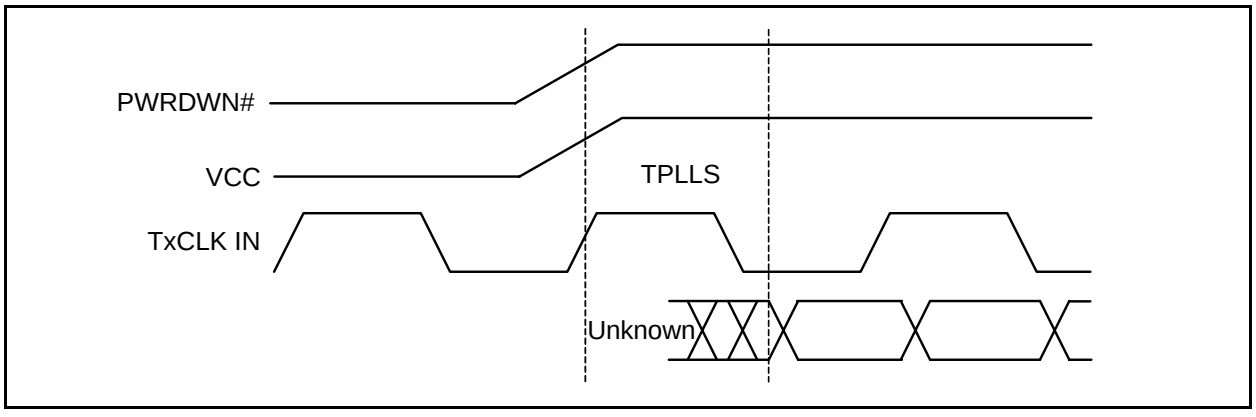


Figure AC3. Phase Lock Loop Set Time

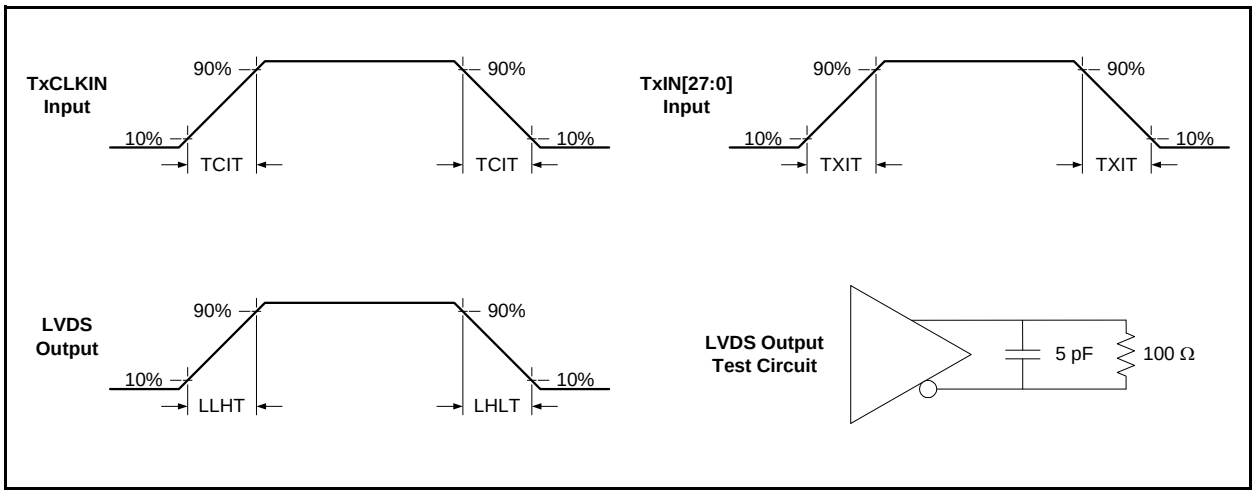


Figure AC4. Transmitter Device Transition Times and Load

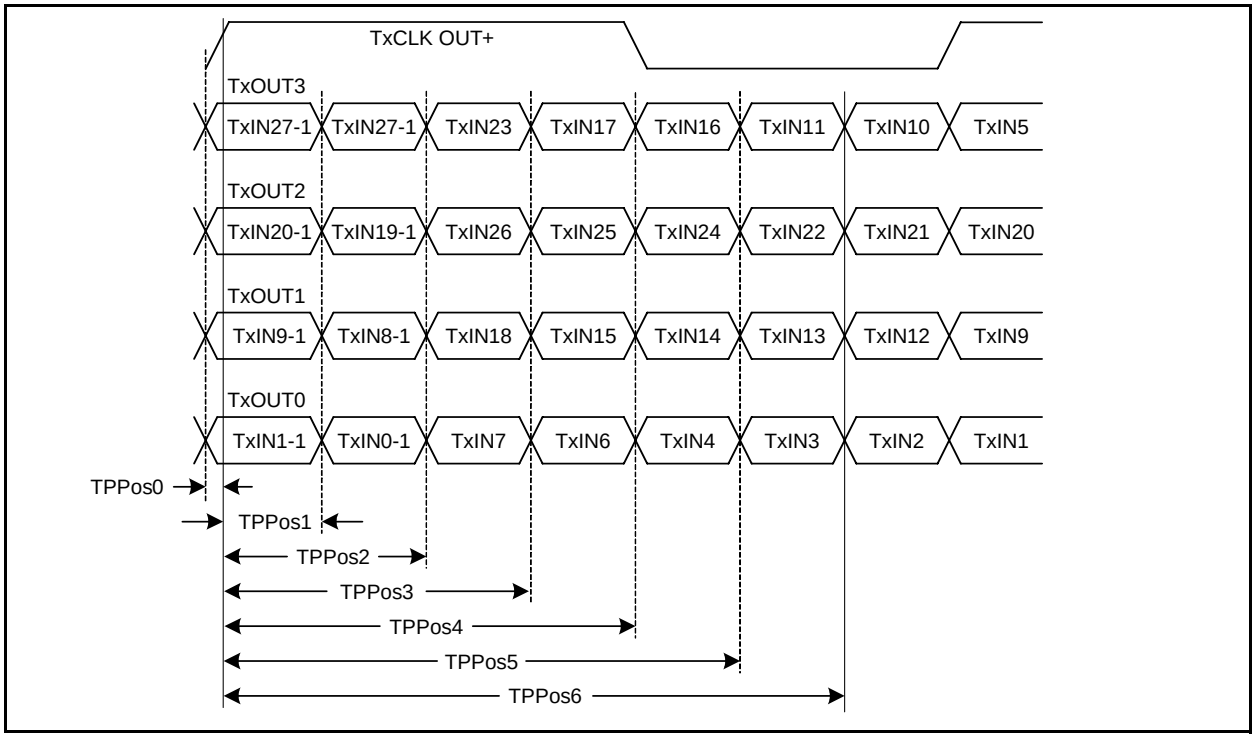
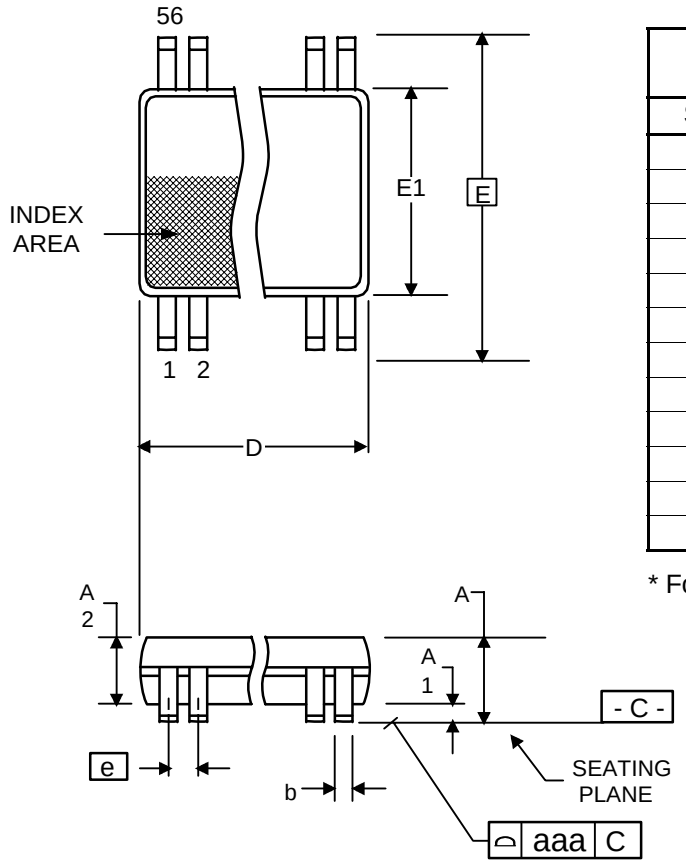


Figure AC5. Transmitter LVDS Output Pulse Position Measurement

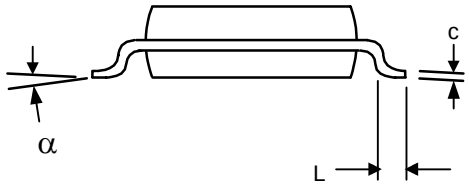
Package Outline and Package Dimensions (56-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.17	0.27	0.007	0.011
C	0.09	0.20	0.0035	0.008
D	13.90	14.10	0.547	0.555
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	0.236	0.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	0.018	0.030
a	0°	8°	0°	8°
aaa	—	0.10	—	0.004

* For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature	Notes
V385AGLF	V385AGLF	Tubes	56-pin TSSOP	-10 to +70° C	
V385AGLFT	V385AGLF	Tape and Reel	56-pin TSSOP	-10 to +70° C	

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.