

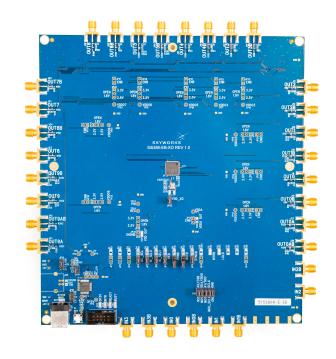
# UG513: Si5386A-E Evaluation Board User's Guide

The Si5386A-E-EB is used for evaluating the Ultra Low Jitter, Any-Frequency, 12-output JESD204B Clock Generator. The Si5386 employs fourth-generation DSPLL technology to enable clock generation for LTE/ JESD204B applications which require the highest level of jitter performance. The Si5386A-E-EB has four independent input clocks and a total of 12 outputs. The Si5386A-E-EB can be easily controlled and configured using Skyworks' Clock Builder Pro<sup>®</sup> (CBPro) software tool.

The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "Si5386A-E-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

#### EVB FEATURES

- Powered from USB port or external power supply
- Onboard 54 MHz XO provides holdover mode of operation on the Si5386
- CBPro GUI programmable VDDO supplies allow each of the ten primary outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5386
- SMA connectors for input clocks and output clocks



## 1. Si5386 Functional Block Diagram

Below is a functional block diagram of the Si5386A-E-EB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults or 6.1 Installing ClockBuilder Pro Desktop Software for more information.

**Note:** All Si5386 schematics, BOMs, User's Guides, and software can be found online at the following link: https://www.skywork-sinc.com/search?q=si538%20evaluation

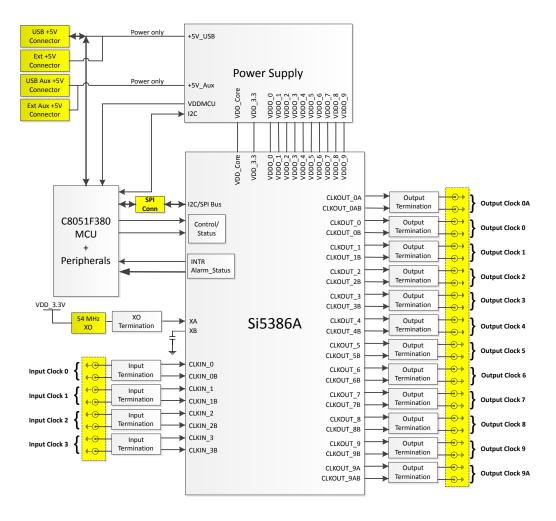


Figure 1.1. Functional Block Diagram of Si5386A-E-EB

UG513: Si5386A-E Evaluation Board User's Guide • Quick Start and Jumper Defaults

## 2. Quick Start and Jumper Defaults

Perform the following steps to quick-start the ClockBuilder<sup>®</sup> Pro software.

- 1. Download and install the ClockBuilder Pro desktop software.
- 2. Connect a USB cable from the Si5386A-E-EB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in the table below.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and verify a frequency plan on the Si5386A-E-EB.
- 6. Download the Si5386 data sheet for more information.

The following table lists the Si5386A-E- EVB jumper defaults.

Location	Туре	l = Installed O= Open	Location	Туре	l = Installed O= Open
JP1	2 pin	0	JP23	2 pin	0
JP2	2 pin	0	JP24	3 pin	all open
JP3	2 pin	0	JP25	2 pin	0
JP4	2 pin	I	JP26	3 pin	all open
JP5	2 pin	I	JP27	2 pin	0
JP6	2 pin	I	JP28	3 pin	all open
JP7	2 pin	I	JP29	2 pin	0
JP8	2 pin	0	JP30	3 pin	all open
JP9	2 pin	0	JP31	2 pin	0
JP10	2 pin	I	JP32	3 pin	all open
JP13	2 pin	0	JP33	2 pin	0
JP14	2 pin	I	JP34	3 pin	all open
JP15	3 pin	1 to 2	JP35	2 pin	0
JP16	3 pin	1 to 2	JP36	3 pin	all open
JP17	2 pin	0	JP39	2 pin	0
JP18	3 pin	all open	JP40	2 pin	0
JP19	2 pin	0	JP41	2 pin	0
JP20	3 pin	all open	JP43	2 pin	I
JP21	2 pin	0			
JP22	3 pin	all open	J36	5x2 Hdr	All 5 installed

Table 2.1. Si5386A-E-EVB Jumper Defaults\*

## 3. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D11	INTRB	Blue	DUT Interrupt Active
D12	LOLB	Blue	DUT Loss of Lock Indicator
D21	READY	Green	MCU Ready
D22	3P3V	Blue	DUT +3.3 V is present
D24	BUSY	Green	MCU Busy
D25	INTR	Red	MCU Interrupt active
D26	VDD DUT	Blue	DUT VDD voltage present
D27	5VUSBMAIN	Blue	Main USB +5 V present

#### Table 3.1. Si5386A-E-EVB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5386 +3.3 V, and Si5386 Output +5 V supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. D11 and D12 are status indicators from the DUT.

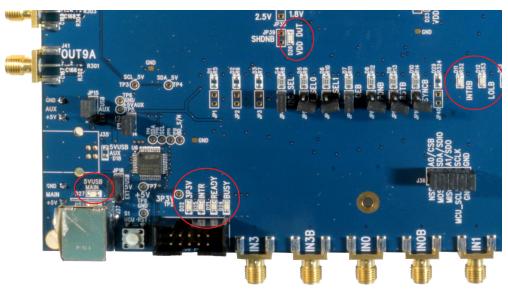


Figure 3.1. Status LEDs

UG513: Si5386A-E Evaluation Board User's Guide • External Reference Input (XA/XB)

## 4. External Reference Input (XA/XB)

An external XO is used to produce an ultra-low jitter reference clock for the DSPLL and to provide a stable reference for the free-run and holdover modes. The XO footprint on the Si5386A-E-EVB can accommodate both 3.2mm x 5 mm and 2.5 mm x 3.2 mm package sizes. The XO frequency must be 54 MHz (recommended) or 48.0231 MHz for Si5386A devices.

When JP43 is shorted the XO shares the VDD\_3.3V DUT power supply sourced from an on-board ultra low noise LDO. When JP43 is left open an external supply must be used to power the XO. See section 9 for Si5386A-E-EVB schematic details.

**Note:** The remaining components marked "NI" are not installed.

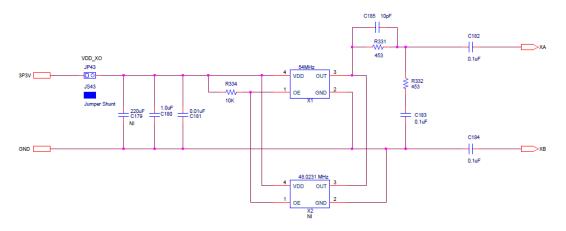


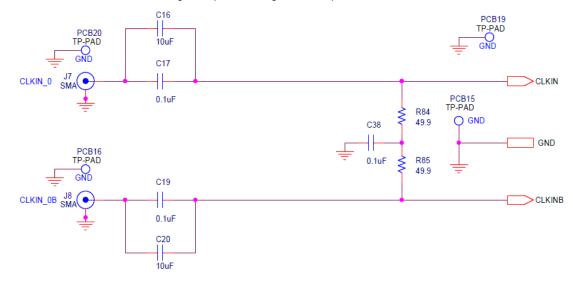
Figure 4.1. External Reference Input Circuit

UG513: Si5386A-E Evaluation Board User's Guide • Clock Input and Output Circuits

## 5. Clock Input and Output Circuits

#### 5.1 Clock Input Circuits (INx/INxB and FB\_IN/FB\_INB)

The Si5386A-E-EB has eight SMA connectors (IN0/IN0B–IN2/IN2B and IN3(FB\_IN)/IN3B(FB\_INB)) for receiving external clock signals. All input clocks are terminated as shown in the figure below. Note input clocks are ac coupled and 50  $\Omega$  terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5386 data sheet.





#### 5.2 Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5386A-E-EB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5386A-E-EB, and provide locations on the PCB for optional dc/ac terminations by the end user.

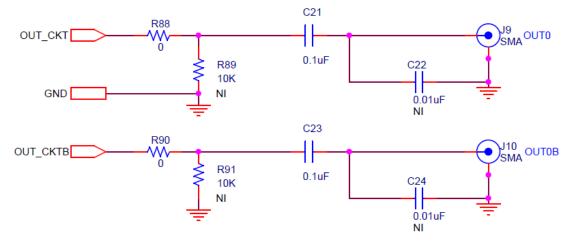


Figure 5.2. Output Clock Termination Circuit

## 6. Using the Si5386 EVB and Installing ClockBuilder Pro Desktop Software

#### 6.1 Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any Windows 7 (or above) PC:

Go to Timing - Clockbuilder Pro Software and download the ClockBuilder Pro software.

Installation instructions, release notes, and a user's guide for ClockBuilder Pro can be found at the download link shown above. Follow the instructions as indicated.

#### 6.2 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software in installed, connect to the EVB with a USB cable as shown below.

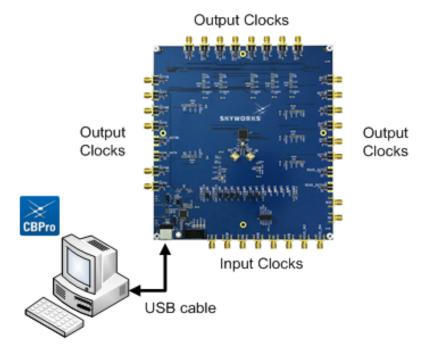


Figure 6.1. EVB Connection Diagram

#### 6.3 Additional Power Supplies

The Si5386A-E-EB comes preconfigured with jumpers installed on JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain +5 V power to all EVB power solely through the J37 USB connector. This setup is the default EVB configuration and is sufficient to configure the device and run multiple clock outputs simultaneously.

In some cases when enabling all outputs or at high output frequencies, the EVB requires more power than a single USB connection can provide. This may result in intermittent device behavior or unexplained increases in jitter/phase-noise. This condition may be checked using the EVB GUI, which is described further below. Selecting the "**All Voltages**" tab of the GUI and clicking on the "**Read All**" button produces a display similar to this one:

nfo	DUT SPI	DUT Setting	gs Editor	DUT Register Editor	Phase INC/DEC	Regulators	All Voltages	GPIO	Status Regist
Volt	age @ Reg	ulator Pins			Voltage @ Regu	lator			
		VDD_PIN	1.953 V	Read	v	DD_REG	1.781 V 🗌	Read	
	١	/DDA_PIN	3.282 V	Read	VD	DA_REG	3.281 V	Read	
	VE	DO0_PIN	0.000 V	Read	VDD	OO_REG (	0.000 V	Read	
	VE	DO1_PIN	0.000 V	Read	VDD	O1_REG (	0.000 V	Read	
	VE	DO2_PIN	0.000 V	Read	VDD	O2_REG (	0.000 V	Read	
	VE	DO3_PIN	0.000 V	Read	VDD	O3_REG (	0.000 V 🗌	Read	
	VE	DO4_PIN	0.000 V	Read	VDD	O4_REG (	0.000 V 🗌	Read	
	VE	DO5_PIN	0.000 V	Read	VDD	O5_REG (	0.000 V 🗌	Read	
	VE	DO6_PIN	0.000 V	Read	VDD	O6_REG (	0.000 V 🗌	Read	
	VE	DO7_PIN	0.000 V	Read	VDD	O7_REG (	0.000 V 🗌	Read	
	VE	DO8_PIN	0.000 V	Read	VDD	O8_REG (	0.000 V 🗌	Read	
	VE	DO9_PIN	0.000 V	Read	VDD	O9_REG (	0.000 V	Read	
Miso	: Rails								
		RAIL_5V	4.902 V	Read					
	R	AIL_3P3V	3.324 V	Read					

Figure 6.2. EVB GUI - Power Supply Check

Verify that the "**RAIL\_5V**" measurement shows the EVB voltage > 4.6 V. An EVB voltage lower than this level may cause the issues described above.

In this case, J33 can be used to provide power to the output drivers separately from the main Si5386 device supplies. To make this change, move jumper JP15 to connect pins 2-3 "EXT". Connect J33 to an external 5 V, 0.5A or higher, power source. Make sure that the polarity of the +5 V and GND connections are correct. Verify that the RAIL\_5V voltage is 4.7 V or higher. The EVB should be powered by the USB connector when turning this auxiliary 5 V supply on or off.

See the figure below for the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

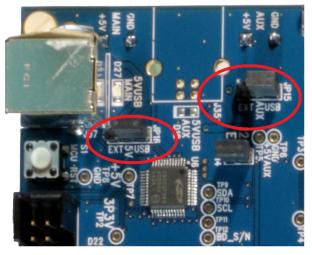


Figure 6.3. JP15-JP16 Standard Jumper Shunt Installation

#### 6.4 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilder Pro installer will install two main applications.

#### **Application 1:**

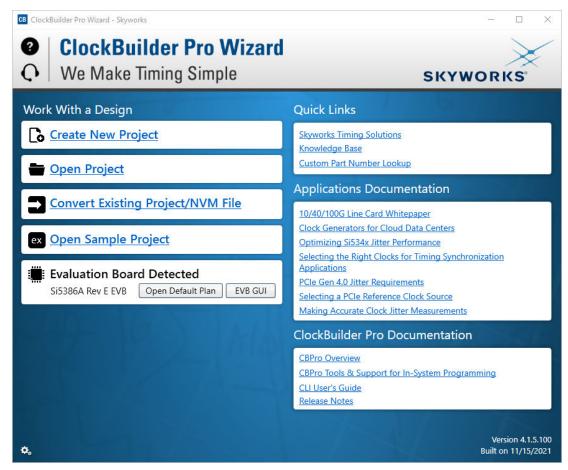


Figure 6.4. ClockBuilder Pro Wizard

Use the CBPro Wizard to do the following:

- · Create a new design.
- Review or edit an existing design.
- · Export: Create in-system programming files.

#### **Application 2:**

Help	Р									
fo D	DUT SPI [	OUT Settings Editor	DUT Re	gister Editor	Phase INC/DEC	Regulators	All Voltages	GPIO	Status Re	Control Registers
				Voltage	Current	Power				Soft Reset and Calibration
	VDD	1.80V	On	1.781 V	174 mA	310 mW	Read			SOFT_RST_ALL
	VDDA	3.30V	On	3.286 V	125 mA	411 mW	Read			SOFT_RST
	VDDO0	1.80V	Off	0.004 V	0 mA	0 mW	Read			Hard Reset, Sync, & Power Do
	VDDO1	1.80V	Off	0 V	0 mA	0 mW	Read			HARD_RST
	VDDO2	1.80V	On	1.796 V	0 mA	0 mW	Read			SYNC
	VDD03	1.80V	Off	0.009 V	0 mA	0 mW	Read			PDN: 0
	VDDO4	1.80V	On	1.791 V	0 mA	0 mW	Read			
	VDDO5	1.80V	Off	0 V	0 mA	0 mW	Read			
	VDDO6	1.80V	On	1.785 V	0 mA	0 mW	Read			
	VDDO7	1.80V	Off	0.004 V	0 mA	0 mW	Read			
	VDDO8	1.80V	On	1.800 V	0 mA	0 mW	Read			
	VDDO9	1.80V	Off	0 V	0 mA	0 mW	Read			
	output 🔽	Select Voltage	🔽	Total	299 mA	0.721 W	Read All			
Sup	pplies	Power On	ower Off	Co	mpare Design Es	timates to Me	asurements			
q										
9 Itered	Ι 🔽 Αι	ito Scroll: On 두	Insert	Marker	Clear Copy	y to Clipboard	I Pause			
mesta	imp Sou	rce Message								
5:19:20	0.634 EVB			Regulator(reg wer: 0.000W	ulator_id=VDD_9	)) => Voltage	Reg: 0.000V, 1	/oltage_l	Pin: 0.000V,	

Figure 6.5. EVB GUI

Use the EVB GUI to do the following:

- · Download configuration to EVB's DUT (Si5386).
- · Control the EVB's regulators.
- Monitor voltage, current, power on the EVB.

#### 6.5 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5386A-E-EB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Skyworks-created Default Configuration
- · Workflow Scenario #2: Modifying the Default Skyworks-created Device Configuration
- Workflow Scenario #3: Testing a User-created Device Configuration

Each is described in more detail in the following sections.

#### 6.6 Workflow Scenario #1: Testing a Skyworks-Created Default Configuration

Verify that the PC and EVB are connected, then launch ClockBuilder Pro by clicking on this icon on your PC's desktop:



Figure 6.6. ClockBuilder Pro Icon

CBPro automatically detects the EVB and device type. When the EVB has been detected, click on the "Open Default Plan" button.

CB Clock	Builder Pro Wizard - Skyworks
9 ()	<b>ClockBuilder Pro Wizard</b> We Make Timing Simple
Work	with a Design
[ò	Create New Project
-	<u>Open Project</u>
٦	Convert Existing Project/NVM File
ex	Open Sample Project
	Evaluation Board Detected Si5386A Rev E EVB Open Default Plan EVB GUI

Figure 6.7. CBPro—Open Default Plan Button

Once you open the default plan, a popup will appear.



Figure 6.8. CBPro—Write Design Dialog

Select "Yes" to write the default plan to the Si5386 device mounted on your EVB. This ensures the device on the EVB is configured with the latest parameters from Skyworks.

Writing Si53	86A Design	to EVB		
Address 0x01	22			

Figure 6.9. CBPro—Write Progress Window

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown in the figure below.

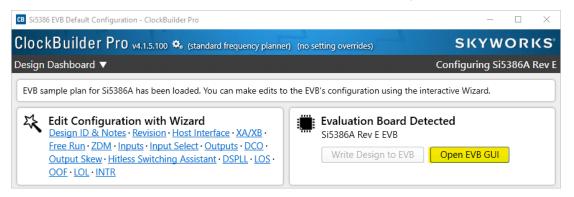


Figure 6.10. CBPro-Open EVB GUI Button

The EVB GUI window will appear on the desktop. Note all power supplies on the "**Regulators**" tab will be set to the values defined in the device's default CBPro project, as shown in the figure below.

e Help									
nfo DUT SPI	DUT Setting	s Editor	DUT Reg	ister Editor	Phase INC/DEC	Regulators	All Voltages	GPIO	Status R
				Voltage	Current	Power			
VE	D 1.80V		n	1.781 V	174 mA	310 mW	Read		
VDE	A 3.30V		n	3.286 V	125 mA	411 mW	Read		
VDDO	2.50V		n	0.004 V	0 mA	0 mW	Read		
VDDO	2.50V		n	0 V	0 mA	0 mW	Read		
VDDO	2 2.50V		n	1.796 V	0 mA	0 mW	Read		
VDDO	03 2.50V		n	0.009 V	0 mA	0 mW	Read		
VDDO	2.50V		n	1.791 V	0 mA	0 mW	Read		
VDDC	05 1.80V		Off	0 V	0 mA	0 mW	Read		
VDDC	06 1.80V		Off	1.785 V	0 mA	0 mW	Read		
VDDC	07 1.80V		Off	0.004 V	0 mA	0 mW	Read		
VDDO	2.50V		n	1.800 V	0 mA	0 mW	Read		
VDDC	09 2.50V		n	0 V	0 mA	0 mW	Read		
All Output	Select V	oltage	•	Total	299 mA	0.721 W	Read All		
Supplies	L Power C	n Po	wer Off	Co	mpare Design Est	imates to Me	asurements		

Figure 6.11. EVB GUI—Regulators

#### 6.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have yet been connected to the INPUT CLOCK differential SMA connectors, labeled "INx/INxB" and located around the perimeter of the EVB, the DUT should now be operating in free-run mode and locked to the onboard XO.

You can run a quick check to determine if the device is powered up, generating output clocks, and consuming power by clicking on the "**Read All**" button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

**Note:** Turning  $V_{DD}$  or  $V_{DDA}$  "Off" will power-down and reset the DUT. Once both of these supplies are turned "On" again, you must reload the desired frequency plan back into the device memory by selecting the "**Write Design to EVB**" button on the CBPro home screen:

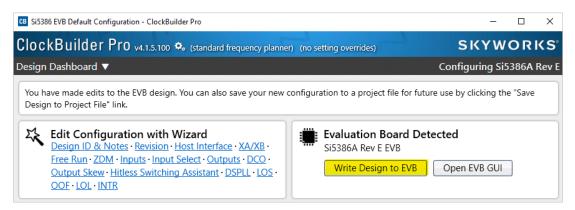


Figure 6.12. CBPro—Write Design Button

Failure to do the step above will cause the device to read in the preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Skyworks for evaluation.

At this point, you should verify the presence and frequencies of the output clocks, running in free-run mode from the XO, using external instrumentation connected to the output clock SMA connectors, labeled OUTx/OUTs. To verify plan inputs, go to the appropriate configuration page or click on "Frequency Plan Valid" to see the design report.

CB Si5386 EVB Default Configuration - ClockBuilder Pro	- D X
ClockBuilder Pro v4.1.5.100 🌣 (standard frequency planner	) (no setting overrides) SKYWORKS
Design Dashboard 🔻	Configuring Si5386A Rev E
You have made edits to the EVB design. You can also save your new c Design to Project File" link.	configuration to a project file for future use by clicking the "Save
Edit Configuration with Wizard           Design ID & Notes • Revision • Host Interface • XA/XB •           Free Run • ZDM • Inputs • Input Select • Outputs • DCO •           Output Skew • Hitless Switching Assistant • DSPLL • LOS •           OOF • LOL • INTR	Evaluation Board Detected Si5386A Rev E EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time. In engineering mode, you can <u>save this project</u> <u>unencrypted</u> .	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a design report (text) or create a draft datasheet addendum (PDF) for your design.	Documentation Si5386 Family Reference Manual Si5386 Datasheet Si5386 EVB User's Guide
<b>Skyworks Cloud Services</b> You can <u>create a custom part number</u> for your design, which can be used to order factory pre-programmed devices. Or <u>request a phase noise report</u> for this design.	Ask for Help Have a question about your design? Click here to get assistance.
Frequency Plan Valid Obsign OK Styrical Pd 1.17 W, Tj 50 °C Est Worst Pd 1.57 W, Tj 119	Home Close

Figure 6.13. CBPro—Design Report Button and Link

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

B Si5386A D	esign Report	-		>
esign Repo	ort			
	U			
Design				C
Host Inte				
I/O Po	wer Supply: VDD (Core)			
	de: 4-Wire			
I2C Ad	dress Range: 104d to 107d / 0x68 to 0x6B (selected via /	AØ/A1 p	oins)	
XA/XB:				
54 MHz	(XO - External Oscillator)			
Inputs:				
IN0:	Unused			
IN1:	30.72 MHz			
	Standard Differential and Single-ended			
	Unused			
IN3:	Unused			
Outputs:				
	153.6 MHz			
	Enabled, LVDS 2.5 V			
	30.72 MHz			
	Enabled, LVDS 2.5 V			
	491.52 MHz			
	DCLK to SYSREF OUT2			
	Enabled, LVDS 2.5 V			
	1.92 MHz			
	SYSREF of DCLK OUT1			
	Enabled, LVDS 2.5 V			
	245.76 MHz			
	DCLK to SYSREF OUT4 Enabled, LVDS 2.5 V			
	1.92 MHz			
0014:	1.92 MHZ SYSREF of DCLK OUT3			
	Enabled, LVDS 2.5 V			
	Unused			
	Unused			
00101	onuseu			
Conveto C	ipboard Save Report Ask for Help		Close	0

Figure 6.14. CBPro—Design Report

#### 6.6.2 Verify Locked Mode Operation

Now, assuming that you connect the input clocks to the EVB as shown in the Design Report above, the DUT on your EVB will be running in "locked" mode.

#### 6.7 Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration

To modify the configuration using the CBPro Wizard, click on the appropriate category. The category may also be selected from a dropdown list by clicking on the "**Design Dashboard**" button above this section.

CB Si5386 EVB Default Configuration - ClockBuilder Pro	- 🗆 X
ClockBuilder Pro v4.1.5.100 🍫 (standard frequency planner)	(no setting overrides)
Design Dashboard 🔻	Configuring Si5386A Rev E
You have made edits to the EVB design. You can also save your new co Design to Project File" link.	nfiguration to a project file for future use by clicking the "Save
Edit Configuration with Wizard Design ID & Notes • Revision • Host Interface • XA/XB • Free Run • ZDM • Inputs • Input Select • Outputs • DCO • Output Skew • Hitless Switching Assistant • DSPLL • LOS • OOF • LOL • INTR	Evaluation Board Detected Si5386A Rev E EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time. In engineering mode, you can <u>save this project</u> <u>unencrypted</u> .	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation Si5386 Family Reference Manual Si5386 Datasheet Si5386 EVB User's Guide
<b>Skyworks Cloud Services</b> You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Click here to get assistance.
Frequency Plan Valid Obesign OK Typical Pd 1.17 W, Tj 50 °C Est Worst Pd 1.57 W, Tj 119	C Home Close

Figure 6.15. CBPro—Edit Settings Links and Pulldown

You will now be taken to the Wizard's step-by-step menu pages to allow you to change any of the default plan's operating configurations.

Step 1 of 17 - Design ID 8 Design ID The device has 8 registers, DE Design ID: The strir Padding Mode: ONUL If yc char Spa If yc char Design Notes Enter anything you want here	v4.1.5.100 🗘 (standard frequency planner) (no setting overrides) Notes  SIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/r (optional; max 8 characters) g you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN L Padded u do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pacter). e Padded u do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pacter).	_ID7. Ided with 0x00 bytes (aka NULL
Design ID The device has 8 registers, DE Design ID: The strin Padding Mode: In VUL If yc char Spa If yc char Design Notes Enter anything you want here	SIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/r (optional; max 8 characters) g you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN L <b>Padded</b> u do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pac citer). e <b>Padded</b> u do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pac	evision identifier. _ID7. Ided with 0x00 bytes (aka NULL
The device has 8 registers, DE Design ID: The strin Padding Mode: Infyce If yce Char If yce Char If yce Char If yce Char If yce Char If string Spac If yce Char If	(optional; max 8 characters) g you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN L Padded u do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pac acter). e Padded u do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pac	_ID7. Ided with 0x00 bytes (aka NULL
Padding Mode:  NUL If yc Char Spa- If yc char Design Notes Enter anything you want here	L Padded J do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pac scter). e Padded J do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pac	ded with 0x00 bytes (aka NULL
Enter anything you want here		
	The text is stored in your project file and included in design reports and custom p d in reports, you can use newlines to start a new paragraph.	art number datasheet addendums.
Frequency Plan Valid		

Figure 6.16. CBPro—Design ID and Notes Edit Page

As you edit the settings, you may notice the "**Frequency Plan Valid**" link in the lower left corner updating. You can click on this link to bring up the design report to confirm that the information is correct. When you are finished editing each page, you may click on the "> Next" or "< Back" buttons to move from page to page. When you are done making all your desired changes, you can click on "Write to EVB" to reconfigure your device. The Design Write status window will appear each time you write to the EVB.

Writing Si53	886A Design to EVB
Address 0x0	128

Figure 6.17. CBPro—Design Write Progress Window

When you have verified your design settings, you may save the design project. Click on the "**Finish**" button to return to the home page and then click on the "**Save Design to Project File**" link. You can use the windows file browser to reach the correct location and enter a filename for this new project.

#### 6.8 Workflow Scenario #3: Testing a User-Created Device Configuration

CB ClockBuilder Pro Wizard - Skyworks	- 🗆 X				
<ul> <li>ClockBuilder Pro Wizard</li> <li>We Make Timing Simple</li> </ul>	SKYWORKS				
Work With a Design	Quick Links				
Create New Project	Skyworks Timing Solutions Knowledge Base				
🖶 <mark>Open Project</mark>	Custom Part Number Lookup				
Convert Existing Project/NVM File	Applications Documentation 10/40/100G Line Card Whitepaper				
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance				
Evaluation Board Detected Si5386A Rev E EVB Open Default Plan EVB GUI	Selecting the Right Clocks for Timing Synchronization Applications PCle Gen 4.0 Jitter Requirements Selecting a PCle Reference Clock Source Making Accurate Clock Jitter Measurements				
LUL GAS MA	ClockBuilder Pro Documentation				
	CBPro Overview CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes				
<b>⇔</b> ₀	Version 4.1.5.100 Built on 11/15/2021				

Figure 6.18. CBPro—Open Design Project Link

Using the windows file browser popup, locate your CBPro design file (\*.slabtimeproj or \*.sitproj file).

CB Open CBPro Project File		
$\leftarrow$ $\rightarrow$ $\checkmark$ $\bigstar$ $\blacksquare$ $\Rightarrow$ This PC $\Rightarrow$ Documents $\Rightarrow$ CBPro	・  で Search CBPro	Q
Organize 🔻 New folder		?
A Name	Date modified Type Size	
GICK access	12/15/2021 4:40 PM Skyworks Timing 13	KB
<ul> <li>This PC</li> <li>3D Objects</li> <li>Desktop</li> <li>Documents</li> </ul>		
File name: Si5386A-RevE-Project	<ul> <li>Skyworks Timing Project</li> <li>Open</li> <li>Cancel</li> </ul>	~ 

Figure 6.19. CBPro—Windows File Browser

Select "Yes" when the WRITE DESIGN to EVB popup appears:

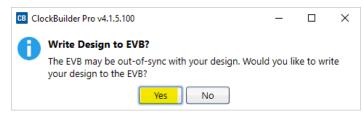


Figure 6.20. CBPro—Write Design Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

#### 6.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

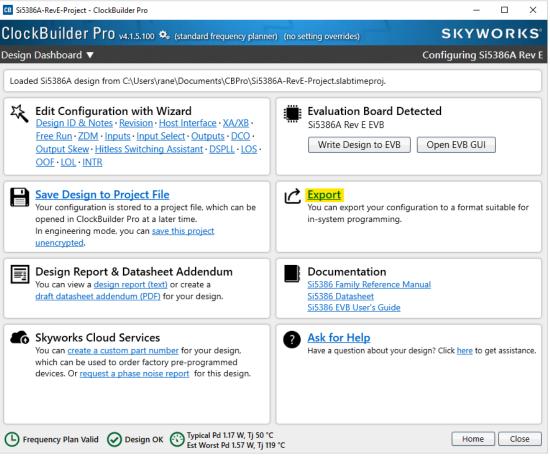


Figure 6.21. CBPro-Export Design Programming File

You can now write your device's complete configuration to file formats suitable for in-system programming.

ntroduction	Register File	Settings File	Multi-Project Register/Settings	Regmap			
About Regi	ster Export						
This export configuration		e registers that	need to be written to the Si53	86A to achi	eve your desi	gn/	
	d line version o prompt to learr		ailable. Type CBProProjectRegi	stersExpor	thelp from	a	
Options							
Export Type	21						
Each and c		Values (CSV) Fil is an address,d	e ata pair in hexadecimal format.	A comma	separates the	address	
The r used		ware code.	ressed in C code via an array of	address,da	ta pairs. This	can be	
If check	ed, an informa I by the # char	tional header v	vill be included at the top of th ler will contain some basic info				
Certain This ens the dow	control registe sures the devic	e is stable duri	egister writes tten before and after writing th ng configuration download and urn inclusion of this sequence o	l resumes r	ormal operat	ion after	9

Figure 6.22. CBPro—Export Configuration Window

UG513: Si5386A-E Evaluation Board User's Guide • Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

## 7. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

The Si5386 device loads the Non-Volatile Memory (OTP) on either a powerup or a hard reset, overwriting any previous volatile register changes. This allows the device to begin functioning as desired on powerup/hard-reset without manual intervention. To restart the device while preserving volatile changes and without loading the OTP, use soft-reset through the registers or EVB-GUI.

**Note:** Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5386 using ClockBuilder Pro on the Si5386 EVB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5386 RAM space and can be done virtually an unlimited number of times. Writing to OTP is limited as described below.

Refer to the Si5386 Family Reference Manual and device datasheet for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

UG513: Si5386A-E Evaluation Board User's Guide • Serial Device Communications (Si5386 <-> MCU)

## 8. Serial Device Communications (Si5386 <-> MCU)

#### 8.1 Onboard SPI Support

The MCU on-board the Si5386A-E-EB communicates with the Si5386 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5386 device is the SPI slave. The Si5386 device can also support a 2-wire I<sup>2</sup>C serial interface, although the Si5386A-E-EB does NOT support the I<sup>2</sup>C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I<sup>2</sup>C.

#### 8.2 External I<sup>2</sup>C Support

I<sup>2</sup>C can be supported if driven from an external I<sup>2</sup>C controller. The serial interface signals between the MCU and Si5386 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I<sup>2</sup>C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5386 device. The shunt at J4 (I2C\_SEL) must also be removed to select I<sup>2</sup>C as Si5386 interface type. An external I<sup>2</sup>C controller connected to the Si5386 side of J36 can then communicate to the Si5386 device. (For more information on I<sup>2</sup>C signal protocol, please refer to the Si5386 data sheet.)

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5386 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4, I<sup>2</sup>C operation should use J36 pin 4 (DUT\_SDA\_SDIO) as the I<sup>2</sup>C SDA and J36 pin 8 (DUT\_SCLK) as the I<sup>2</sup>C SCLK. Please note the external I<sup>2</sup>C controller will need to supply its own I<sup>2</sup>C signal pull-up resistors.

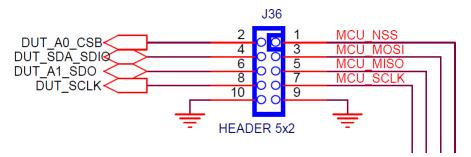


Figure 8.1. Serial Communications Header J36

UG513: Si5386A-E Evaluation Board User's Guide • Si5386A-E-EB Schematic and Bill of Materials (BOM)

## 9. Si5386A-E-EB Schematic and Bill of Materials (BOM)

The Si5386 EVB Schematic and Bill of Materials (BOM) can be found online at: https://www.skyworksinc.com/search?q=si538%20evaluation

Note: Please be aware the Si5386 EVB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

## SKYWORKS

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