UC1843B-SP QML Class V, Radiation Hardened Current-Mode PWM Controller

1 Features

- QML class V (QMLV) qualified, SMD 5962-86704
- 5962**R**8670412VYC:
  - Radiation hardness assurance (RHA) up to 100-krad(Si) total ionizing dose (TID)
- Optimized for offline and DC-to-DC converters
- Low start-up current (< 0.5 mA)
- Trimmed oscillator discharge current
- Automatic feed forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lockout (UVLO) with hysteresis
- Double-pulse suppression
- High-current totem-pole output
- Internally-trimmed bandgap reference
- 500-kHz operation
- Low R_O error amplifier

2 Applications

- DC-DC converters
- Communications payload
- Optical imaging payload
- Radar imaging payload
- Supports various topologies:
  - Flyback, forward buck, boost
  - Push-pull, half-bridge, full-bridge with external interface circuit

3 Description

The UC1843B-SP control IC is a radiation hardened pin-for-pin compatible version of the UC1843A-SP. Providing the necessary characteristics to control current-mode switched-mode power supplies, this device has improved features. Start-up current is specified to be less than 0.5 mA and oscillator discharge is trimmed to 8.3 mA. During UVLO, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

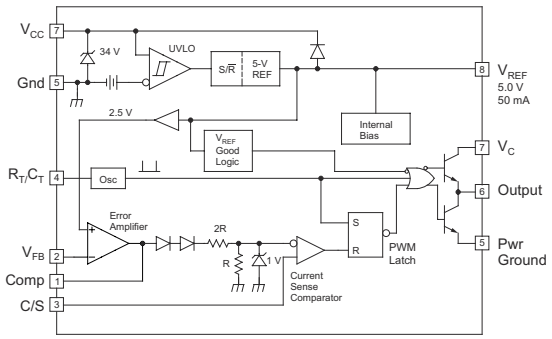
Device Information

PART NUMBER(1)	GRADE(2)	PACKAGE
5962R8670412VYC	Flight grade QMLV-RHA 100 krad(Si)	CFP/HKU (10) 6.48 mm × 7.02 mm
UC1843BHKU/EM	Engineering samples(3)	
5962R8670412V9A	Flight grade QMLV-RHA KGD 100 krad(Si)	Die

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) For additional information about part grade, view SLYB235.

(3) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2019) to Revision B (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *Applications* section	1
• Updated Device Information table in *Description* section	1
• Added Bare Die Information table to *Pin Configuration and Functions* section	3
• Added UC1843B-SP Bare Die Pin Locations figure to *Pin Configuration and Functions* section	3
• Added Bond Pad Coordinates in Microns table to *Pin Configuration and Functions* section	3

Changes from Revision * (April 2019) to Revision A (September 2019)	Page
• Changed the package image in the *Pin Configuration and Functions* section	3
• Changed <10 mA To: <17 mA in Figure 7-5	11

5 Pin Configuration and Functions

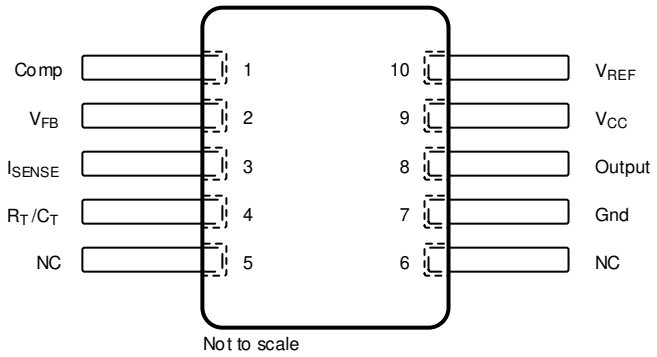


Figure 5-1. HKU Package
10-Pin CFP
Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Comp	1	I	Error amplifier output.
V_{FB}	2	I	Voltage feedback input to error amplifier.
I_{SENSE}	3	I	Current sense comparator input pin.
R_T/C_T	4	I	RC time constant input to oscillator.
NC	5, 6	—	No connect.
Gnd	7	—	Ground.
Output	8	O	Regulated output.
V_{CC}	9	—	Unregulated supply voltage.
V_{REF}	10	O	5-V internally generated reference.

Table 5-2. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Backgrind Si - Finish	Ground	AlCu	2000 nm

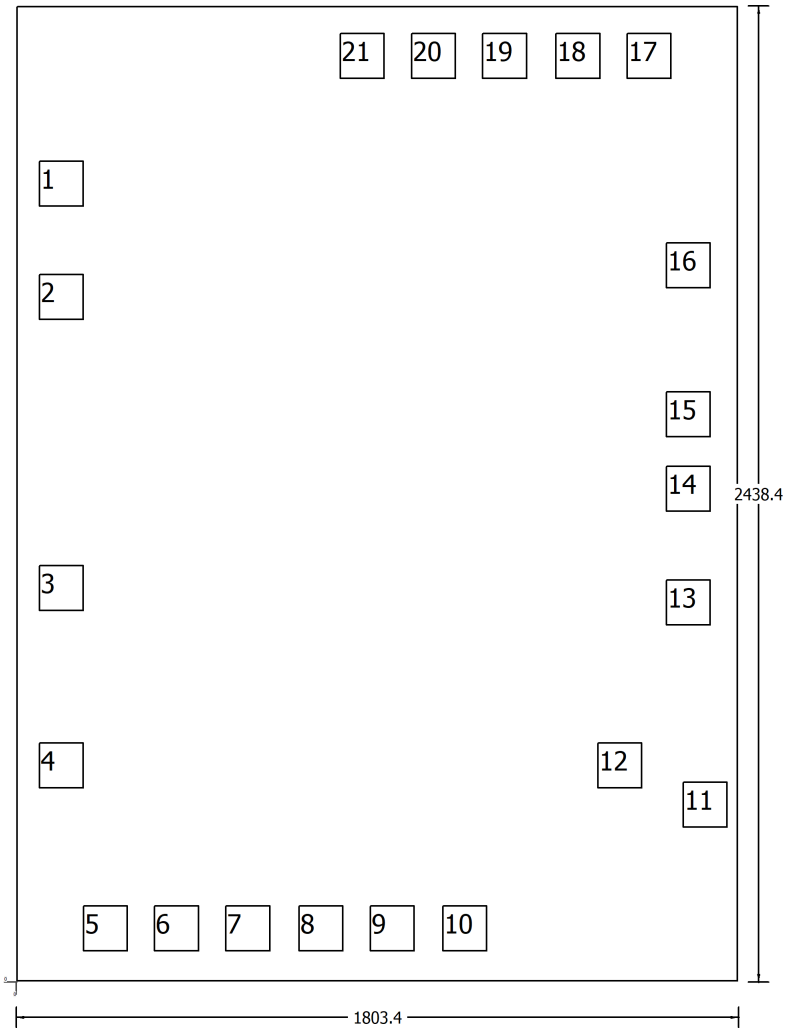


Figure 5-2. UC1843B-SP Bare Die Pin Number Locations

Table 5-3. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
COMP	1	55.88	1935.458	170.181	2052.3
VFB	2	55.88	1651.829	170.181	1768.671
ISENSE	3	55.88	925.028	170.181	1041.87
Rt/Ct	4	55.88	481.858	170.181	598.7
N/C	5	165.623	74.746	279.925	191.588
N/C	6	343.425	74.746	457.726	191.588
N/C	7	521.227	74.746	635.528	191.588
N/C	8	704.109	74.746	818.41	191.588
N/C	9	881.91	74.746	996.211	191.588
N/C	10	1062.932	74.746	1177.234	191.588
GND	11	1662.756	384.359	1777.057	501.201
GND	12	1449.69	481.858	1563.991	598.7
OUTPUT	13	1620.685	889.041	1734.986	1005.883
VCC	14	1620.685	1172.67	1734.986	1289.512
VCC	15	1620.685	1358.803	1734.986	1475.644
VREF	16	1620.685	1731.066	1734.986	1847.907
N/C	17	1523.03	2254.009	1637.331	2370.85
N/C	18	1345.228	2254.009	1459.529	2370.85
N/C	19	1162.346	2254.009	1276.647	2370.85
N/C	20	984.544	2254.009	1098.846	2370.85
N/C	21	806.742	2254.009	921.043	2370.85

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, low-impedance source(1)		30	V
V_I	Input voltage (V_{FB}, I_{SENSE})	–0.3	6.3	V
	Supply current	Self limiting		
I_O	Output current		±1	A
	Error amplifier output sink current		10	mA
	Output energy (capacitive load)		5	µJ
P_D	Power dissipation (T_A = 25°C)		1	W
T_{lead}	Lead temperature (soldering, 10 s)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Current limiting this input will allow for higher supply voltages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (T_A = T_J = –55°C to 125°C), unless otherwise noted

		MIN	MAX	UNIT
V_{CC}	Supply voltage	12	25	V
	Sink/source output current (continuous or time average)	0	200	mA
	Reference load current	0	20	mA

6.4 Thermal Information

THERMAL METRIC(1)		UC1843B-SP HKU (CFP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.42	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{CC} = 15 V[1], R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J = 25°C, I_O = 1 mA		4.85	5	5.1	V
Line regulation	V_{IN} = 12 to 25 V			6	20	mV
Load regulation	I_O = 1 to 20 mA			6	25	mV
Temperature stability[2] [3]				0.2	0.4	mV/°C
Total output variation[2]	Over line, load, and temperature		4.85		5.1	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C			50		μV
Long-term stability	1000 hours, T_A = 125°C[2]			5	25	mV
Short-circuit output current			–30	–100	–180	mA
OSCILLATOR						
Initial accuracy	T_J = 25°C[4]		47	52	57	kHz
Voltage stability	V_{CC} = 12 to 25 V			0.2%	1%	
Temperature stability	T_J = –55°C to 125°C[2]			5%		
Amplitude peak-to-peak	V pin 4[2]			1.7		V
Discharge current	V pin 4 = 2 V[5]	T_J = 25°C	7.8	8.3	8.8	mA
		T_J = Full range	7.5		8.8	
ERROR AMPLIFIER						
Input voltage	V_{Comp} = 2.5 V		2.45	2.50	2.55	V
Input bias current				–0.3	–1	μA
Open-loop voltage gain	V_O = 2 to 4 V		65	90		dB
Unity-gain bandwidth	T_J = 25°C[2]		0.7	1		MHz
PSRR	V_{CC} = 12 to 25 V		60	70		dB
Output sink current	V_{FB} = 2.7 V, V_{Comp} = 1.1 V		2	6		mA
Output source current	V_{FB} = 2.3 V, V_{Comp} = 5 V		–0.5	–0.8		mA
High-level output voltage	V_{FB} = 2.3 V, R_L = 15 kΩ to ground		5	6		V
Low-level output voltage	V_{FB} = 2.7 V, R_L = 15 kΩ to V_{REF}			0.7	1.1	V
CURRENT SENSE						
Gain[6] [7]			2.85	3	3.15	V/V
Maximum input signal	V_{Comp} = 5 V[6]		0.9	1	1.1	V
PSRR	V_{CC} = 12 to 25 V[6]			70		dB
Input bias current				–2	–10	μA
Delay to output	V_{ISENSE} = 0 to 2 V[2]			150	300	ns

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Output low-level voltage	I_{SINK} = 20 mA		0.1	0.4	V
	I_{SINK} = 200 mA		1.5	2.2	
Output high-level voltage	I_{SOURCE} = –20 mA	13	13.5		V
	I_{SOURCE} = –200 mA	12	13.5		
Rise time	C_L = 1 nF, T_J = 25°C(2)		50	150	ns
Fall time	C_L = 1 nF, T_J = 25°C(2)		50	150	ns
UVLO saturation	V_{CC} = 5 V, I_{SINK} = 10 mA		0.7	1.2	V
UNDERVOLTAGE LOCKOUT					
Start threshold		7.8	8.4	9	V
Minimum operation voltage after turnon		7	7.6	8.2	V
PWM					
Maximum duty cycle		94%	96%	100%	
Minimum duty cycle				0%	
TOTAL STANDBY CURRENT					
Start-up current			0.3	0.5	mA
Operating supply current	V_{FB} = V_{ISENSE} = 0 V		11	17	mA
V_{CC} Zener voltage	I_{CC} = 25 mA	30	34		V

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) Parameters ensured by design and/or characterization, if not production tested.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation: Temperature Stability = V_{REF} (max) – V_{REF} (min) / T_J (max) – T_J (min). V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency.
(5) This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 µA of current to the measurement. The total current flowing into the R_T or C_T pin will be approximately 300 µA higher than the measured value.
(6) Parameter measured at trip point of latch with V_{FB} = 0 V.
(7) Gain defined as: G = ΔV_{Comp} / ΔV_{ISENSE}; V_{ISENSE} = 0 to 0.8 V.

6.6 Typical Characteristics

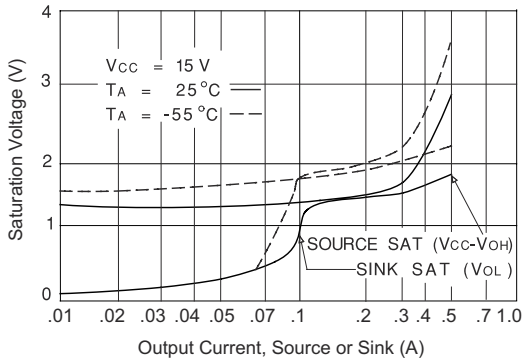


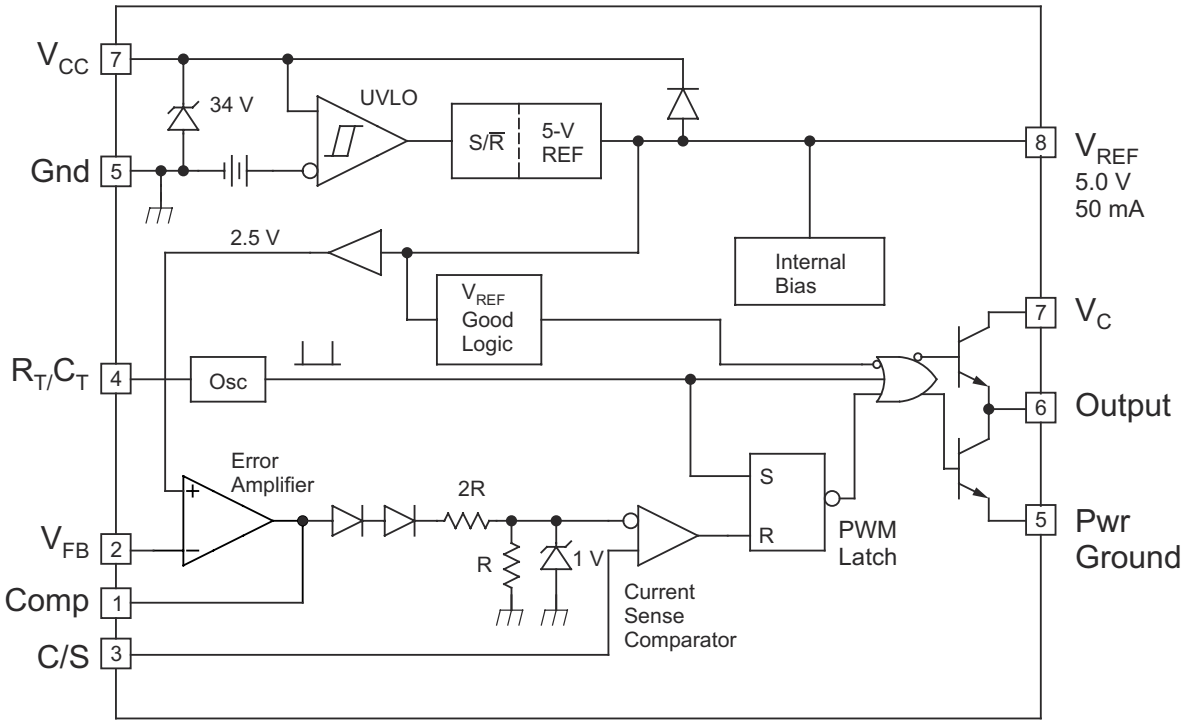
Figure 6-1. Output Saturation Characteristics

7 Detailed Description

7.1 Overview

The UC1843B-SP control IC is a pin-for-pin compatible improved version of the UC1843A-SP. Providing the necessary characteristics to control current-mode switched-mode power supplies, this device has improved features. Start-up current is specified to be less than 0.5 mA and oscillator discharge is trimmed to 8.3 mA. During UVLO, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

7.2 Functional Block Diagram



7.3 Feature Description

UC1843B-SP is a current mode controller, used to support various topologies such as forward, flyback, buck, and boost. Using an external interface circuit will also support half-bridge, full-bridge, and push-pull configurations.

Figure 7-1 shows the two-loop current-mode control system. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way, the error signal actually controls peak inductor current. This contrasts with voltage control in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; that is, the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

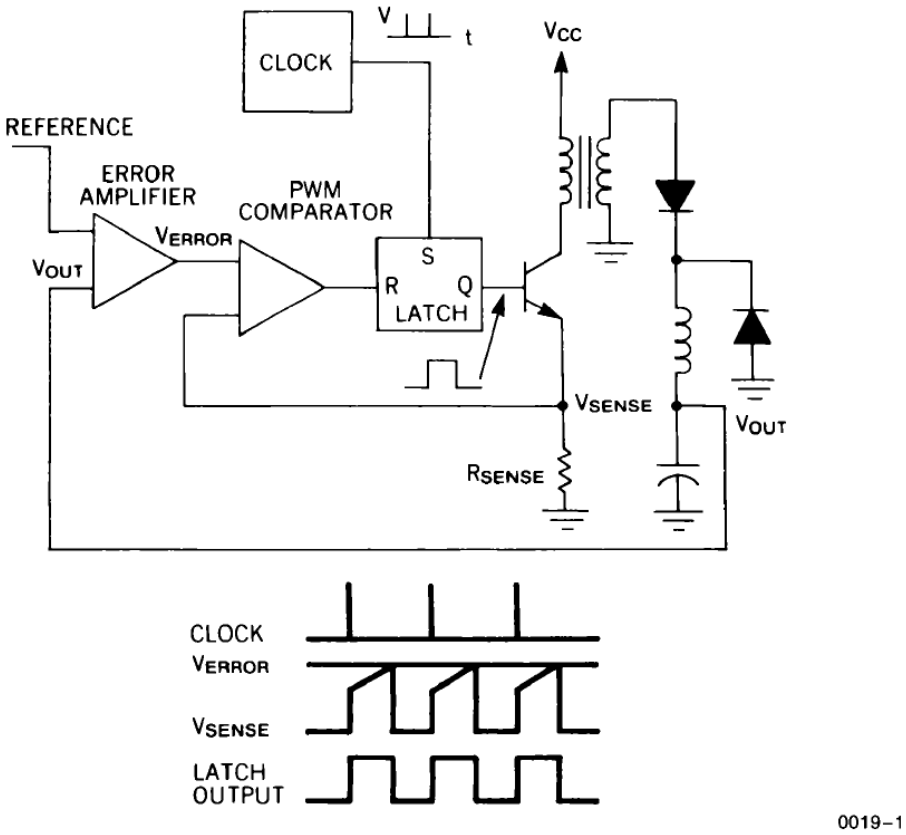


Figure 7-1. Two-Loop Current-Mode Control System

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the purposes of small signal analysis (see Figure 7-2). The two pole control to output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain bandwidth than would be possible with pulse-width control, giving the supply improved small signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as shown in Figure 7-3.

Capacitor C_i and resistor R_i, in Figure 7-3(A), add a low frequency zero, which cancels one of the two control to output poles of non-current mode converters. For large signal load changes, in which converter response is limited by inductor slew rate, the error amplifier saturates while the inductor is catching up with the load. During this time, C_i charges to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be long. However, the compensation network of Figure 7-3(B) can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Current limiting is greatly simplified with current mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

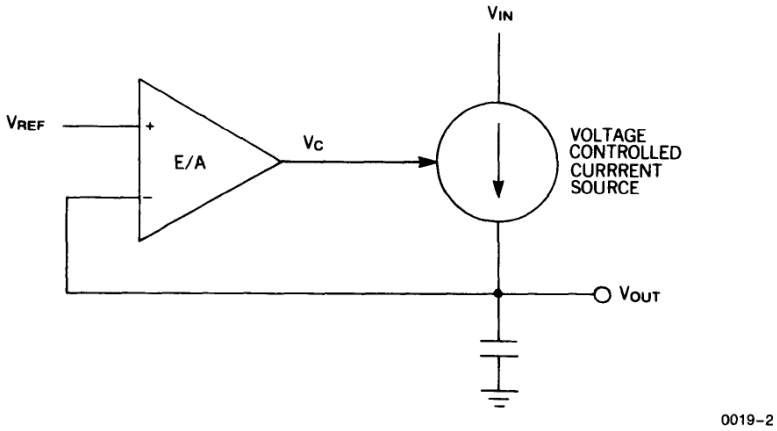
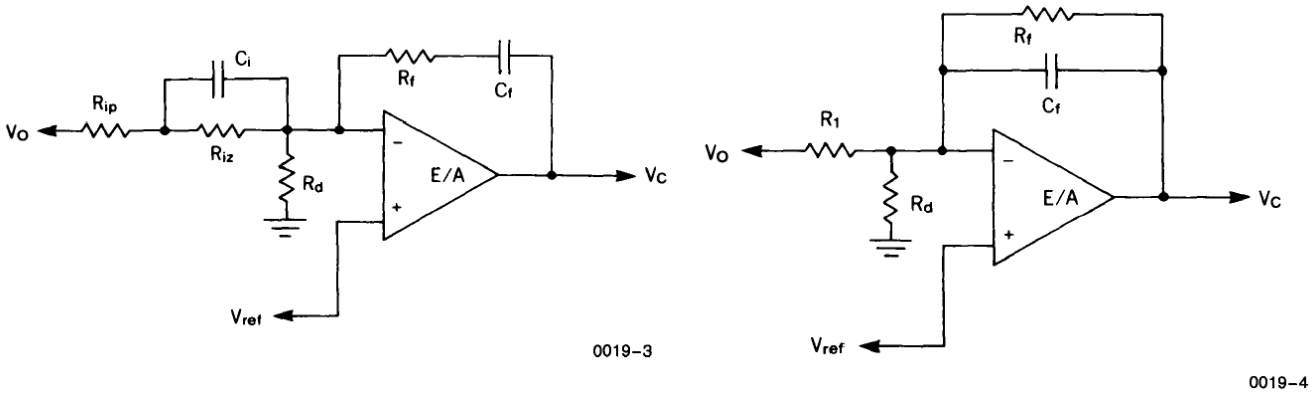


Figure 7-2. Inductor Looks Like a Current Source to Small Signals



A. Direct duty cycle control

B. Current mode control

Figure 7-3. Required Error Amplifier Compensation for Continuous Inductor Current Designs

7.3.1 UVLO

The UVLO circuit ensures that V_{CC} is adequate to make the UC1843B-SP fully operational before enabling the output stage. Figure 7-4 shows that the UVLO turnon and turnoff thresholds are fixed internally at 8.4 V and 7.6 V, respectively. The 0.6-V hysteresis prevents V_{CC} oscillations during power sequencing.

Figure 7-5 shows supply current requirements. Start-up current is < 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as shown in Figure 7-6. During normal circuit operation, V_{CC} is developed from auxiliary winding, W_{Aux}, with D_1 and C_{IN}. However, at start-up, C_{IN} must be charged to 8.4 V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when V_{AC} = 90-V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130-V RMS) conditions.

During UVLO, the output driver is in a low state. While it does not exhibit the same saturation characteristics as normal operation, it can easily sink 1 mA, enough to ensure the MOSFET is held off. For efficient operations, an LDO can take the place of R_{IN} and be disabled during the operation of the device.

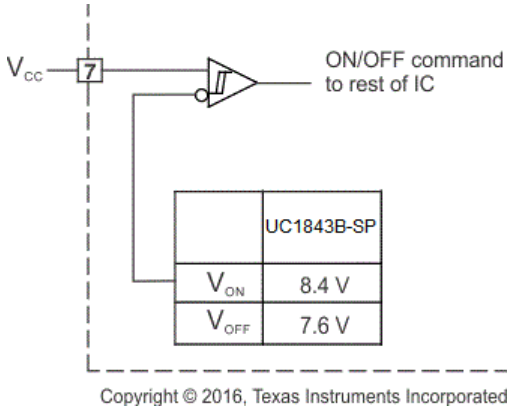
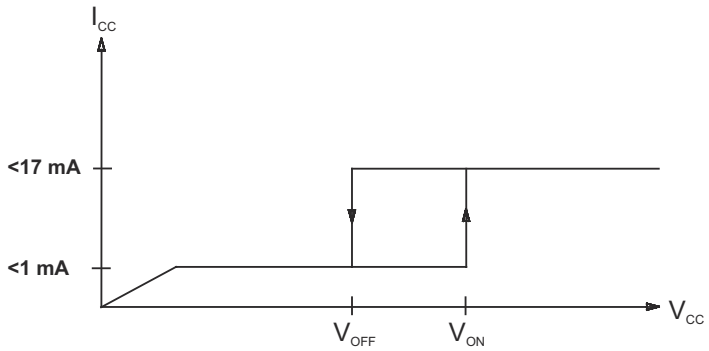


Figure 7-4. UVLO Turnon and Turnoff Threshold



During UVLO, the output driver is biased to sink minor amounts of current.

Figure 7-5. Supply Current Requirements

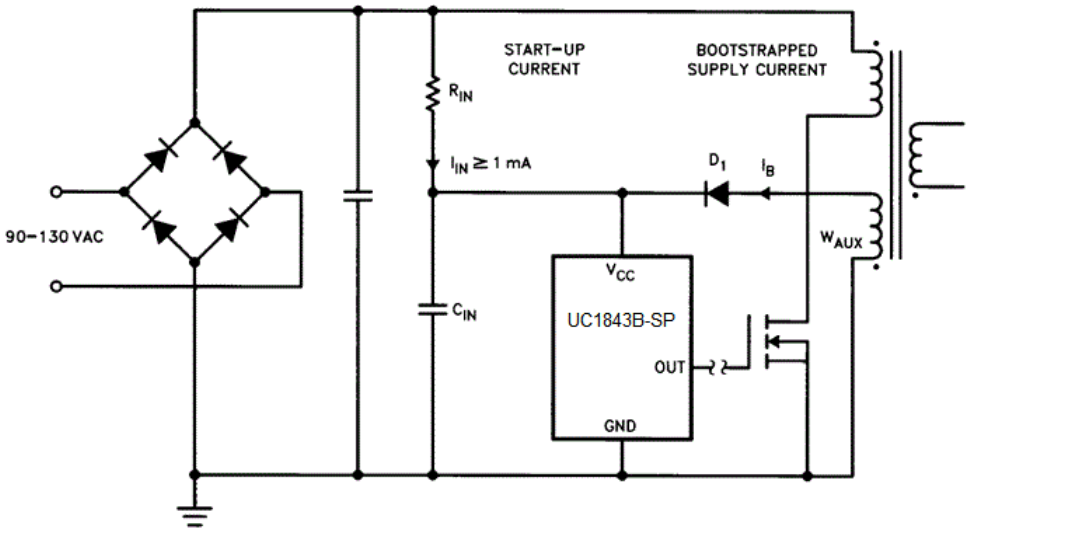


Figure 7-6. Providing Power to the UC1843B-SP

7.3.2 Reference

As highlighted in Section 7.2, UC1843B-SP incorporates a 5-V internal reference regulator with ±2% set point variation over temperature.

7.3.3 Totem-Pole Output

The UC1843B-SP PWM has a single totem-pole output which can be operated to ±1-A peak for driving MOSFET gates, and a 200-mA average current for bipolar power U-100A transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30 V is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance. Adding resistance will increase the switching losses of the converter, but will often reducing ringing and switching noise.

The use of a Schottky diode from the PWM output to ground prevents the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3 V at 200 mA. Most 1- to 3-A Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible enhances circuit performance. Implementation of the complete drive scheme is shown in Figure 7-7 through Figure 7-9. Transformer-driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figure 7-7 through Figure 7-9 show suggested circuits for driving MOSFETs and bipolar transistors with the UC1843B-SP output. The simple circuit of Figure 7-7 can be used when the control IC is not electrically isolated from the MOSFET turnon and turnoff to ±1 A. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode, D_1, prevents the output of the IC from going far below ground during turnoff.

Figure 7-8 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 7-9. Resistors R_1 and R_2 fix the on-state base current while capacitor C_I provides a negative base current pulse to remove stored charge at turnoff.

Because the UC1843B-SP series has only a single output, an interface circuit is needed to control push-pull, half-bridge, or full-bridge topologies. The UC1706 dual output driver with internal toggle flip-flop performs this function. Section 8.2 shows a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC1705/7-SP driver ICs.

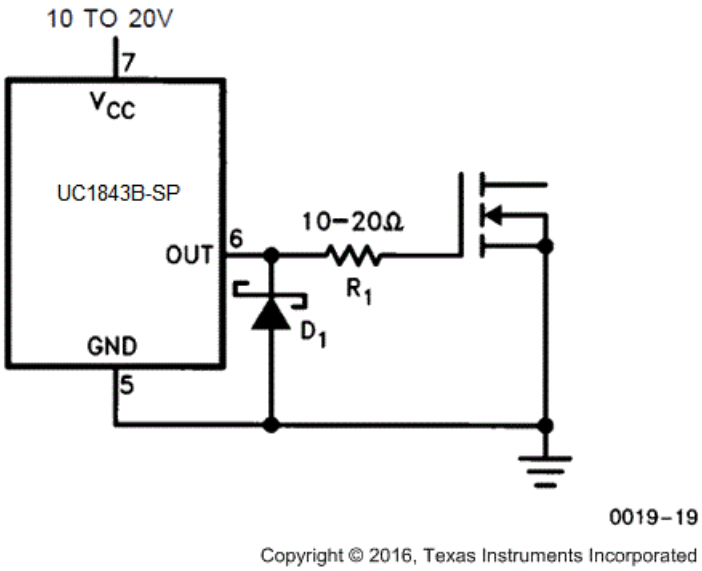


Figure 7-7. Direct MOSFET Drive

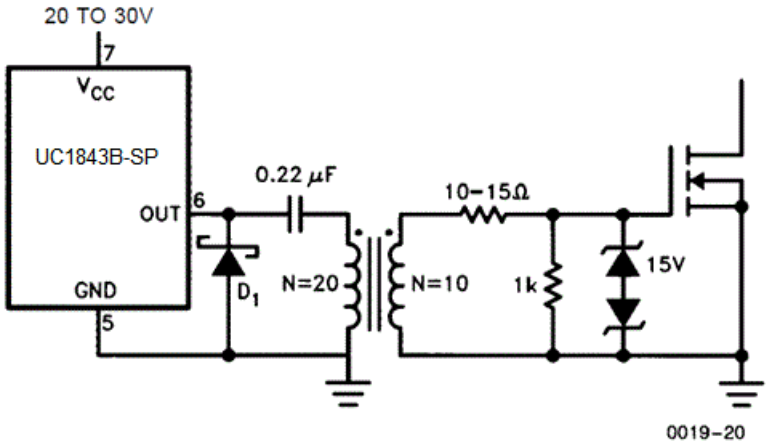


Figure 7-8. Isolated MOSFET Drive

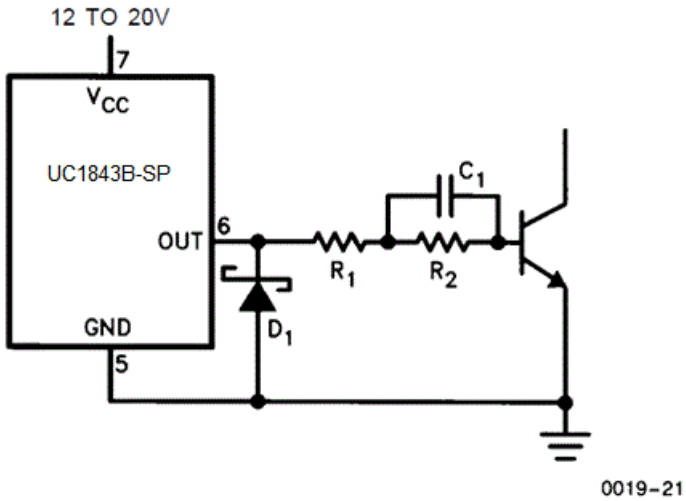


Figure 7-9. Bipolar Drive With Negative Turnoff Bias

7.4 Device Functional Modes

The UC1843B-SP uses fixed frequency, peak current mode control. An internal oscillator initiates the turnon of the driver to high-side power switch. The external power switch current is sensed through an external resistor and is compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors, as shown in Section 7.2. When the sensed current reaches the stepped down COMP voltage, the high-side power switch is turned off.

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

UC1843B-SP can be used as a controller to design various topologies such as buck, boost, flyback, and forward. Using an external interphase circuit can also support push-pull, half-bridge, and full-bridge topologies.

8.2 Typical Application

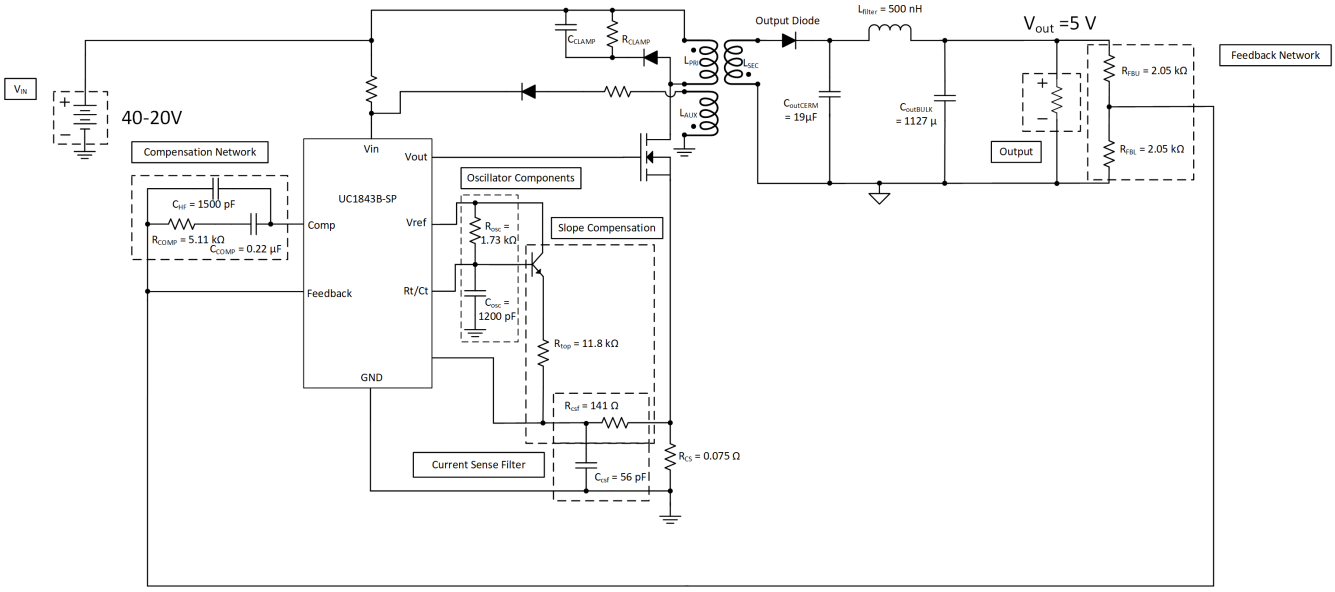


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

See Table 8-1 for parameter values.

Table 8-1. Design Parameters

PARAMETER	SPECIFICATIONS
Input Power Supply	20 to 40 VDC
Output Voltage	5 VDC
Output Current	0 to 10 A
Output Current Pre-load	100 mA
Operating Temperature	25°C
Switching Frequency of UC1843B-SP	200 kHz
Peak Input Current Limit	12 A
Bandwidth	~4 kHz
Phase Margin	~80°

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

Choosing a switching frequency has a trade off between efficiency and bandwidth. Higher switching frequencies will have larger bandwidth, but a lower efficiency than lower switching frequencies. A switching frequency of 200 kHz was chosen as a trade off between bandwidth and efficiency. Using Equation 1, R_T and C_T were chosen to be 7.15 kΩ and 1200 pF, respectively.

$$f_{osc} \approx \frac{1.72}{R_{osc} \times C_{osc}} \tag{1}$$

$$f_{osc} \approx \frac{1.72}{7.15\ \text{k}\Omega \times 1200\ \text{pF}} = 200\ \text{kHz} \tag{2}$$

8.2.2.2 Transformer

The transformer of the design consists of two major values, turns ratio and primary side inductance. There is no minimum limit to the turns ratio of the transformer, just a maximum limit. The equation below will give the turns ratio as a function of duty cycle, which if you put in the maximum duty cycle of the converter will give you a maximum turns ratio. The UC1843B-SP design targeted a duty cycle of 50%, which is somewhat low for this controller. The suggested value would be around 70% duty cycle to take advantage of the fact the UC1843B-SP has full duty cycle range. The equation of the turns ratio of the transformer is Equation 3.

$$N_{psMAX} = \frac{V_{inMIN} \times D_{lim}}{(V_{out} + V_{Diode}) \times (1 - D_{lim})} \tag{3}$$

$$N_{psMAX} = \frac{20\ \text{V} \times 0.5}{(5\ \text{V} + 0.7\ \text{V}) \times (1 - 0.5)} = 3.5 \tag{4}$$

Often the turns ratio will slightly change in design due to how the transformer is manufactured. For the UC1843B-SP design a turns ratio of 3.33 was used. Another turns ratio that is important is the turns ratio of the auxiliary winding. The auxiliary winding is found by figuring out what positive voltage is needed from the auxiliary winding. Picking what voltage the auxiliary winding should have lets one pick the turns ratio from the secondary to the auxiliary winding, which in turn allows for the turns ratio from primary to auxiliary to be found. The equation for the turns ratio for the auxiliary winding is Equation 5.

$$N_{pa} = \frac{N_{ps} \times (V_{out} + V_{Diode})}{V_{aux}} \tag{5}$$

$$N_{pa} = \frac{3.33 \times (5\ \text{V} + 0.7\ \text{V})}{13\ \text{V}} = 1.46 \tag{6}$$

An auxiliary winding of 1.43 was used for the UC1843B-SP design due to manufacturing constraints. The primary inductance of the transformer is found from picking an appropriate ripple current. A higher inductance will often mean reduced current ripple, thus lower EMI and noise, but a higher inductance will also increase physical size and limit the bandwidth of the design. A lower inductance will do the opposite, increasing current ripple, lowering EMI, lowering noise, decreasing physical size, and increasing the limited bandwidth of the design. The percent ripple current can be anywhere from 20% to 80% depending on the design. The equation for finding the primary inductance from the percentage ripple current is Equation 7.

$$L_{PRI} = \frac{V_{inMAX}^2 \times D_{MIN}^2}{V_{out} \times I_{out} \times f_{osc} \times \%_{Ripple}} \quad (7)$$

$$\frac{(40\ V)^2 \times 0.25^2}{5\ V \times 10\ A \times 200\ kHz \times 0.4} = 25\ \mu H \quad (8)$$

There are quite a few physical limitations when making transformers, so often this inductance will change slightly. For the UC1843B-SP design a primary inductance of 21 µH. This corresponds to a percent ripple of around 0.475. The peak and primary currents of the transformer are also generally useful for figuring out the physical structure of the transformer. See the following equations for proper calculations.

$$I_{Ripple} = \frac{V_{out} \times I_{out} \times \%_{Ripple}}{V_{inMAX} \times D_{MIN}} \quad (9)$$

$$I_{Ripple} = \frac{5\ V \times 10\ A \times 0.475}{40\ V \times 0.25} = 2.375\ A \quad (10)$$

$$I_{PriPeak} = \frac{V_{out} \times I_{out}}{V_{inMIN} \times D_{MAX} \times \eta} + \frac{I_{Ripple}}{2} \quad (11)$$

$$I_{PriPeak} = \frac{5\ V \times 10\ A}{20\ V \times 0.5 \times 0.8} + \frac{2.375}{2} = 7.44\ A \quad (12)$$

$$I_{PriRMS} = D \times \left(\frac{V_{out} \times I_{out}}{V_{in} \times D}\right)^2 + \frac{I_{Ripple}^2}{3} \quad (13)$$

$$I_{PriRMS} = 0.5 \times \left(\frac{5\ V \times 10\ A}{20\ V \times 0.5}\right)^2 + \frac{(2.375\ A)^2}{3} = 3.79\ A \quad (14)$$

$$I_{SecRMS} = (1 - D) \times I_{out}^2 + \frac{(I_{Ripple} \times N_{ps})^2}{3} \quad (15)$$

$$I_{SecRMS} = 0.5 \times (10\ A)^2 + \frac{(2.375\ A \times 3.33)^2}{3} = 8.42\ A \quad (16)$$

8.2.2.3 RCD Diode Clamp

For the UC1843B-SP design a resistor and capacitor are used. The resistor and capacitor is generally a value that is found through testing, but starting values can be obtained. To figure out the resistor and capacitor needed for the RCD clamp, one must first pick how much the node is allowed to overshoot. The equation for finding the voltage of the clamp is Equation 17.

$$V_{clamp} = K_{clamp} \times N_{ps} \times (V_{out} + V_{Diode}) \quad (17)$$

Note that K_{clamp} is recommended to be 1.5 as this will allow for only around 50% overshoot. Knowing the parasitic inductance of the transformer and how much the snubber voltage is allowed to change over the switching cycle, can allow one to figuring out starting values for the resistor and capacitor using Equation 18 and Equation 19.

$$R_{clamp} = \frac{V_{clamp}^2}{\frac{1}{2} \times L_{leakage} \times I_{PriPeak}^2 \times \frac{V_{clamp}}{V_{clamp} - N_{ps} \times (V_{out} + V_{Diode})} \times f_{osc}} \quad (18)$$

$$C_{clamp} = \frac{V_{clamp}}{\Delta V_{clamp} \times V_{clamp} \times R_{clamp} \times f_{osc}} \quad (19)$$

A starting value of 10% is generally used for ΔV_{clamp}.

8.2.2.4 Output Diode

The voltage stress by the converter on the diode can be found with Equation 20.

$$V_{DiodeStress} = V_{out} + \frac{V_{inMAX}}{N_{ps}} \quad (20)$$

$$V_{DiodeStress} = 5 \text{ V} + \frac{40 \text{ V}}{3.33} = 17 \text{ V} \quad (21)$$

Note that any diode picked should have a voltage rating of well above this value as it does not include parasitic spikes in the equation. The UC1843B-SP diode was picked to have a voltage rating of 60 V.

8.2.2.5 Output Filter and Capacitor

The output capacitance value is picked such that there is enough capacitance for the required voltage ripple and output current load step. The UC1843B-SP design uses equations Equation 22 and Equation 24 to find a minimum capacitance.

$$C_{out} > \frac{I_{out} \times D_{MAX}}{V_{Ripple} \times f_{osc}} \quad (22)$$

$$C_{out} > \frac{10 \text{ A} \times 0.5}{50 \text{ mV} \times 200 \text{ kHz}} = 500 \text{ µF} \quad (23)$$

$$C_{out} > \frac{\Delta I_{step}}{2\pi \times \Delta V_{out} \times f_{co}} \quad (24)$$

$$C_{out} > \frac{10 \text{ A}}{2\pi \times 0.7 \text{ V} \times 2.2 \text{ kHz}} = 1 \text{ mF} \quad (25)$$

A value of around 1145 µF was chosen to keep output voltage ripple low. Note that the output voltage ripple in the design was further decreased by adding an output filter and by adding an inductor after a small portion of the output capacitance. Six ceramic capacitors were picked to be placed before the output filter and then the large tantalum capacitors with some small ceramics were added to be part of the output filter. The initial ceramics will help with the initial current ripple, but have a very large output voltage ripple. This voltage ripple will be attenuated by the inductor and capacitor combination placed between the ceramic capacitors and the output. The equations below allow for finding the amount of attenuation that will come from a specific output filter inductance. An inductance of 500 nH was chosen to attenuate the output voltage ripple and the attenuation was sufficient for the design.

$$F_{resonant} = \frac{1}{2\pi \times L_{Filter} \times C_{oBulk}} \quad (26)$$

$$F_{resonant} = \frac{1}{2\pi \times 0.5\ nH \times 1127\ \mu F} = 6.7\ kHz \quad (27)$$

$$F_{Zero} = \frac{1}{2\pi \times C_{oBulk} \times ESR_{oBulk}} \quad (28)$$

$$F_{Zero} = \frac{1}{2\pi \times 1127\ \mu F \times 0.009\ \Omega} = 15.69\ kHz \quad (29)$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{f_{osc}}{f_{resonant}}\right) - 20 \times \log_{10}\left(\frac{f_{osc}}{f_{zero}}\right) \quad (30)$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{200\ kHz}{6.7\ kHz}\right) - 20 \times \log_{10}\left(\frac{200\ kHz}{15.69\ kHz}\right) = 36.88\ dB \quad (31)$$

Sometimes the output filter can cause peaking at high frequencies, this can be damped by adding a resistor in parallel with the inductor. For the UC1843B-SP design, 0.5 Ω was used as a very conservative value. The resistance needed to damp the peaking can be calculated using the following equations:

$$\omega_o = \frac{2(C_{oCerm} + C_{oBulk})}{L_{Filter} \times C_{oCerm} \times C_{oBulk}} \quad (32)$$

$$\omega_o = \frac{2(19\ \mu F + 1127\ \mu F)}{500\ nH \times 19\ \mu F \times 1127\ \mu F} = 463\ kHz \quad (33)$$

$$R_{Filter} = \frac{R_o \times L_{Filter} \times (C_{oCerm} + C_{oBulk}) - \frac{L_{Filter}}{\omega_o}}{\frac{R_o \times (C_{oCerm} + C_{oBulk})}{\omega_o} - L_{Filter} \times C_{oCerm}} \quad (34)$$

$$R_{Filter} = \frac{0.5 \times 500\ nH \times (19\ \mu F + 1127\ \mu F) - \frac{500\ nH}{463\ kHz}}{\frac{0.5 \times (19\ \mu F + 1127\ \mu F)}{463\ kHz} - 500\ nH \times 19\ \mu F} = 0.232\ \Omega \quad (35)$$

8.2.2.6 Compensation

The poles and zeros of a flyback converter can be found with the following equations:

$$f_{ESR} = \frac{1 + D}{2\pi \times C_{out} \times R_{ESR}} \quad (36)$$

$$f_{ESR} = \frac{1 + 0.5}{2\pi \times 1146\ \mu F \times 0.009\ \Omega} = 23.15\ kHz \quad (37)$$

$$f_P = \frac{1}{2\pi \times C_{out} \times R_o} \quad (38)$$

$$f_P = \frac{1}{2\pi \times 1146\ \mu F \times 0.5} = 278\ Hz \quad (39)$$

$$f_{RHPZ} = \frac{R_{out} \times (1 - D_{MAX})^2}{2\pi \times \frac{L_{PRI}}{N_{ps}^2} \times D_{MAX}} \quad (40)$$

$$f_{RHPZ} = \frac{0.5 \times (1 - 0.5)^2}{2\pi \times \frac{21\ \mu H}{3.33^2} \times 0.5} = 21\ kHz \quad (41)$$

$$f_{Compensation\ Zero} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} = \frac{1}{2\pi \times 5.11\ k\Omega \times 0.22\ \mu F} = 142\ Hz \quad (42)$$

$$f_{Compensation\ Pole} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} = \frac{1}{2\pi \times 5.11\ k\Omega \times 1500\ pF} = 20.76\ kHz \quad (43)$$

Type IIB compensation was selected to compensate the poles and zeros of the flyback converter for the design. Since the right half plane zero (RHPZ) of the flyback converter is unable to be compensated, the crossover frequency of the converter should be between one fourth to a whole decade below the RHPZ of the converter. Type IIB compensation has 1 pole and 1 zero to help compensate the converter. The pole from the compensation is suggested to be placed by the RHPZ of the converter and the zero from compensation is suggested to be placed a decade before the expected crossover frequency. Using these guidelines the compensation values for the converter were picked for the converter. For the non-isolated portion of the board this means choosing the value of the compensation resistors and capacitors along these guidelines. Increasing or decreasing the gain of the design can be compensated for by dividing the resistor from compensation down and increasing the values of the capacitors by the same amount. This allows for the gain to be controlled in the system without changing the poles and zeros of the system. Optimization is needed for compensation values, and those values can be validated through testing.

8.2.2.7 Sense Resistor and Slope Compensation

The sense resistor is used to sense the ripple current from the transformer as well as shutdown the switching cycle if the peak current of the converter is allowed to get too high. The voltage threshold of the CS pin is around 1 V, thus the equation to find the sense resistor from the peak current is shown in Equation 44.

$$R_{cs} = \frac{V_{CS\ Threshold} - V_{Slope\ Comp\ Offset}}{I_{limit}} \quad (44)$$

$$R_{cs} = \frac{1\ V - 0.1\ V}{12\ A} = 0.075\ \Omega \quad (45)$$

Note that I_{limit} should be greater than $I_{PriPeak}$, and that the voltage offset from the slope compensation will be dependant on the amount of slope compensation in the design. The value of 0.075 Ω for the sense resistance was found to be the optimum value adding some headroom for slope compensation offset of 0.1 V. Slope compensation was implemented with a BJT being turned off and on by the RC pin of the device. The BJT was placed between the REF pin and a resistor divider to the CS pin. The optimum slope compensation value can be found from the following equations after picking a value for the top of the divider:

$$S_c = \frac{V_{out} \times R_{cs} \times G_{cs}}{L_{PRI} \times N_{ps}} \quad (46)$$

$$S_c = \frac{5 \text{ V} \times 0.075 \ \Omega \times 3}{21 \ \mu\text{H} \times 3.33} = 16088 \quad (47)$$

$$S_{osc} = \frac{f_{osc} \times V_{oscpp}}{D_{MIN}} \quad (48)$$

$$S_{osc} = \frac{200 \text{ kHz} \times 1.7 \text{ V}}{0.25} = 1360000 \quad (49)$$

$$R_{csf} = \frac{R_{top}}{\frac{S_{osc}}{S_c} - 1} \quad (50)$$

$$R_{csf} = \frac{11.8 \text{ k}\Omega}{\frac{1360000}{16088} - 1} = 141 \ \Omega \quad (51)$$

The UC1843B-SP design uses a much higher resistor of 1.47 kΩ, but this is an attempt to be very conservative. Note that the bottom resistor can be used as part of a filter to the CS pin as well, which is implemented in the design using a capacitor near the CS pin. Care was taken such that the RC filter would not filter the switching frequency by having the RC time constant be a decade less than the switching frequency.

8.2.3 Application Curves

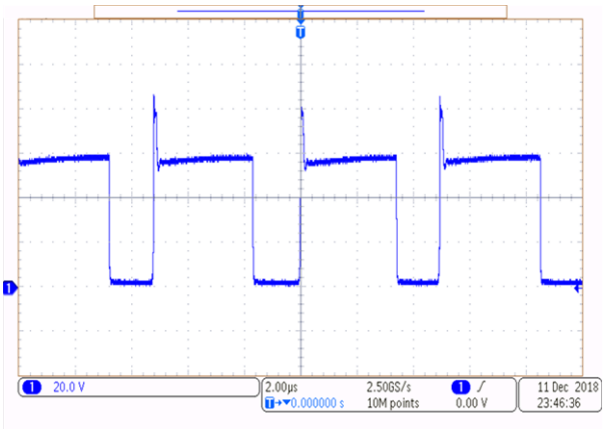


Figure 8-2. Switch Node of Flyback Converter

For the test in Figure 8-2, 40 V was applied to the input and 10 A was drawn from the output. Ringing can be present on the switching node if the converter is run in discontinuous conduction mode rather than the continuous conduction mode the design was run with.

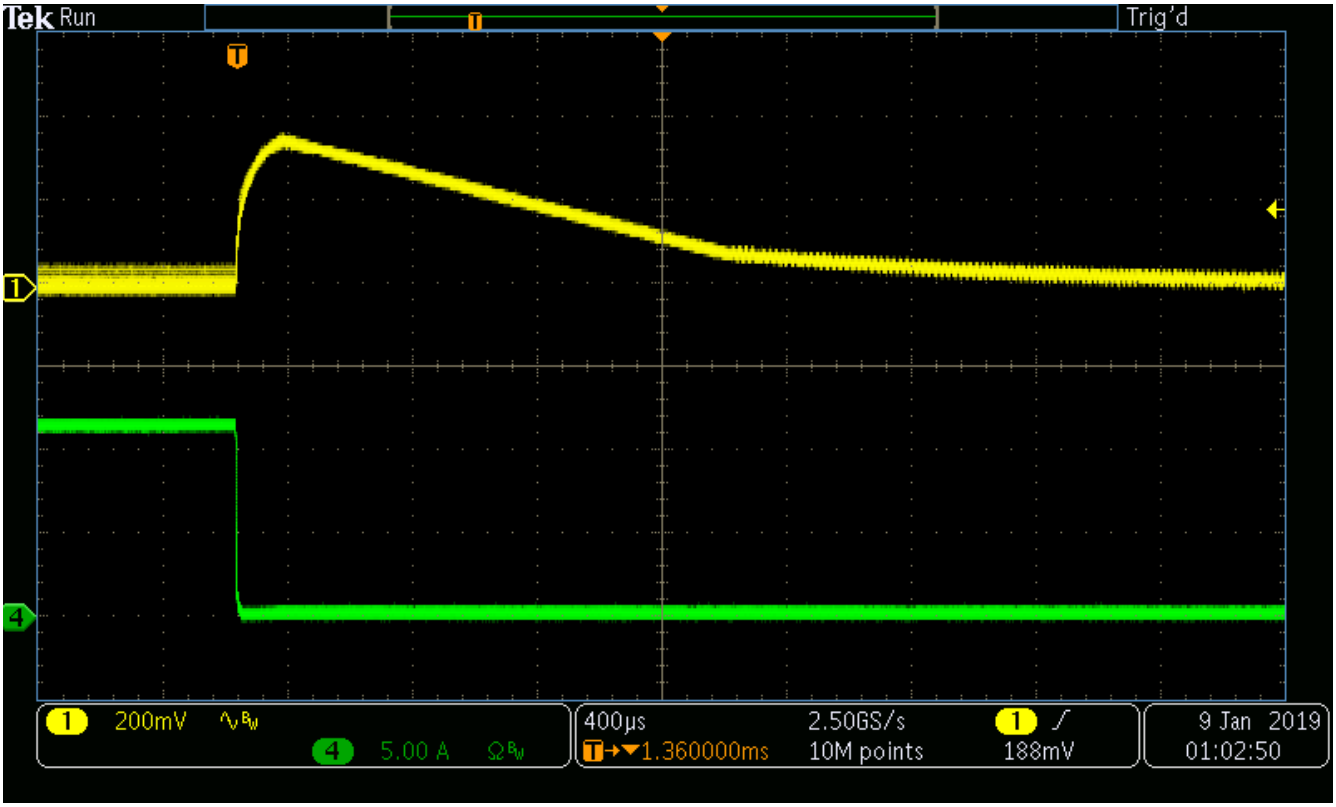


Figure 8-3. Load Step Down With 40 V_{IN}

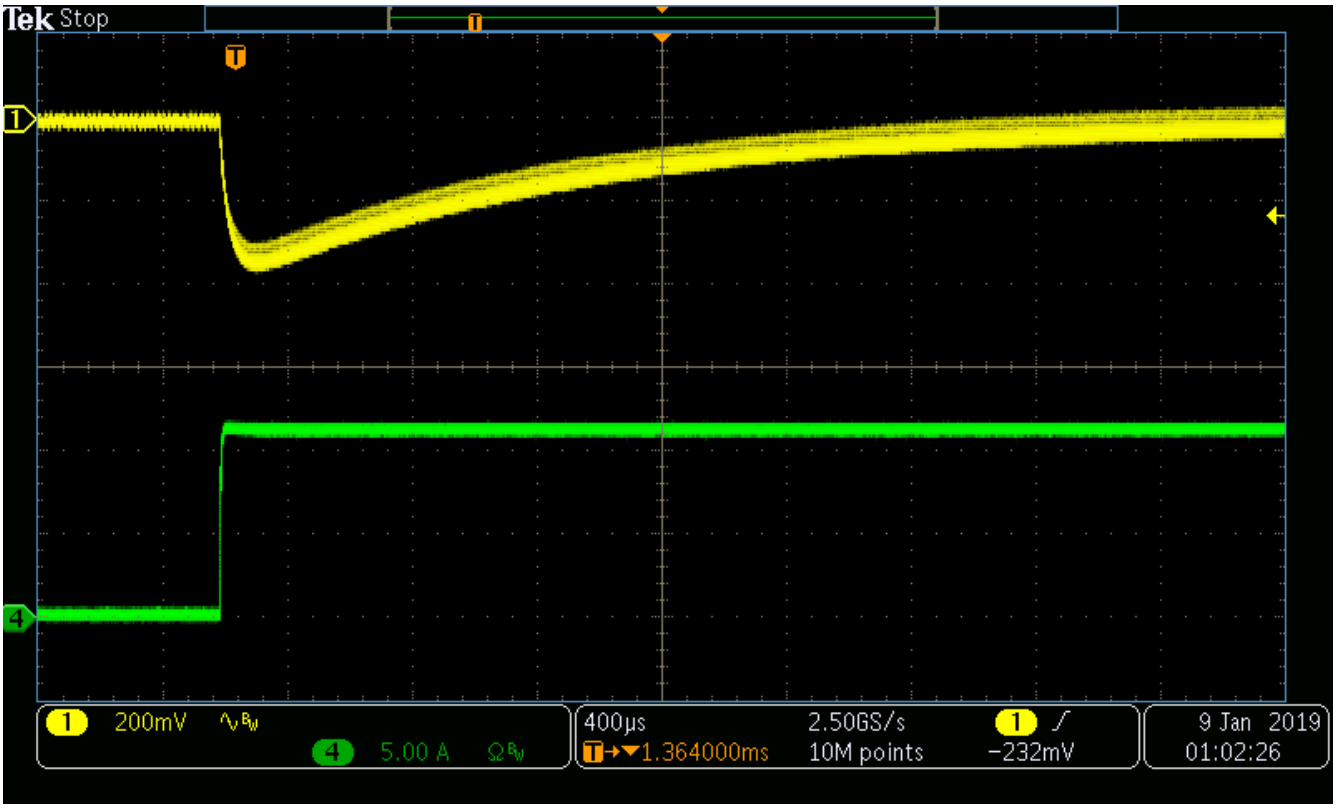


Figure 8-4. Load Step Up With 40 V_{IN}

For tests shown in and , 40 V was applied to the input and a load step was applied to the output. The load step applied was from 0 A to 10 A and 10 A to 0 A. Note that those currents do not include the 0.1-A pre-load. The curves show that the stability of the design due to the lack of ringing during the load step.

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 8 V and 32 V. This input supply should be well regulated. If the input supply is located more than a few inches from the UC1843B-SP converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 100 µF is a typical choice; however, this varies heavily on the start up circuitry of the device. This is because the input voltage to the device will decrease during start up and the input capacitance will have to provide enough charge to allow the UC1843B-SP to initially switch.

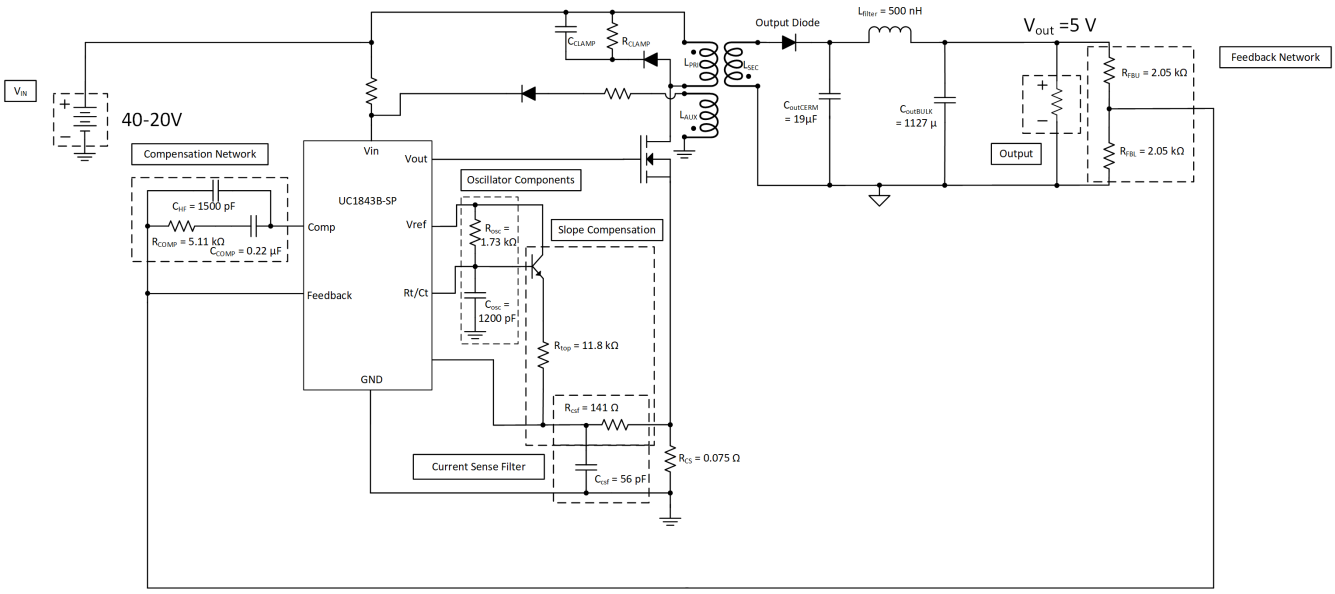


Figure 9-1. Flyback Regulator

10 Layout

10.1 Layout Guidelines

Always try to use a low EMI inductor with a ferrite closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a farther away from the low-power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

10.1.1 Feedback Traces

Try to run the feedback trace as far as possible from the inductor and noisy power traces. The designer should also make the feedback trace as direct as possible and somewhat thick. These two guidelines sometimes involve a trade-off, but keeping the trace away from inductor EMI and other noise sources is the more critical guideline. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

10.1.2 Input/Output Capacitors

When using a low-value ceramic input filter capacitor, locate it as close as possible to the V_{IN} pin of the IC. This eliminates as much trace inductance effects as possible and gives the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case, it should also be positioned as close as possible to the IC.

10.1.3 Compensation Components

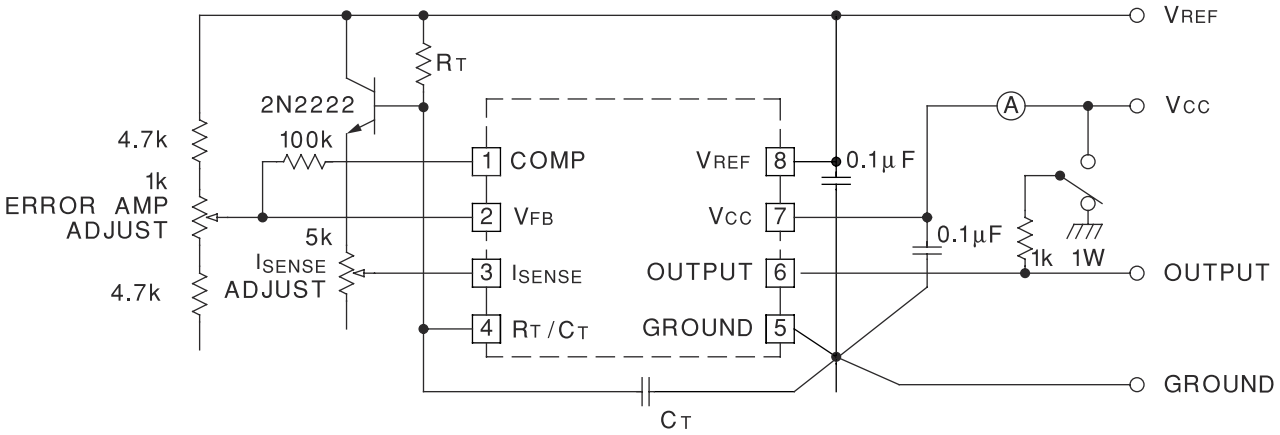
External compensation components for stability should also be placed close to the IC. TI recommends to also use surface mount components for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

10.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode should be as close as possible to each other. This helps reduce the EMI radiated by the power traces due to the high-switching currents through them. This also reduces lead inductance and resistance, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise by reducing ground loop errors and absorbing more of the EMI radiated by the inductor.

For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are located) and the signal plane (where the feedback and compensation and components are located) for improved performance. On multi-layer boards, vias are required to connect traces and different planes. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states: one state when the switch is on and one when the switch is off. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

10.2 Layout Example



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 10-1. Open-Loop Laboratory Test Fixture

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R8670412V9A	ACTIVE	XCEPT	KGD	0	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R8670412VYC	ACTIVE	CFP	HKU	10	1	RoHS-Exempt & Green	AU	N / A for Pkg Type	-55 to 125	R8670412VYC UC1843B-SP	Samples
UC1843BHKU/EM	ACTIVE	CFP	HKU	10	1	RoHS-Exempt & Green	AU	N / A for Pkg Type	25 to 25	UC1843BHKUM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

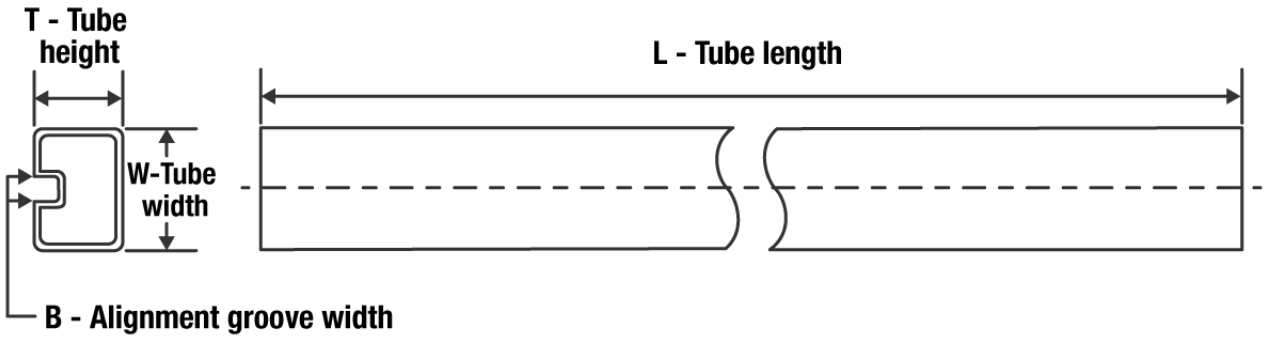
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

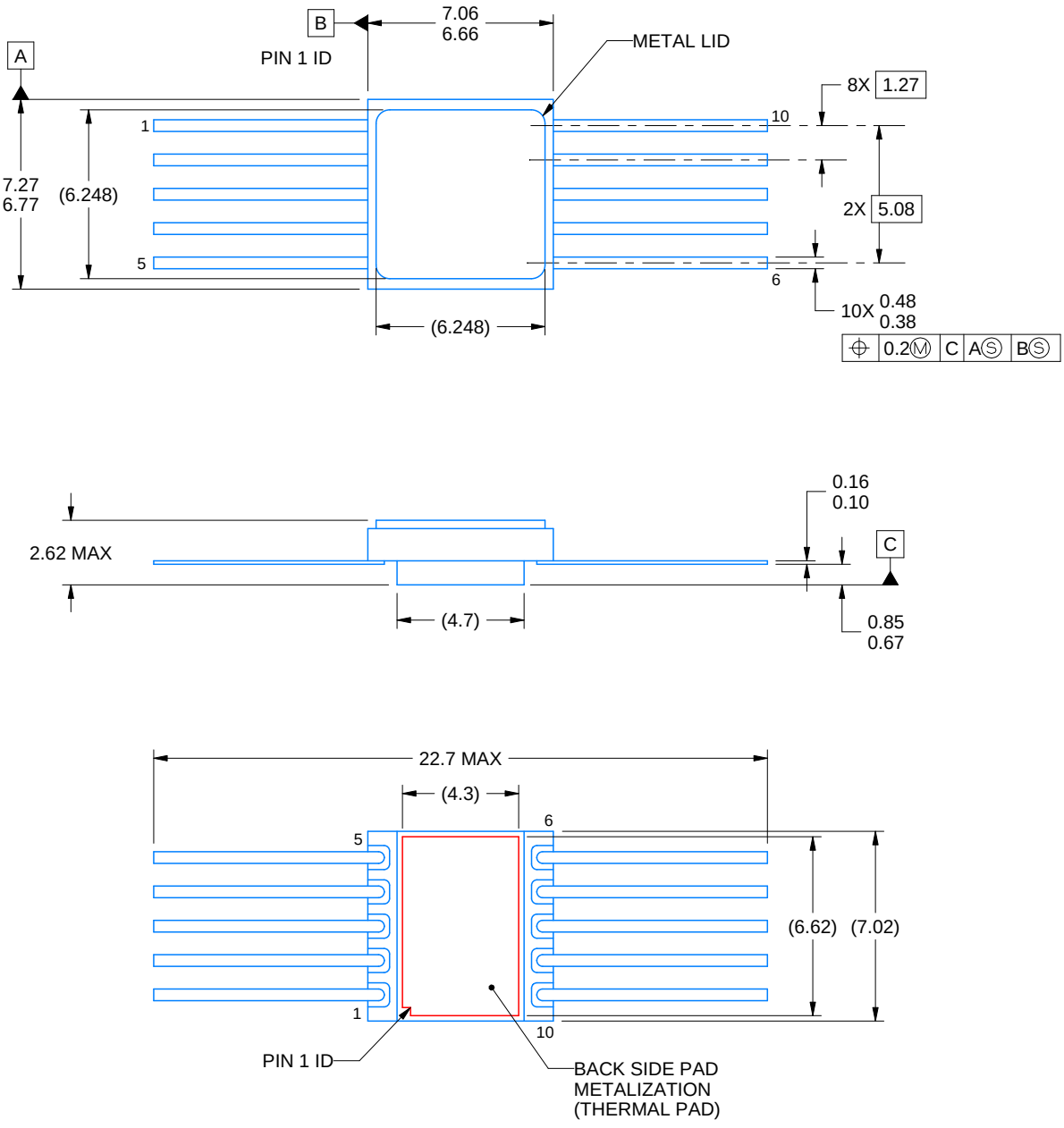
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R8670412VYC	HKU	CFP	10	1	506.98	26.16	6220	NA
UC1843BHKU/EM	HKU	CFP	10	1	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKU0010A

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK



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NOTES:

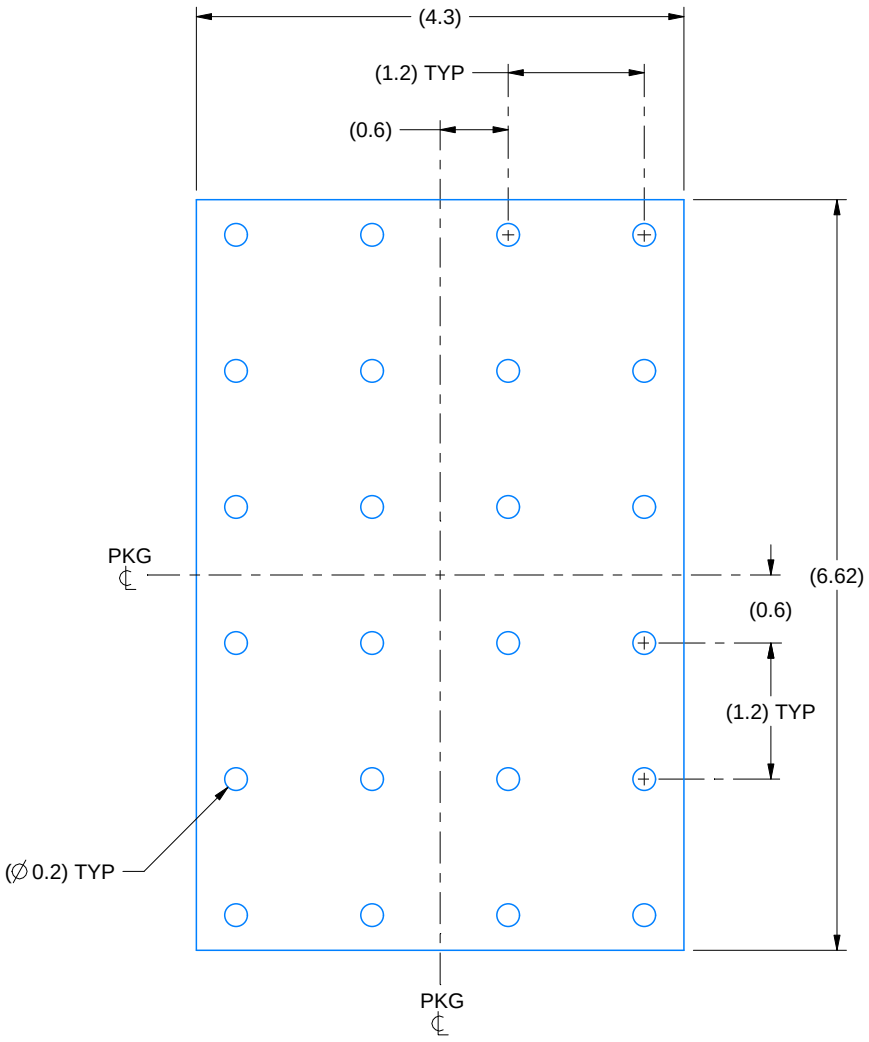
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.
5. This drawing does not comply with MIL STD 1835. Do not use this package for compliant product.
6. Metal lid is connected to back side pad metalization.

EXAMPLE BOARD LAYOUT

HKU0010A

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

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