TSU111H

Datasheet

High temperature (150 °C) and long mission profile automotive grade, high accuracy (250 µV) 5 V CMOS operational amplifier

TSU111HYLT
SOT23-5

Maturity status link
TSU111H

Related products	
TSU101, TSU102 and TSU104	For further power savings
TSZ121, TSZ122 and TSZ124	For increased accuracy

Features

- AEC-Q100 qualified
- Long mission profile
- High temperature qualified 150 °C
- Micro ampere current consumption: I_{CC} = 1.7 µA typ. at 25 °C
- Low offset voltage: 250 µV max. at 25 °C, 600 µV max. over full temperature range (-40 to 150 °C)
- Low noise over 0.1 to 10 Hz bandwidth: 3.9 µVpp
- Low supply voltage: 1.5 V to 5.5 V
- Rail-to-rail input and output
- Gain bandwidth product: 23 kHz typ.
- Low input bias current: 1 pA max. at 25 °C
- High tolerance to ESD: 4 kV HBM
- High accuracy without calibration
- Tolerance to power supply transient drops

Applications

- Battery management system: ultra-low power op amp detects when battery is charging/discharging and wakes up CPU
- Onboard chargers (OBC)
- Wireless chargers

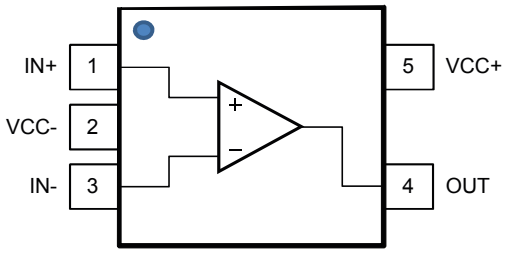
Description

The TSU111H operational amplifier (op amp) offers an ultralow power consumption of 1.7 µA typical and 2.4 µA maximum when supplied by 1.8 V.

The ultralow power consumption, the high accuracy of 250 µV max., and 23 kHz gain bandwidth make the TSU111H ideal for sensor signal conditioning, battery management systems, onboard (OBC) and wireless chargers.

1 Package pin connection

Figure 1. Pin connection (top view)



SOT23-5

Table 1. Pin description

Pin n°	Pin name	Description
1	IN+	Non-inverting input channel
2	VCC-	Negative supply voltage
3	IN-	Inverting input channel
4	OUT	Output channel
5	VCC+	Positive supply voltage

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (1)		± V_{CC}	
V_{in}	Input voltage (3)		(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	
I_{in}	Input current (4)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		160	
R_{thja}	Thermal resistance junction-to-ambient (5) (6)	SOT23-5	250	°C/W
ESD	HBM: human body model (7)		4000	V
	CDM: charged device model (8)		1500	

1. *All voltage values, except the differential voltage are with respect to the network ground terminal.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.*
3. *(V_{CC+})- V_{in} must not exceed 6 V, V_{in} - (V_{CC-}) must not exceed 6 V.*
4. *The input current must be limited by a resistor in-series with the inputs.*
5. *R_{th} are typical values.*
6. *Short-circuits can cause excessive heating and destructive dissipation.*
7. *Related to ESDA/JEDEC JS-001 Apr. 2010.*
8. *Related to JEDEC JESD22-C101-E Dec. 2009.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common-mode input voltage range	(V_{CC-}) to (V_{CC+}) + 0.1	
T_{oper}	Operating free-air temperature range	-40 to 150	°C

3 Electrical characteristics

Table 4. Electrical characteristics at (V_{CC+}) = 1.8 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			250	µV
		-40 °C < T < 150 °C			600	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 25 °C			6	µV/°C
		25 °C < T < 150 °C			3	
I_{io}	Input offset current (1)	T = 25 °C		1		pA
I_{ib}	Input bias current (1)	T = 25 °C		1		
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 1.8 V	T = 25 °C	74	102		dB
		-40 °C < T < 150 °C	67			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	95	126		
		R = 100 kΩ, -40 °C < T < 150 °C	82			
V_{OH}	High-level output voltage, (drop from V_{CC+}), V_{ID} = 200 mV	R_L = 10 kΩ, T = 25 °C		11	25	mV
		R = 10 kΩ, -40 °C < T < 150 °C			40	
V_{OL}	Low-level output voltage, V_{ID} = - 200 mV	R_L = 10 kΩ, T = 25 °C		9	25	
		R_L = 10 kΩ, -40 °C < T < 150 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC}, V_{ID} = - 200 mV	T = 25 °C	2.8	5		mA
		-40 °C < T < 150 °C	1.5			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	2	4		
		-40 °C < T < 150 °C	1.5			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		1.7	2.4	µA
		-40 °C < T < 150 °C			2.6	
		-40 °C < T < 125 °C			2.5	
AC performance						
GBP	Gain bandwidth product	R_L = 100 kΩ, C_L = 60 pF	10	23		kHz
Φ_m	Phase margin R_L = 1 MΩ, C_L = 60 pF	T = 25 °C		79		degrees
GM	Gain margin	R_L = 100 kΩ, C_L = 60 pF		24		dB
SRp	Slew rate (10 % to 90 %) R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	T = 25 °C	1.4	3.5		V/ms
		-40 °C < T < 150 °C	0.9			
SRn	Slew rate (10 % to 90 %) R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	T = 25 °C	2.2	5.5		V/ms
		-40 °C < T < 150 °C	1.1			
e_n	Equivalent input noise voltage	f = 100 Hz		200		nV/√Hz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_{n-pp}	Equivalent input noise voltage (Noise RTI)	0.1 to 10 Hz		3.9		µVpp
$trec_P$	Overload recovery time (from positive rail) Overload recovery time (from positive rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T < 150 °C		220		µs
$trec_N$	Overload recovery time (from negative rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T < 150 °C		300		
T_s	Settling time	1 V step, G = +1, 0.1%		645		
$T_{startup}$	Startup time (time between V_{supply} reaching min. operating and V_{io} final value)	G = 1, V_{in} = 0.2 V		1100		

1. *Guaranteed by design.*

Table 5. Electrical characteristics at (V_{CC+}) = 3.3 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC} / 2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		DC performance				
V_{io}	Input offset voltage	T = 25 °C			250	µV
		-40 °C < T < 150 °C			600	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 25 °C			6	µV/°C
		25 °C < T < 150 °C			3	
I_{io}	Input offset current (1)	T = 25 °C		1		pA
I_{ib}	Input bias current (1)	T = 25 °C		1		
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 3.3 V	T = 25 °C	78	105		dB
		-40 °C < T < 150 °C	73			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	100	134		
		R_L = 100 kΩ, -40 °C < T < 150 °C	88			
V_{OH}	High-level output voltage, (drop from V_{CC+}), V_{ID} = 200 mV	R_L = 10 kΩ, T = 25 °C		11	25	mV
		R_L = 10 kΩ, -40 °C < T < 150 °C			40	
V_{OL}	Low-level output voltage, V_{ID} = -200 mV	R_L = 10 kΩ, T = 25 °C		9	25	
		R_L = 10 kΩ, -40 °C < T < 150 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC}, V_{ID} = -200 mV	T = 25 °C	12	22		mA
		-40 °C < T < 150 °C	6			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	9	17		
		-40 °C < T < 150 °C	5			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		1.8	2.6	µA
		-40 °C < T < 150 °C			2.8	
		-40 °C < T < 125 °C			2.7	
		AC performance				
GBP	Gain bandwidth product	R_L = 100 kΩ, C_L = 60 pF	14	25		kHz
Φ_m	Phase margin			80		degrees
G_m	Gain margin			25		dB
SR_p	Slew rate (10 % to 90 %) R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	T = 25 °C	1.4	3.5		V/ms
		-40 °C < T < 150 °C	0.9			
SR_n	Slew rate (10 % to 90 %) R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	T = 25 °C	2.5	5.5		V/ms
		-40 °C < T < 150 °C	1.1			
T_s	Settling time	1 V step, G = +1, 0.1%		445		µs
e_n	Equivalent input noise voltage	f = 100 Hz		200		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		4.6		µVpp
t_{recP}	Overload recovery time (from positive rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T < 150 °C		400		µs
t_{recN}	Overload recovery time (from negative rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T < 150 °C		600		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{startup}$	Startup time (time between V_{supply} reaching min operating and V_{io} final value)	G = 1, V_{in} = 0.2 V		330		µs

1. *Guaranteed by design.*

Table 6. Electrical characteristics at (V_{CC+}) = 5 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC} /2 (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			250	µV
		-40 °C < T < 150 °C			600	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 25 °C			6	µV/°C
		25 °C < T < 150 °C			3	
I_{io}	Input offset current (1)	T = 25 °C		1		pA
I_{ib}	Input bias current (1)	T = 25 °C		1		
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$),$V_{icm}$ = 0 to 5 V	T = 25 °C	76	107		dB
		-40 °C < T < 150 °C	73			
SVR	Supply voltage rejection ratio, V_{CC} = 1.5 to 5.5 V, V_{icm} = 0 V	T = 25 °C	89	110		
		-40 °C < T < 150 °C	78			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	105	139		
		R_L = 100 kΩ, -40 °C < T < 150 °C	86			
V_{OH}	High-level output voltage, (drop from V_{CC+}), V_{ID} = 200 mV	R_L = 10 kΩ, T = 25 °C		12	25	mV
		RL= 10 kΩ, -40 °C < T < 150 °C			40	
V_{OL}	Low-level output voltage, V_{ID} = - 200 mV	R_L = 10 kΩ, T = 25 °C		7	25	
		RL= 10 kΩ, -40 °C < T < 150 °C			40	
I_{sink}	Output sink current, V_{out} = V_{CC}, V_{ID} = - 200 mV	T = 25 °C	30	45		mA
		-40 °C < T < 150 °C	15			
I_{source}	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	25	39		
		-40 °C < T < 150 °C	18			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		2	3	µA
		-40 °C < T < 150 °C			4.4	
		-40 °C < T < 125 °C			3.5	
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF	14	25		kHz
Φ_m	Phase margin			81		degrees
G_m	Gain margin			24		dB
SR_p	Slew rate (10 % to 90 %) R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	T = 25 °C	1.4	3.8		V/ms
		-40 °C < T < 150 °C	0.9			
SR_n	Slew rate (10 % to 90 %) R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	T = 25 °C	2.5	5.5		V/ms
		-40 °C < T < 150 °C	1.1			
T_s	Settling time	1 V step, G = +1, 0.1%		430		µs
e_n	Equivalent input noise voltage	f = 100 Hz		200		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		4.4		µVpp
t_{recP}	Overload recovery time (from positive rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, 25 °C		550		µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{recN}	Overload recovery time (from negative rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, 25 °C		900		µs
$T_{startup}$	Startup time (time between V_{supply} reaching min operating and V_{io} final value)	G = 1, V_{in} = 0.2 V		350		

1. *Guaranteed by design.*

4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage at low V_{icm}

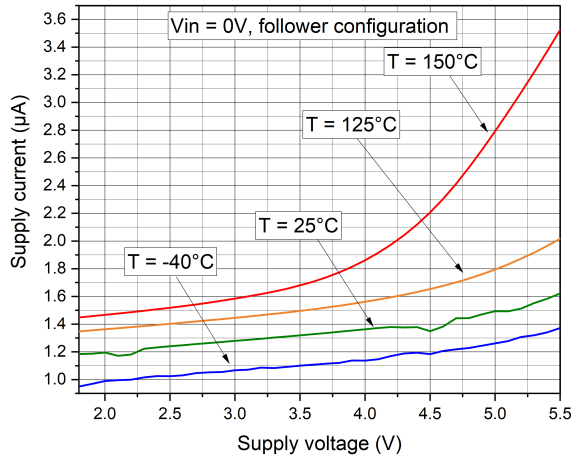


Figure 3. Supply current vs. supply voltage at high V_{icm}

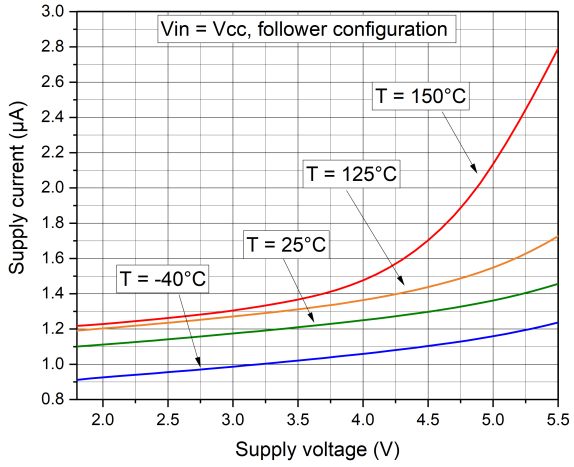


Figure 4. Supply current vs. supply voltage at mid V_{icm}

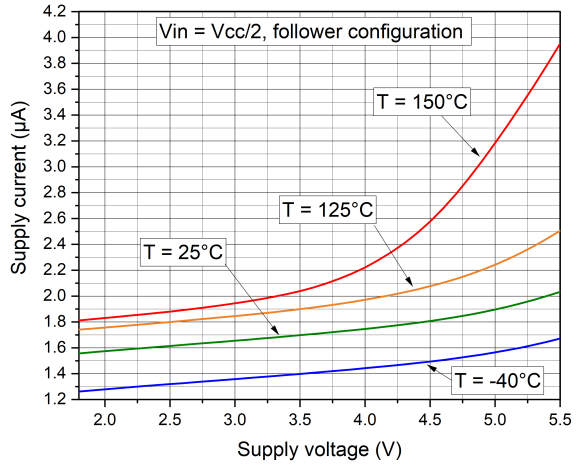


Figure 5. Supply current vs. common mode voltage at 1.8 V supply voltage

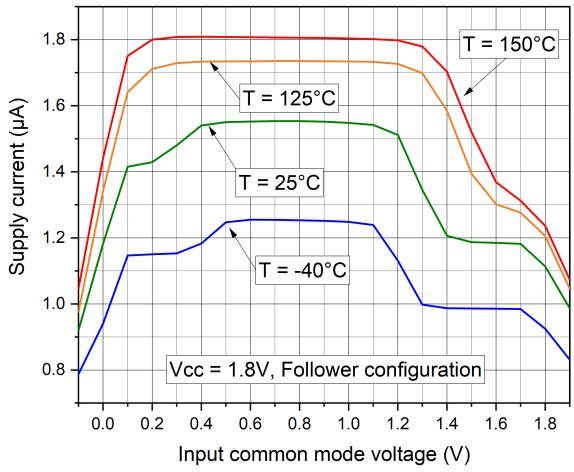


Figure 6. Supply current vs. common mode voltage at 3.3 V supply voltage

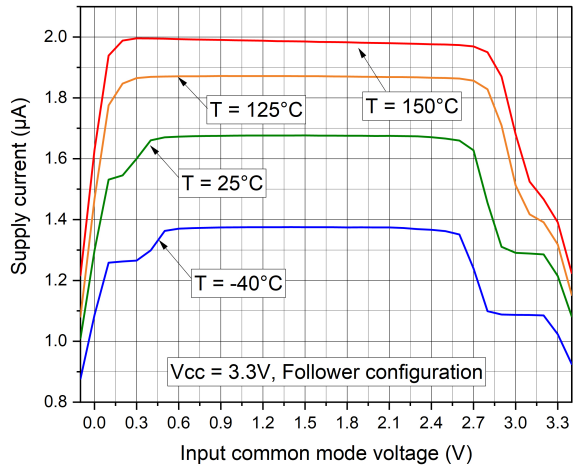


Figure 7. Supply current vs. common mode voltage at 5 V supply voltage

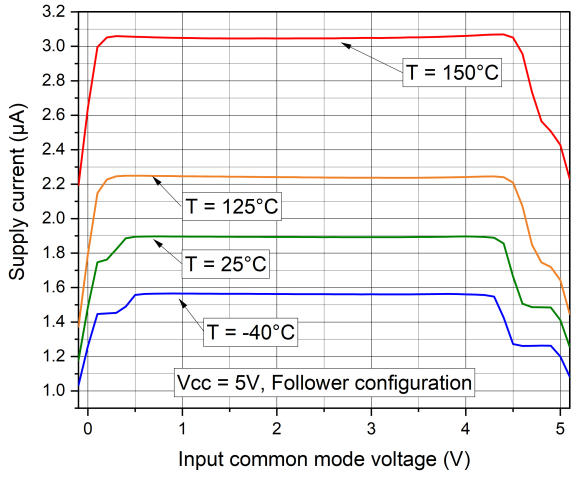


Figure 8. Input offset voltage vs. common mode voltage at 1.8 V supply voltage

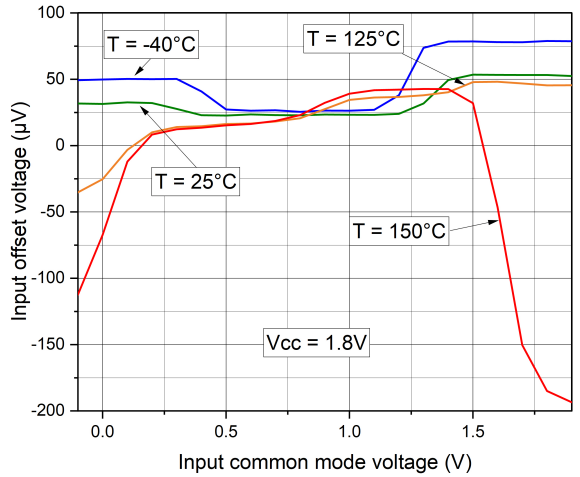


Figure 9. Input offset voltage vs. common mode voltage at 3.3 V supply voltage

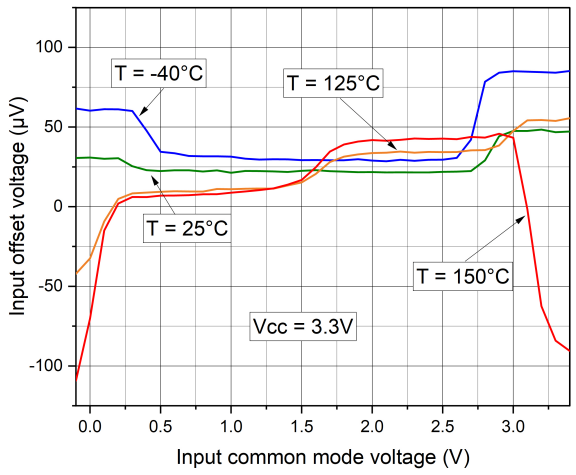


Figure 10. Input offset voltage vs. common mode voltage at 5 V supply voltage

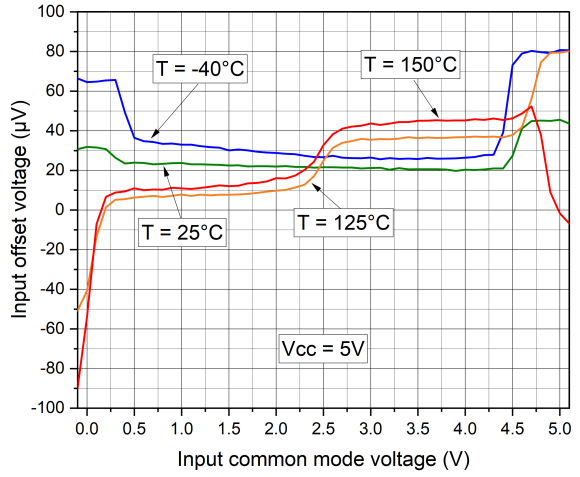


Figure 11. Input offset voltage vs. supply voltage at mid V_{icm}

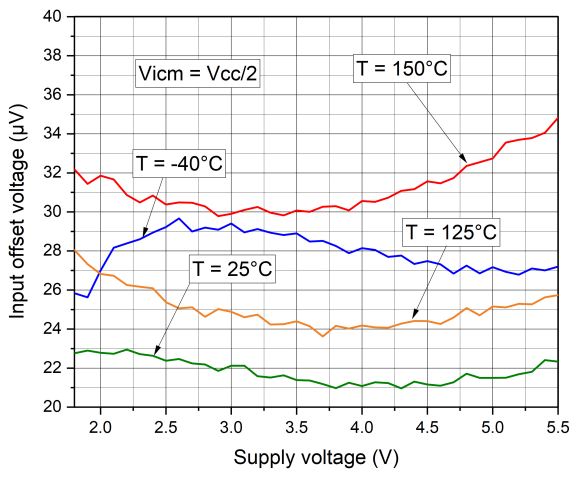


Figure 12. High level output voltage (drop from V_{cc+})

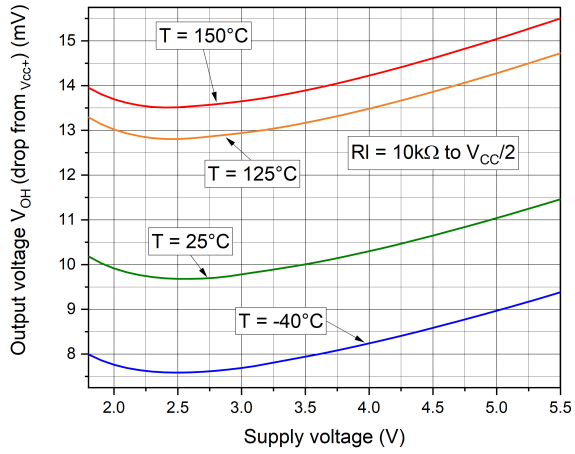


Figure 13. Low level output voltage

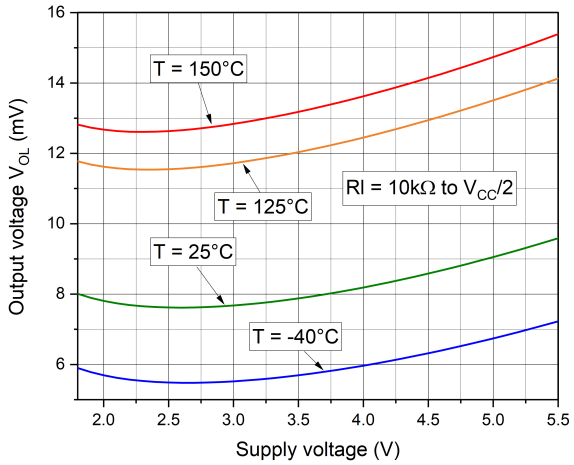


Figure 14. Output characteristics at 1.8 V supply voltage and mid V_{icm}

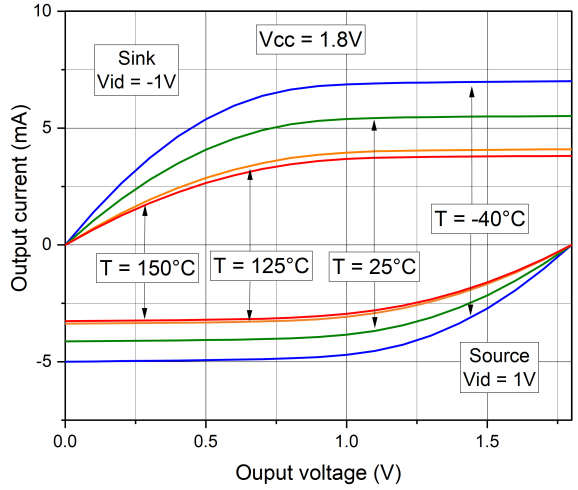


Figure 15. Output characteristics at 3.3 V supply voltage and mid V_{icm}

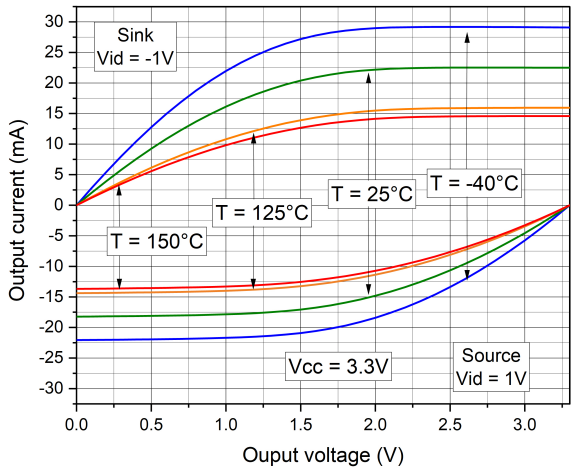


Figure 16. Output characteristics at 5 V supply voltage and mid V_{icm}

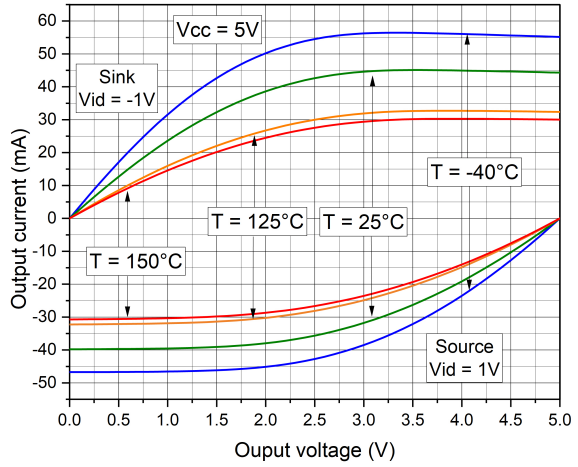


Figure 17. Output saturation with a sine wave on the input at F = 1 Hz

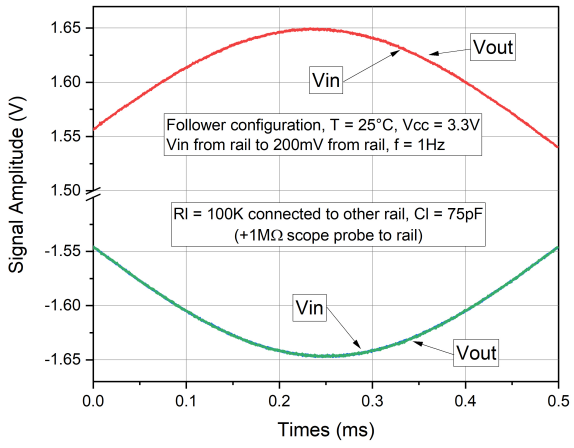


Figure 18. Output saturation with a sine wave on the input at F = 100 Hz

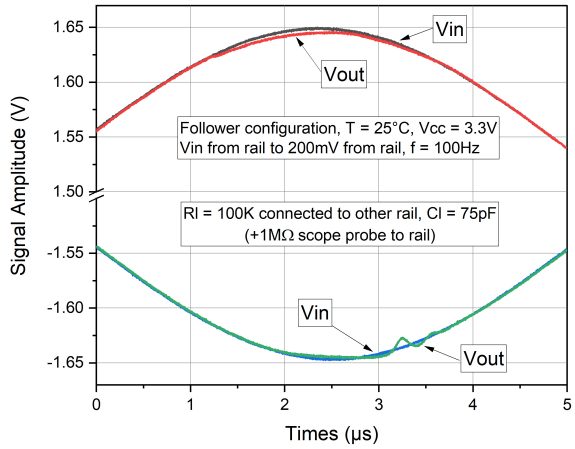


Figure 19. Output saturation with a sine wave on the input at F = 500 Hz

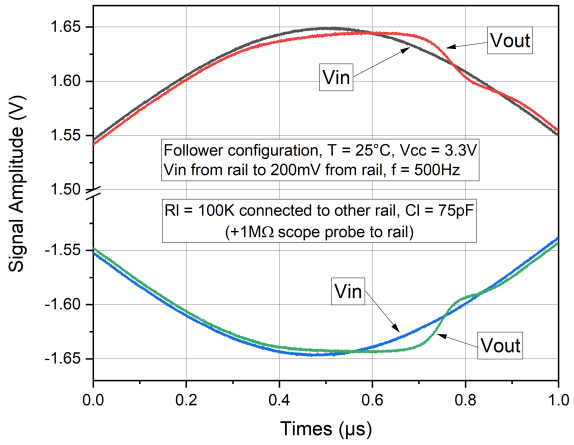


Figure 20. Output saturation with a square wave on the input at F = 100 Hz

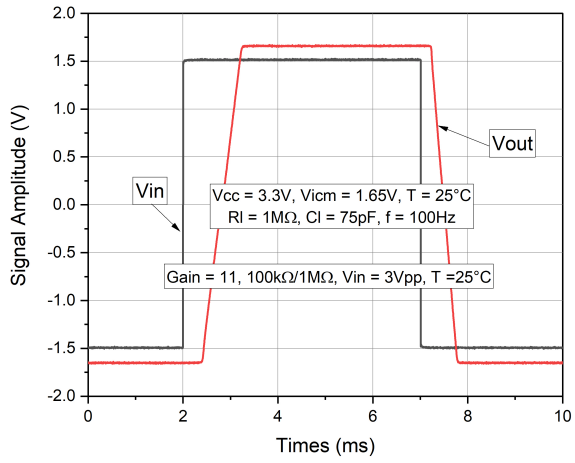


Figure 21. Phase reversal free

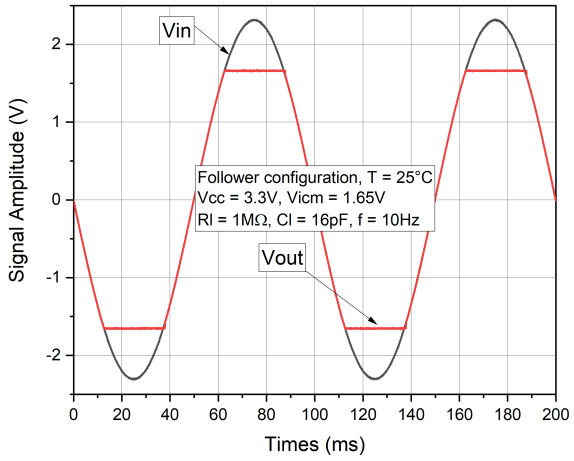


Figure 22. Output swing vs. input signal frequency

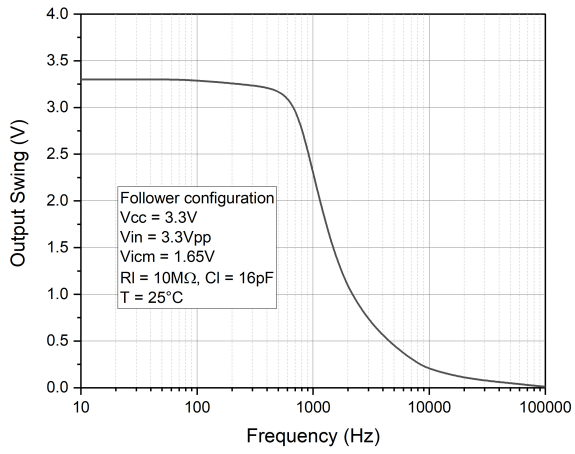


Figure 23. Triangulation of a sine wave at f = 1 kHz

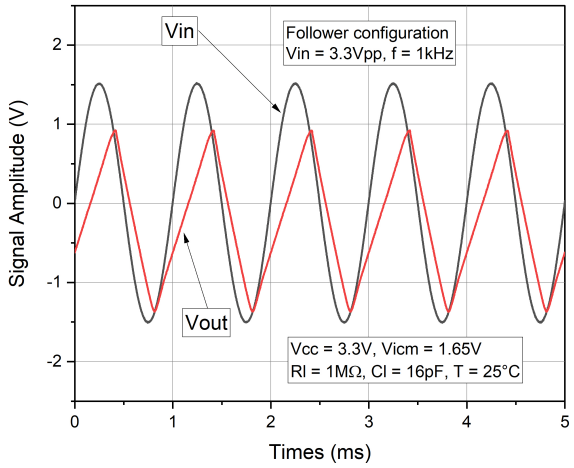


Figure 24. Large signal response at 3.3 V supply voltage at f = 100 Hz

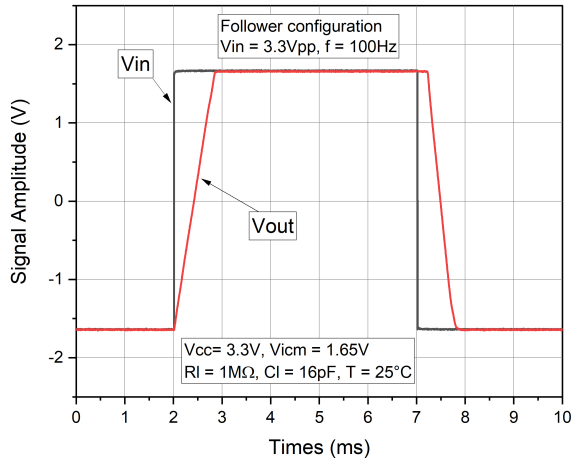


Figure 25. Small signal response at 3.3 V supply voltage at f = 1 kHz

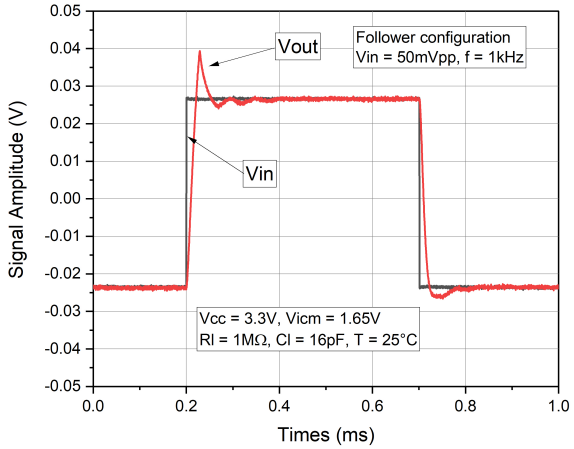


Figure 26. Overshoot vs. capacitive load at 3.3 V supply voltage

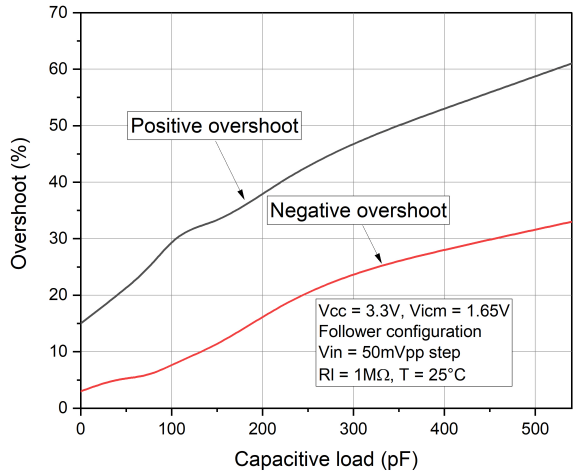


Figure 27. Recovery time from negative saturation vs. supply voltage

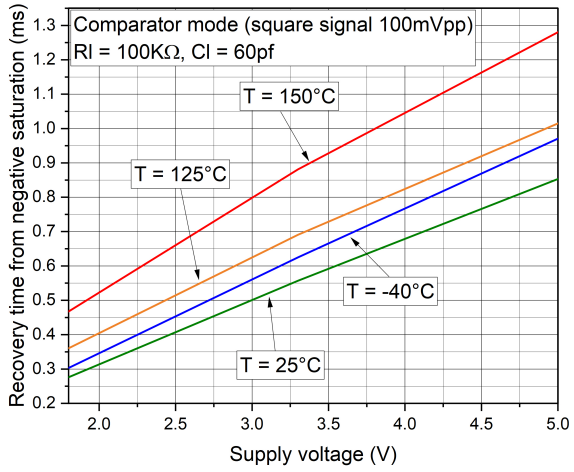


Figure 28. Recovery time from positive saturation vs. supply voltage

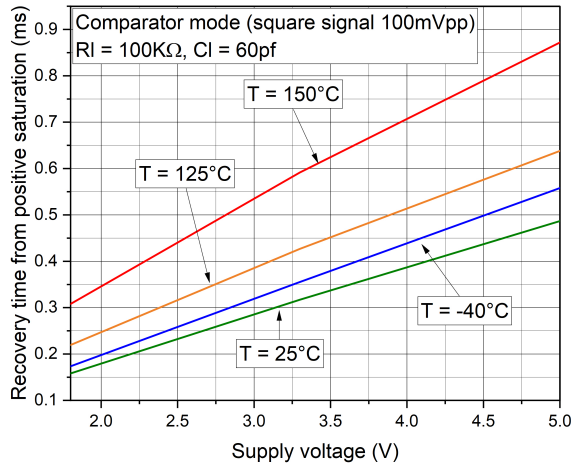


Figure 29. Slew rate vs. supply voltage at mid V_{icm}

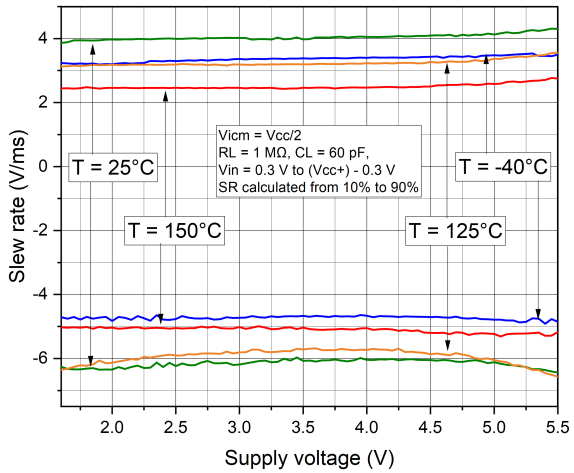


Figure 30. Negative overshoot vs. input common-mode voltage at 1.8 V supply voltage

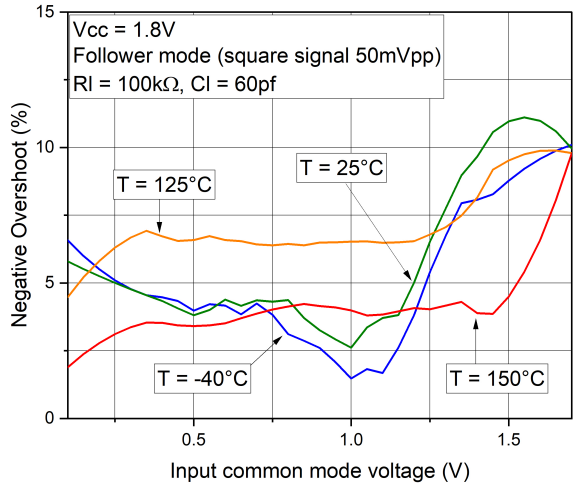


Figure 31. Positive overshoot vs. input common-mode voltage at 1.8 V supply voltage

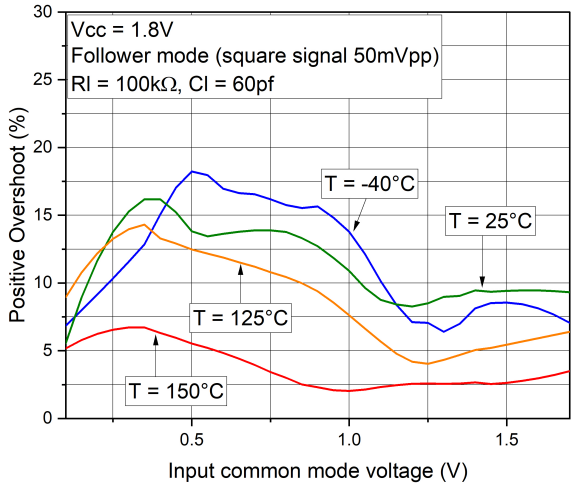


Figure 32. Negative overshoot vs. input common-mode voltage at 3 V supply voltage

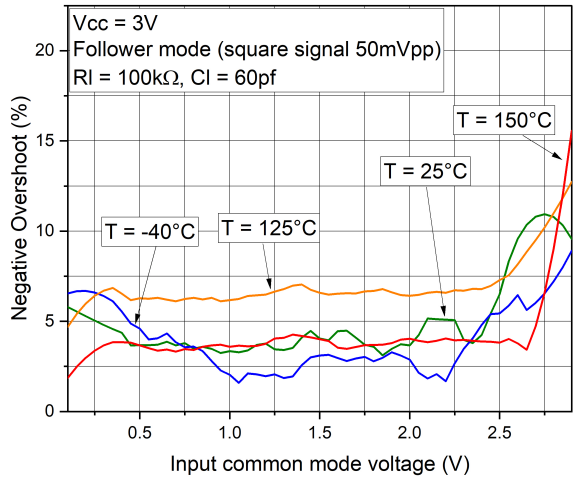


Figure 33. Positive overshoot vs. input common-mode voltage at 3 V supply voltage

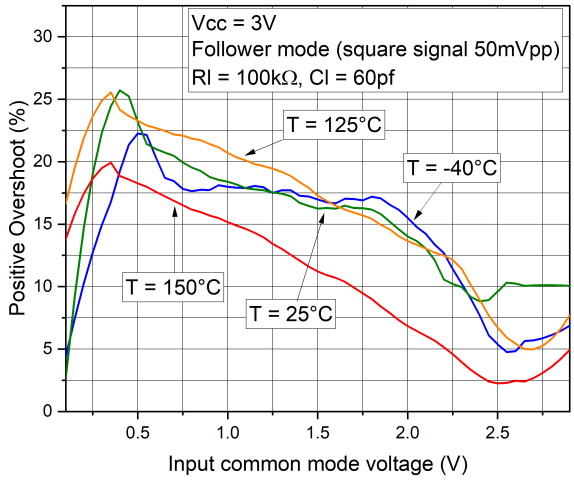


Figure 34. Negative overshoot vs. input common-mode voltage at 5 V supply voltage

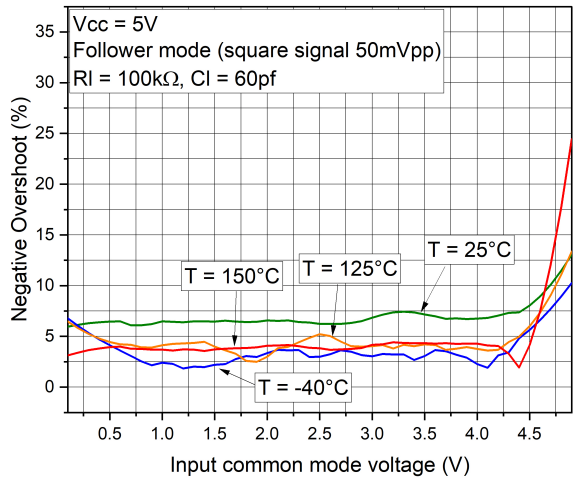


Figure 35. Positive overshoot vs. input common-mode voltage at 5 V supply voltage

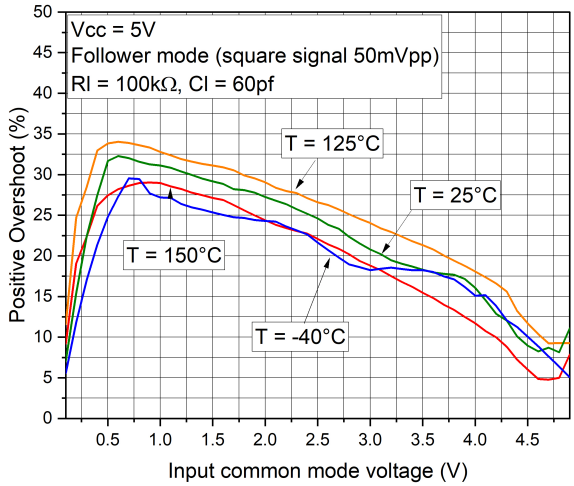


Figure 36. Bode diagram at 1.8 V supply voltage

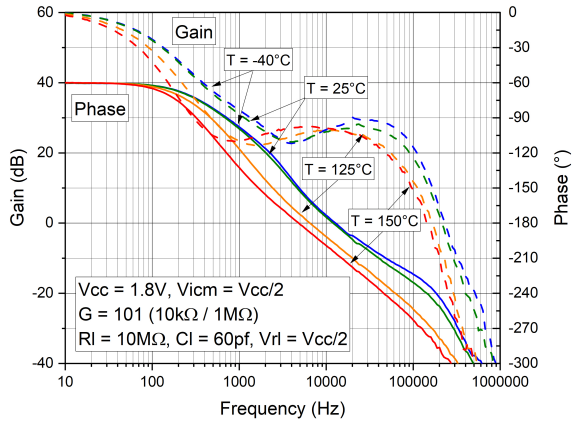


Figure 37. Bode diagram at 3.3 V supply voltage

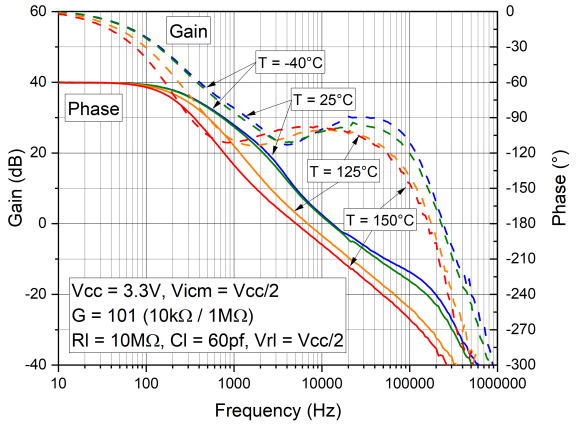


Figure 38. Bode diagram at 5 V supply voltage

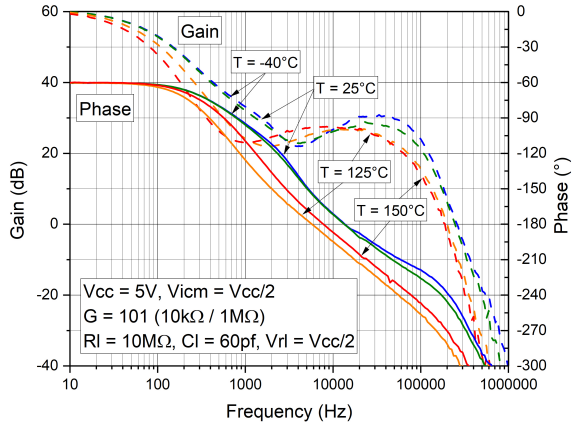


Figure 39. Crosstalk diagram at 1.8 V supply voltage

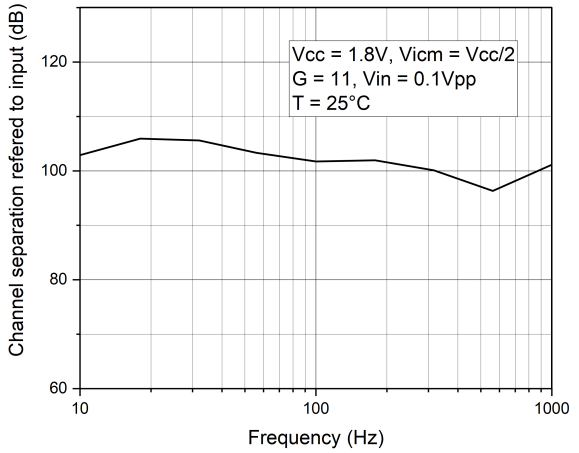


Figure 40. Crosstalk diagram at 5 V supply voltage

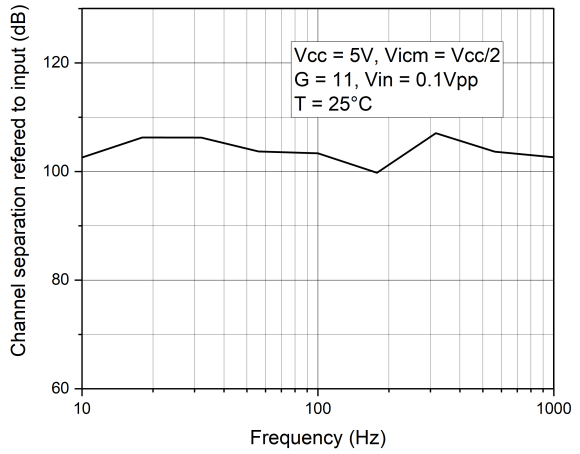


Figure 41. PSRR diagram at 1.8 V supply voltage

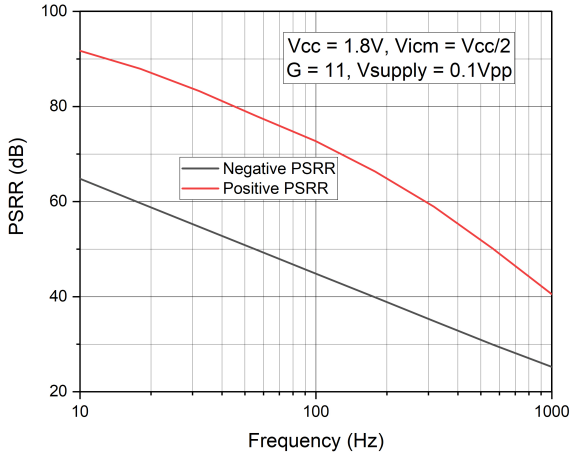


Figure 42. PSRR diagram at 5 V supply voltage

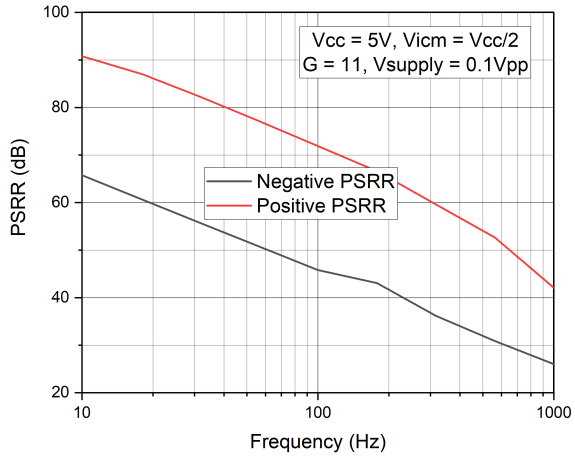


Figure 43. Input referred voltage noise density for different power supply voltages at mid Vicm

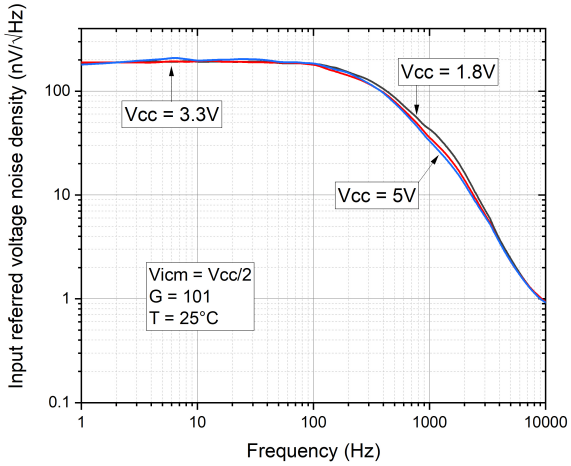


Figure 44. Noise amplitude on 0.1 to 10 Hz freq. range at 1.8 V supply voltage

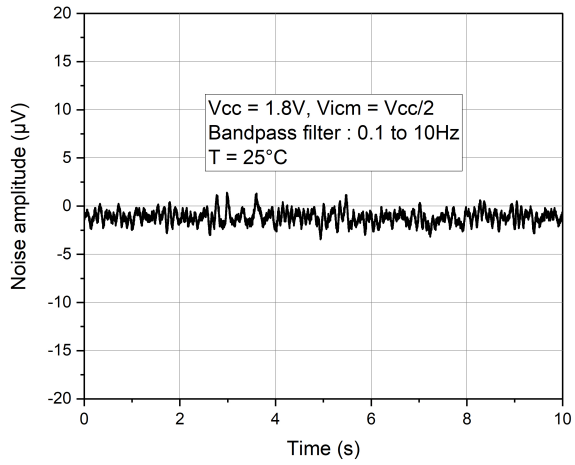


Figure 45. Noise amplitude on 0.1 to 10 Hz freq. range at 3.3 V supply voltage

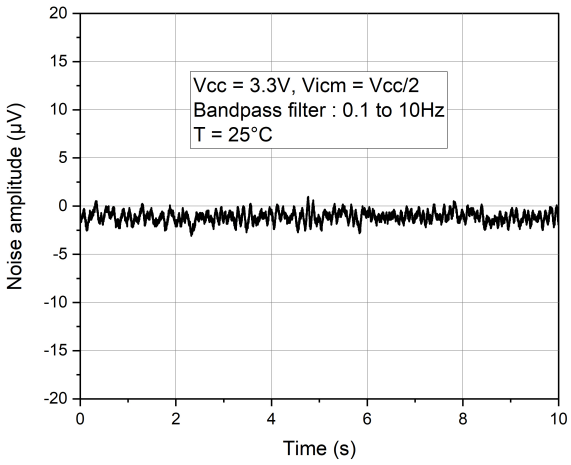


Figure 46. Noise amplitude on 0.1 to 10 Hz freq. range at 5 V supply voltage

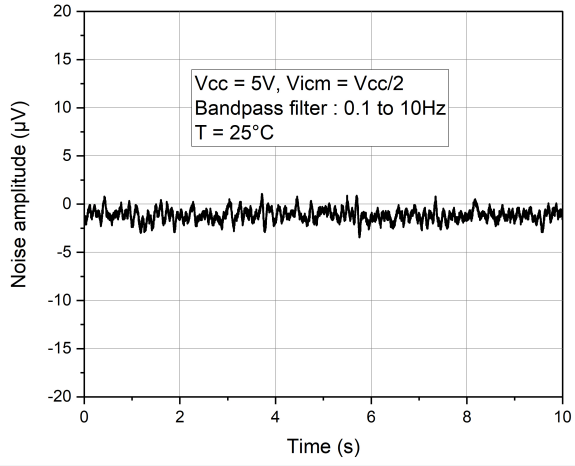


Figure 47. Input offset voltage distribution at 1.8 V supply voltage

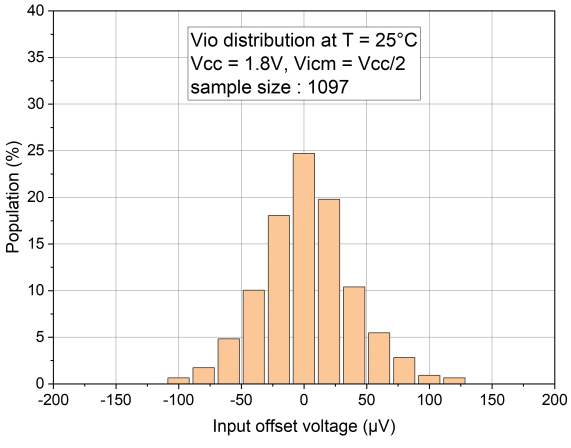


Figure 48. Input offset voltage distribution at 3.3 V supply voltage

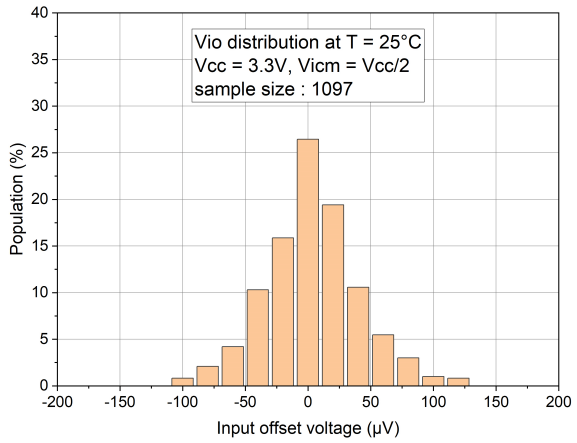


Figure 49. Input offset voltage distribution at 5 V supply voltage

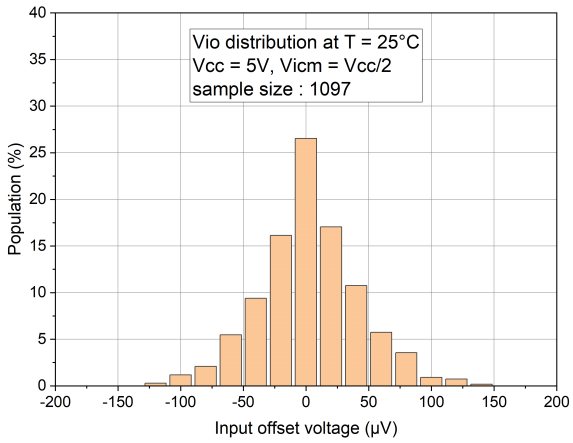


Figure 50. Input offset voltage temperature coefficient distribution from - 40 °C to 25 °C at 1.8 V supply voltage

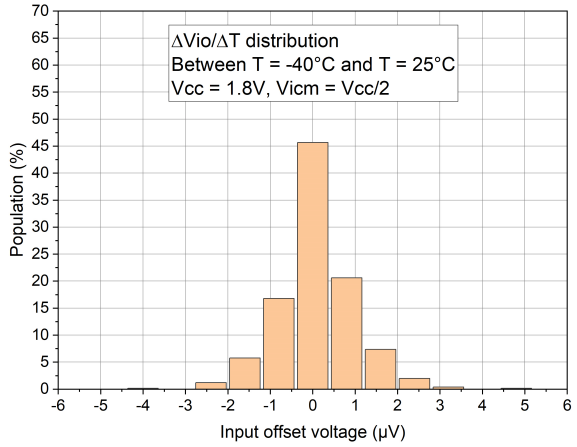


Figure 51. Input offset voltage temperature coefficient distribution from - 40 °C to 25 °C at 5 V supply voltage

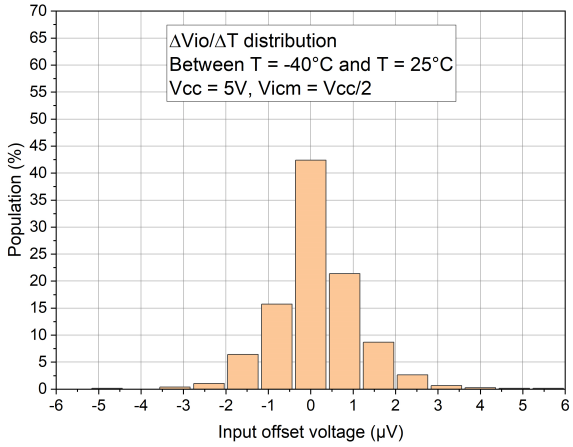


Figure 52. Input offset voltage temperature coefficient distribution from 25 °C to 150 °C at 1.8 V supply voltage

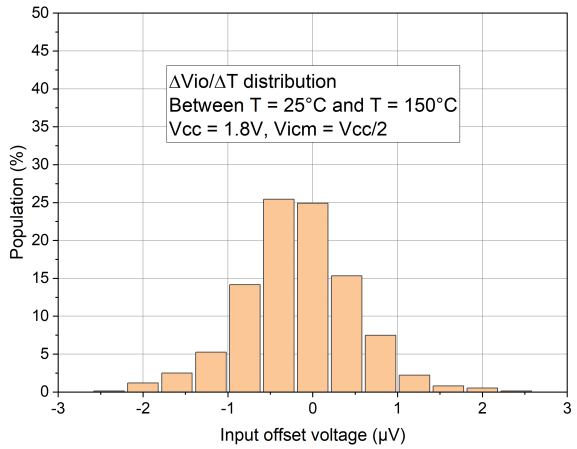


Figure 53. Input offset voltage temperature coefficient distribution from 25 °C to 150 °C at 5 V supply voltage

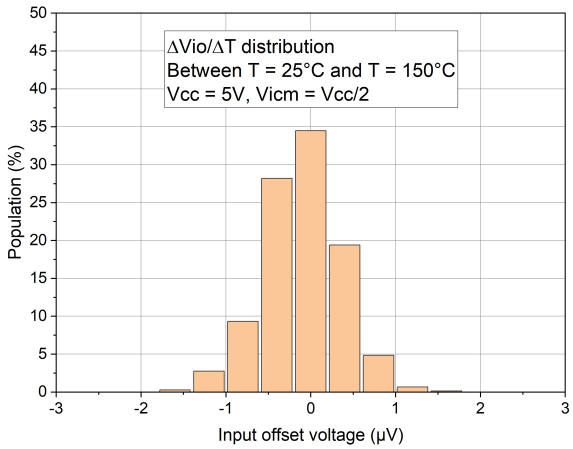


Figure 54. Input offset voltage vs. temperature at 1.8 V supply voltage

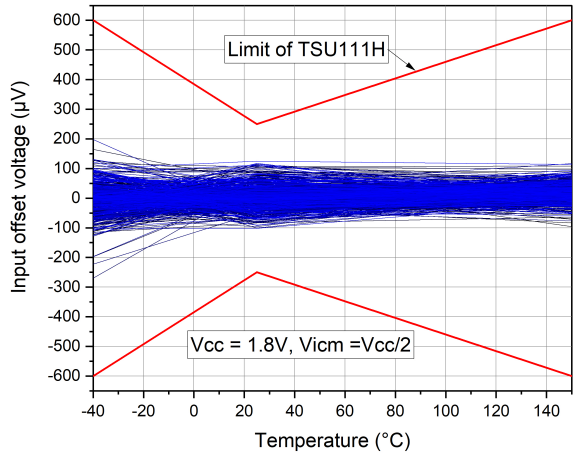
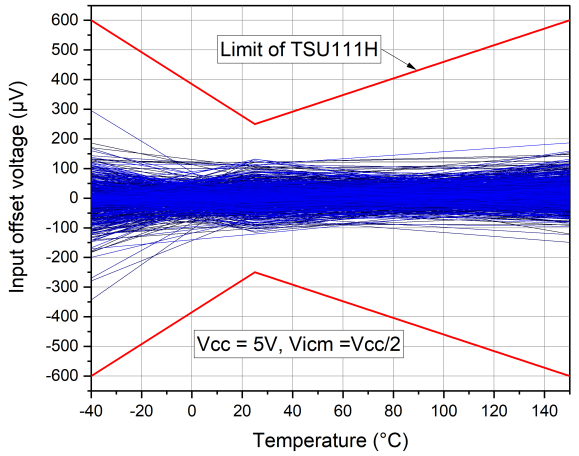


Figure 55. Input offset voltage vs. temperature at 5 V supply voltage



5 Ordering information

5.1 Nanopower applications

The TSU111H can operate from 1.5 V to 5.5 V. The parameters are fully specified at 1.8 V, 3.3 V, and 5 V supply voltages and are very stable in the full VCC range. Additionally, the main specifications are guaranteed on the temperature range from -40 to 150 °C.

5.1.1 Schematic optimization aiming for nanopower

To benefit from the full performance of the TSU111IY, the impedances must be maximized so that current consumption is not lost where it is not required.

For example, an aluminum electrolytic capacitance can have significantly high leakage. This leakage may be greater than the current consumption of the op amp. For this reason, ceramic type capacitors are preferred.

For the same reason, big resistor values should be used in the feedback loop. However, there are two main limitations to be considered when choosing a resistor.

1. Noise generated: a 100 kΩ resistor generates 40 nV/√Hz, a bigger resistor value generates even more noise.
2. Leakage on the PCB: leakage can be generated by moisture. This can be improved by using a specific coating process on the PCB.

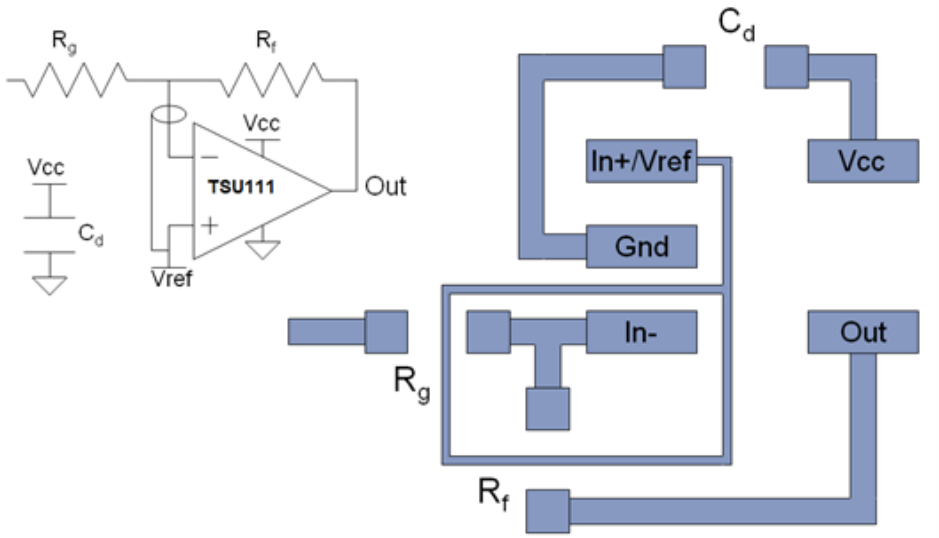
5.1.2 PCB layout considerations

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

Minimizing the leakage from sensitive high impedance nodes on the inputs of the TSU111H can be performed with a guarding technique. The technique consists of surrounding high impedance tracks by a low impedance track (the ring). The ring is at the same electrical potential as the high impedance node.

Therefore, even if some parasitic impedance exists between the tracks, no leakage current can flow through them as they are at the same potential (see Figure 56. Guarding on the PCB).

Figure 56. Guarding on the PCB



5.2 Rail-to-rail input

The TSU111H is built with two complementary PMOS and NMOS input differential pairs. Thus, the device has a rail-to-rail input, and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V.

The TSU111H has been designed to prevent phase reversal behavior.

5.3 Input offset voltage drift overtemperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift overtemperature is computed using Eq. (1).

$$\frac{\Delta V_{IO}}{\Delta T} = \max \left| \frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C} \right| \quad (1)$$

Where T = -40 °C and 150 °C

The TSU111H datasheet maximum values are guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.4 Using the TSU111H with sensors

The TSU111H has MOS inputs, thus input bias currents can be guaranteed down to 10 pA maximum at ambient temperature. This is an important parameter when the operational amplifier is used in combination with high impedance sensors.

The TSU111H is perfectly suited for trans-impedance configuration. This configuration allows a current to be converted into a voltage value with a gain set by the user. It is an ideal choice for portable electrochemical gas sensing or photo/UV sensing applications. The TSU111H, using trans-impedance configuration, is able to provide a voltage value based on the physical parameter sensed by the sensor.

5.5 Fast desaturation

When the TSU111H goes into saturation mode, it takes a short period of time to recover, typically 500 µs. When recovering after saturation, the TSU111H does not exhibit any voltage peaks that could generate issues (such as false alarms) in the application (see Figure 20).

We can observe that this circuit still exhibits good gain even close to the rails, that is, A_{vd} greater than 100 dB for V_{CC} = 3.3 V with V_{out} varying from 200 mV up to a supply voltage minus 200 mV. With a trans-impedance schematic, a voltage reference can be used to keep the signal away from the supply rails.

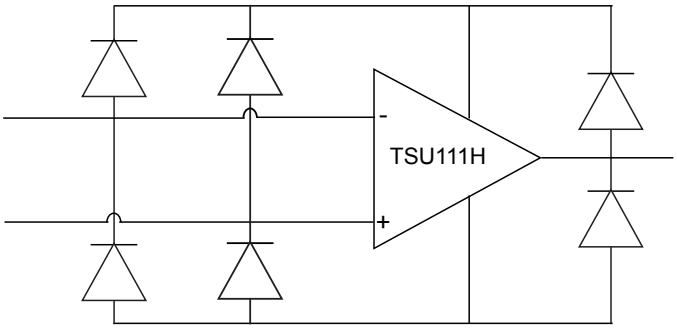
5.6 Using the TSU111H in comparator mode

The TSU111H can be used as a comparator. In this case, the output stage of the device always operates in saturation mode. In addition, Figure 5, Figure 6, Figure 7, show that the current consumption is not higher and even decreases smoothly close to the rails. The TSU111H is obviously an operational amplifier and is therefore optimized for use in linear mode. We recommend using the TS88 series of nanopower comparators if the primary function is to perform a signal comparison only.

5.7 ESD structure of the TSU111H

The TSU111H is protected against electrostatic discharge (ESD) with dedicated diodes (see Figure 57. ESD structure). These diodes must be considered at application level especially when signals applied on the input pins go beyond the power supply rails (V_{CC+}) or (V_{CC-}).

Figure 57. ESD structure



Current through the diodes must be limited to a maximum of 10 mA, as stated in Table 2. A serial resistor on the inputs can be used to limit this current.

5.8 EMI robustness of nanopower devices

Nanopower devices exhibit higher impedance nodes and consequently they are more sensitive to EMI. To improve the natural robustness of the TSU111H device, we recommend adding three capacitors of around 22 pF each between the two inputs, and between each input and ground. These capacitors lower the impedance of the input at high frequencies and therefore reduce the impact of the radiation.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5L package information

Figure 58. SOT23-5L package outline

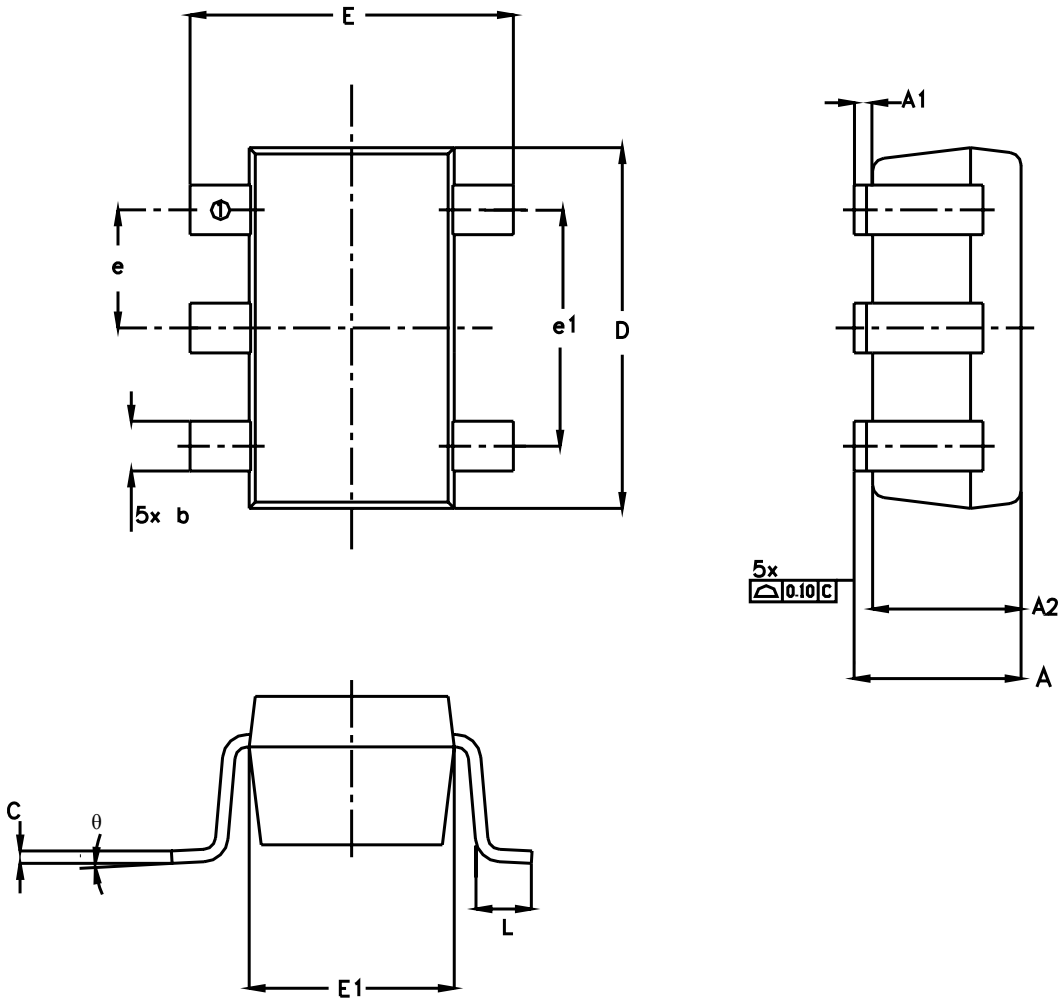
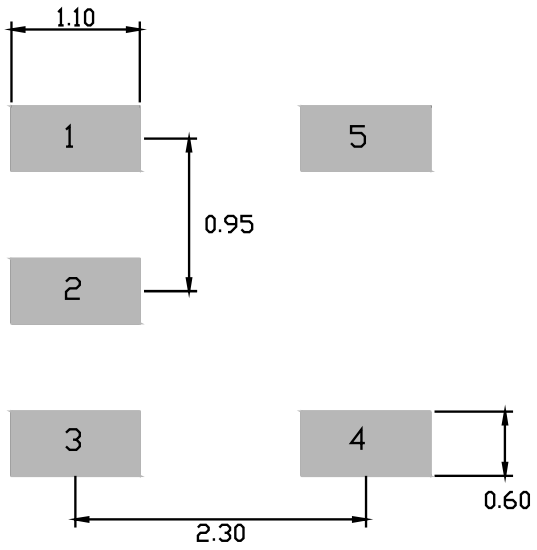


Table 7. **SOT23-5L mechanical data**

Symbol	mm			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1	0.00		0.15	0.000		0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.30		0.50	0.012		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.012	0.018	0.024
θ	0	4	8	0	4	8
N	5			5		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 59. **SOT23-5L recommended footprint**



7 Ordering information

Table 8. Order codes

Order code	Temperature range	Package [1]	Marking
TSU111HYLT	-40 °C to +150 °C	SOT23-5	K1J

1. *All devices are delivered in tape and reel packing.*

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
06-Dec-2022	1	Initial release.

Contents

List of tables

List of figures