# RAD-TOLERANT CLASS V, WIDEBAND, FULLY DIFFERENTIAL AMPLIFIER

## FEATURES

- **Fully Differential Architecture**
- **Centered Input Common-Mode Range**
- **Minimum Gain of 2V/V (6 dB)**
- **Bandwidth: 1100 MHz (Gain = 6 dB)**
- **Slew Rate: 5100 V/µs**
- **1% Settling Time: 5.5 ns**
- **$HD_2$: –76 dBc at 70 MHz**
- **$HD_3$: –88 dBc at 70 MHz**
- **$OIP_2$: 84 dBm at 70 MHz**
- **$OIP_3$: 42 dBm at 70 MHz**
- **Input Voltage Noise: 2.2 nV/√Hz (f >10 MHz)**
- **Noise Figure: 19.8 dB**
- **Output Common-Mode Control**
- **Power Supply:**
  - **Voltage: 3 V (±1.5 V) to 5 V (±2.5 V)**
  - **Current: 37.7 mA**
- **Power-Down Capability: 0.65 mA**
- **Rad-Tolerant: 150 kRad (Si) TID**
- **QML-V Qualified, SMD 5962-07223**

## APPLICATIONS

- **5 V Data-Acquisition Systems**
- **High-Linearity ADC Amplifier**
- **Wireless Communication**
- **Medical Imaging**
- **Test and Measurement**

## RELATED PRODUCTS

| DEVICE | MIN. GAIN | COMMON-MODE RANGE OF INPUT(1) |
|---|---|---|
| THS4511-SP | 6 dB | –0.3 V to 2.3 V |
| THS4513-SP | 6 dB | 0.75 V to 4.25 V |

(1) Assumes a 5 V single-ended power supply.

## DESCRIPTION/ORDERING INFORMATION

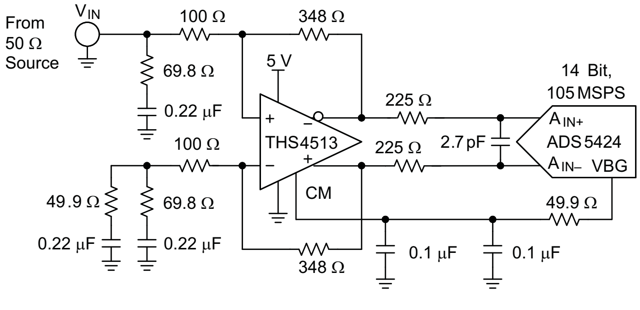
The THS4513 is a wideband, fully differential op amp designed for 3.3 V to 5 V data-acquisition systems. It has very low noise at 2.2 nV/√Hz, and extremely low harmonic distortion of –76 dBc $HD_2$ and –88 dBc $HD_3$ at 70 MHz with 2 Vpp output, G = 14 dB, and 100 Ω load. Slew rate is very high at 5100 V/µs and with settling time of 5.5 ns to 1% (2 V step), it is ideal for pulsed applications. It is suitable for minimum gain of 6 dB.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 5 mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4 mV differential offset voltage. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

The input and output are optimized for best performance with their common-mode voltages set to mid-supply. Along with high performance at low power supply voltage, this makes for extremely high performance single supply 5 V data acquisition systems.

The THS4513 is offered in a 16-pin ceramic flatpack package (W), and is characterized for operation over the full military temperature range from –55°C to 125°C.

**THS4513 + ADS5424 Circuit**



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGING/ORDERING INFORMATION[1]

| TEMPERATURE | PACKAGED DEVICES | |
|---|---|---|
| | **CERAMIC FLATPACK W (16)[2]** | **SYMBOL** |
| –55°C to 125°C | 5962-0722301VFA | 5962-0722301VFA |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

| | | | UNIT |
|---|---|---|---|
| $V_{S-}$ to $V_{S+}$ | Supply voltage | | 6 V |
| $V_I$ | Input voltage | | $\pm V_S$ |
| $V_{ID}$ | Differential input voltage | | 4 V |
| $I_O$ | Output current | | 200 mA |
| | Continuous power dissipation | | See Dissipation Rating Table |
| $T_J$ | Maximum junction temperature | | 150°C |
| $T_A$ | Operating free-air temperature range | | –55°C to 125°C |
| $T_{stg}$ | Storage temperature range | | –65°C to 150°C |
| | ESD ratings | HBM | 2000 |
| | | CDM | 1500 |
| | | MM | 100 |

(1) The absolute maximum ratings under any condition are limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## DISSIPATION RATING TABLE

| PACKAGE | $\theta_{JC}$ | $\theta_{JA}$ | POWER RATING | |
|---|---|---|---|---|
| | | | $T_A \leq 25°C$ | $T_A = 125°C$ |
| W (16) | 14.7°C/W | 189°C/W | 661 mW | 132 mW |

## SPECIFICATIONS; $V_{S+} – V_{S–}$ = 5 V (Unchanged after 150 kRad):

Test conditions unless otherwise noted: $V_{S+}$ = 2.5 V, $V_{S–}$ = –2.5 V, G = 14 dB, CM = open, $V_O$ = 2 Vpp, $R_F$ = 348 Ω, $R_L$ = 200 Ω Differential, $T_A$ = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to Mid-Supply

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| Small-Signal Bandwidth | G = 6 dB, $V_O$ = 100 mVpp | | | 1.1 | | GHz |
| | G = 10 dB, $V_O$ = 100 mVpp | | | 1.0 | | GHz |
| | G = 14 dB, $V_O$ = 100 mVpp | | | 720 | | MHz |
| Gain-Bandwidth Product | G = 10 dB | | | 3.0 | | GHz |
| Bandwidth for 0.1 dB Flatness | G = 10 dB, $V_O$ = 2 Vpp | | | 65 | | MHz |
| | G = 14 dB, $V_O$ = 2 Vpp | | | 115 | | |
| Large-Signal Bandwidth | G = 6 dB, $V_O$ = 2 Vpp | | | 1.1 | | GHz |
| Slew Rate (Differential) | 2 V Step, G = 6 dB | | | 5100 | | V/µs |
| Rise Time Fall Time | | | | 0.5 | | ns |
| | | | | 0.5 | | |
| Settling Time to 1% | | | | 5.5 | | |
| 2nd Order Harmonic Distortion | f = 10 MHz, $R_L$ = 100 Ω | | | –106 | | dBc |
| | f = 50 MHz, $R_L$ = 100 Ω | | | –90 | | |
| | f = 100 MHz, $R_L$ = 100 Ω | | | –87 | | |
| 3rd Order Harmonic Distortion | f = 10 MHz, $R_L$ = 100 Ω | | | –108 | | dBc |
| | f = 50 MHz, $R_L$ = 100 Ω | | | –106 | | |
| | f = 100 MHz, $R_L$ = 100 Ω | | | –83 | | |
| 2nd Order Intermodulation Distortion | $V_O$ = 2 Vpp envelope, 200 kHz Tone Spacing, $R_L$ = 100 Ω | $f_C$ = 50 MHz | | –83 | | dBc |
| | | $f_C$ = 100 MHz | | –75 | | |
| 3rd Order Intermodulation Distortion | | $f_C$ = 50 MHz | | –83 | | |
| | | $f_C$ = 100 MHz | | –74 | | |
| 2nd Order Output Intercept Point | 200 kHz Tone Spacing $R_L$ = 100 Ω | $f_C$ = 50 MHz | | 84 | | dBm |
| | | $f_C$ = 100 MHz | | 77 | | |
| 3rd Order Output Intercept Point | | $f_C$ = 50 MHz | | 42 | | |
| | | $f_C$ = 100 MHz | | 38 | | |
| Noise Figure | 50 Ω System, 10 MHz, G = 6 dB | | | 19.8 | | dB |
| Input Voltage Noise | f > 10 MHz | | | 2.2 | | nV/$\sqrt{Hz}$ |
| Input Current Noise | f > 10 MHz | | | 1.7 | | pA/$\sqrt{Hz}$ |
| **DC PERFORMANCE** | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | | | | 63 | | dB |
| Input Offset Voltage | $T_A$ = 25°C | | | 1 | 4 | mV |
| | $T_A$ = –55°C to 125°C | | | | 5.5 | mV |
| Average Offset Voltage Drift | $T_A$ = –55°C to 125°C | | | 2.6 | | µV/°C |
| Input Bias Current | $T_A$ = 25°C | | | 8 | 15.5 | µA |
| | $T_A$ = –55°C to 125°C | | | | 20 | |
| Average Bias Current Drift | $T_A$ = –55°C to 125°C | | | 20 | | nA/°C |
| Input Offset Current | $T_A$ = 25°C | | | 1.6 | 3.6 | µA |
| | $T_A$ = –55°C to 125°C | | | | 7 | |
| Average Offset Current Drift | $T_A$ = –55°C to 125°C | | | 4 | | nA/°C |

## SPECIFICATIONS; $V_{S+}$ – $V_{S–}$ = 5 V (Unchanged after 150 kRad): (continued)

Test conditions unless otherwise noted: $V_{S+}$ = 2.5 V, $V_{S–}$ = –2.5 V, G = 14 dB, CM = open, $V_O$ = 2 Vpp, $R_F$ = 348 Ω, $R_L$ = 200 Ω Differential, $T_A$ = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to Mid-Supply

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| Common-Mode Input Range High | | | | 1.75 | | V |
| Common-Mode Input Range Low | | | | –1.75 | | |
| Common-Mode Rejection Ratio | | | | 80 | | dB |
| Differential Input Impedance | | | | 1.67 \|\| 0.5 | | MΩ \|\| pF |
| Common-Mode Input Impedance | | | | 1.2 \|\| 1.5 | | |
| **OUTPUT** | | | | | | |
| Maximum Output Voltage High | Each output with 100Ω to mid-supply | $T_A$ = 25°C | 1.2 | 1.4 | | V |
| | | $T_A$ = –55°C to 125°C | 1.0 | | | |
| Minimum Output Voltage Low | | $T_A$ = 25°C | | –1.4 | –1.2 | V |
| | | $T_A$ = –55°C to 125°C | | | –1.0 | |
| Differential Output Voltage Swing | $T_A$ = 25°C | | 4.8 | 5.6 | | V |
| | $T_A$ = –55°C to 125°C | | 4.0 | | | |
| Differential Output Current Drive | $R_L$ = 10 Ω | | | 96 | | mA |
| Output Balance Error | $V_O$ = 100 mV, f = 1 MHz | | | –52 | | dB |
| Closed-Loop Output Impedance | f = 1 MHz | | | 0.3 | | Ω |
| **OUTPUT COMMON-MODE VOLTAGE CONTROL** | | | | | | |
| Small-Signal Bandwidth | | | | 250 | | MHz |
| Slew Rate | | | | 110 | | V/μs |
| Gain | | | | 1 | | V/V |
| Output Common-Mode Offset from CM input | –1 V < CM < 1 V | | | 5 | | mV |
| CM Input Bias Current | –1 V < CM < 1 V | | | ±40 | | μA |
| CM Input Voltage Range | | | | –1.25 to 1.25 | | V |
| CM Input Impedance | | | | 23 \|\| 2.8 | | kΩ \|\| pF |
| CM Default Voltage | | | | 0 | | V |
| **POWER SUPPLY** | | | | | | |
| Specified Operating Voltage | | | 3 | 5 | 5.5 | V |
| Maximum Quiescent Current | $T_A$ = 25°C | | | 37.7 | 40.9 | mA |
| | $T_A$ = –55°C to 125°C | | | | 42.5 | |
| Minimum Quiescent Current | $T_A$ = 25°C | | 34.5 | 37.7 | | mA |
| | $T_A$ = –55°C to 125°C | | 32.5 | | | |
| Power Supply Rejection (±PSRR) | | | | 90 | | dB |
| **POWER DOWN** | | | | | | |
| Enable Voltage Threshold | Referenced to $V_{S–}$ , Assured *on* above 2.1 V + $V_{S–}$ | | | >2.1 + $V_{S–}$ | | V |
| Disable Voltage Threshold | Assured *off* below 0.7 V + $V_{S–}$ | | | <0.7 + $V_{S–}$ | | V |
| Powerdown Quiescent Current | $T_A$ = 25°C | | | 0.65 | 0.9 | mA |
| | $T_A$ = –55°C to 125°C | | | | 1.2 | |
| Input Bias Current | $\overline{PD}$ = $V_{S–}$ | | | 100 | | μA |
| Input Impedance | | | | 50 \|\| 2 | | kΩ \|\| pF |
| Turn-on Time Delay | Measured to output on | | | 55 | | ns |
| Turn-off Time Delay | Measured to output off | | | 10 | | μs |

## SPECIFICATIONS; $V_{S+} – V_{S–}$ = 3 V (Unchanged after 150 kRad):

Test conditions unless otherwise noted: $V_{S+}$ = 1.5 V, $V_{S–}$ = –1.5 V, G = 14 dB, CM = open, $V_O$ = 1 Vpp, $R_F$ = 348 Ω, $R_L$ = 200 Ω Differential, $T_A$ = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to Mid-Supply

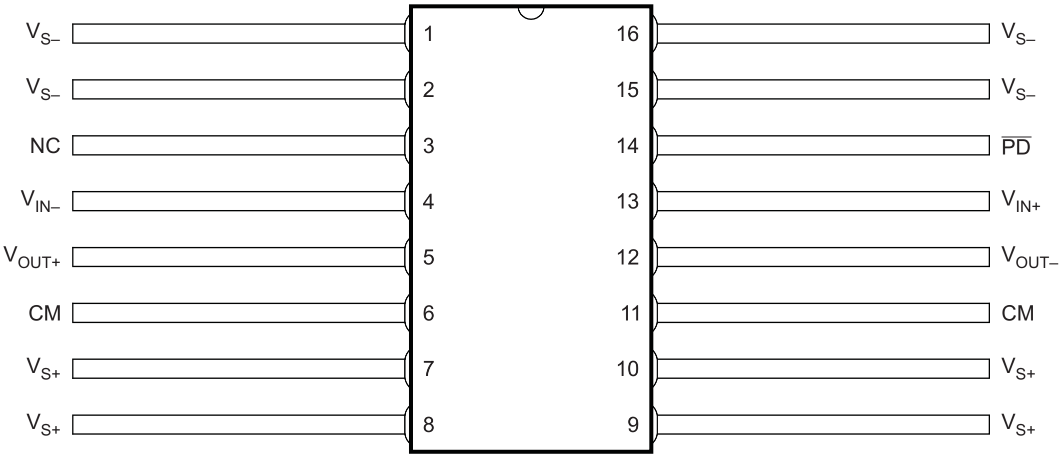
| PARAMETER | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|
| **AC PERFORMANCE** | | | | |
| Small-Signal Bandwidth | G = 6 dB, $V_O$ = 100 mVpp | | 1.1 | GHz |
| | G = 10 dB, $V_O$ = 100 mVpp | | 1.0 | GHz |
| Gain-Bandwidth Product | G = 10 dB | | 3.0 | GHz |
| Bandwidth for 0.1 dB Flatness | G = 10 dB, $V_O$ = 1 Vpp | | 68 | MHz |
| | G = 14 dB, $V_O$ = 1 Vpp | | 115 | |
| Large-Signal Bandwidth | G = 6 dB, $V_O$ = 1 Vpp | | 1.1 | GHz |
| Slew Rate (Differential) | 1V Step, G = 6 dB | | 2600 | V/µs |
| Rise Time | | | 0.25 | ns |
| Fall Time | | | 0.25 | |
| Settling Time to 1% | | | 5.5 | |
| $2^{nd}$ Order Harmonic Distortion | f = 10 MHz, $R_L$ = 100 Ω | | –100 | dBc |
| | f = 50 MHz, $R_L$ = 100 Ω | | –70 | |
| | f = 100 MHz, $R_L$ = 100 Ω | | –63 | |
| $3^{rd}$ Order Harmonic Distortion | f = 10 MHz, $R_L$ = 100 Ω | | –75 | dBc |
| | f = 50 MHz, $R_L$ = 100 Ω | | –64 | |
| | f = 100 MHz, $R_L$ = 100 Ω | | –45 | |
| $2^{nd}$ Order Intermodulation Distortion | $V_O$ = 1 Vpp<br>200 kHz Tone Spacing,<br>$R_L$ = 100 Ω | $f_C$ = 50 MHz | –93 | dBc |
| | | $f_C$ = 100 MHz | –80 | |
| $3^{rd}$ Order Intermodulation Distortion | | $f_C$ = 50 MHz | –80 | |
| | | $f_C$ = 100 MHz | –74 | |
| $2^{nd}$ Order Output Intercept Point | 200 kHz Tone Spacing<br>$R_L$ = 100 Ω | $f_C$ = 50 MHz | 58 | dBm |
| | | $f_C$ = 100 MHz | 52 | |
| $3^{rd}$ Order Output Intercept Point | | $f_C$ = 50 MHz | 32 | |
| | | $f_C$ = 100 MHz | 26 | |
| Noise Figure | 50 Ω System, 10 MHz, G = 6 dB | | 19.8 | dB |
| Input Voltage Noise | f > 10 MHz | | 2.2 | nV/√Hz |
| Input Current Noise | f > 10 MHz | | 1.7 | pA/√Hz |
| **DC PERFORMANCE** | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | | | 68 | dB |
| Input Offset Voltage | $T_A$ = 25°C | | 1 | mV |
| Average Offset Voltage Drift | $T_A$ = –55°C to 125°C | | 2.6 | µV/°C |
| Input Bias Current | $T_A$ = 25°C | | 6 | µA |
| Average Bias Current Drift | $T_A$ = –55°C to 125°C | | 20 | nA/°C |
| Input Offset Current | $T_A$ = 25°C | | 1.6 | µA |
| Average Offset Current Drift | $T_A$ = –55°C to 125°C | | 4 | nA/°C |
| **INPUT** | | | | |
| Common-Mode Input Range High | | | 0.75 | V |
| Common-Mode Input Range Low | | | –0.75 | |
| Common-Mode Rejection Ratio | | | 80 | dB |
| Differential Input Impedance | | | 1.67 \|\| 0.5 | MΩ \|\| pF |
| Common-Mode Input Impedance | | | 1.2 \|\| 1.5 | |

## SPECIFICATIONS; $V_{S+} - V_{S-}$ = 3 V (Unchanged after 150 kRad): (continued)

Test conditions unless otherwise noted: $V_{S+}$ = 1.5 V, $V_{S-}$ = –1.5 V, G = 14 dB, CM = open, $V_O$ = 1 Vpp, $R_F$ = 348 Ω, $R_L$ = 200 Ω Differential, $T_A$ = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to Mid-Supply

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| **OUTPUT** | | | |
| Maximum Output Voltage High | Each output with 100 Ω to mid-supply | 0.45 | V |
| Minimum Output Voltage Low | | –0.45 | V |
| Differential Output Voltage Swing | | 1.8 | V |
| Differential Output Current Drive | $R_L$ = 10 Ω | 50 | mA |
| Output Balance Error | $V_O$ = 100 mV, f = 1 MHz | –54 | dB |
| Closed-Loop Output Impedance | f = 1 MHz | 0.3 | Ω |
| **OUTPUT COMMON-MODE VOLTAGE CONTROL** | | | |
| Small-Signal Bandwidth | | 150 | MHz |
| Slew Rate | | 60 | V/μs |
| Gain | | 1 | V/V |
| Output Common-Mode Offset from CM input | –0.5 V < CM < 0.5 V | 4 | mV |
| CM Input Bias Current | –0.5 V < CM < 0.5 V | ±40 | μA |
| CM Input Voltage Range | | –1.5 to 1.5 | V |
| CM Input Impedance | | 20 \|\| 2.8 | kΩ \|\| pF |
| CM Default Voltage | | 0 | V |
| **POWER SUPPLY** | | | |
| Quiescent Current | | 34.8 | mA |
| Power Supply Rejection (±PSRR) | | 80 | dB |
| **POWER DOWN** | | | |
| Enable Voltage Threshold | Referenced to $V_{s-}$ ,Assured *on* above 2.1 V + $V_{S-}$ | >2.1 | V |
| Disable Voltage Threshold | Assured *off* below 0.7 V + $V_{S-}$ | <0.7 | V |
| Powerdown Quiescent Current | | 0.46 | mA |
| Input Bias Current | $\overline{PD}$ = $V_{S-}$ | 65 | μA |
| Input Impedance | | 50 \|\| 2 | kΩ \|\| pF |
| Turn-On Time Delay | Measured to output on | 100 | ns |
| Turn-Off Time Delay | Measured to output off | 10 | μs |

**W PACKAGE
TOP VIEW**



## TERMINAL FUNCTIONS

| TERMINAL (RGT PACKAGE) | | DESCRIPTION |
|---|---|---|
| NO. | NAME | |
| 3 | NC | No internal connection |
| 4 | $V_{IN-}$ | Inverting amplifier input |
| 5 | $V_{OUT+}$ | Non-inverting amplifier output |
| 6, 11 | CM | Common-mode voltage input |
| 7, 8, 9, 10 | $V_{S+}$ | Positive amplifier power supply input |
| 12 | $V_{OUT-}$ | Inverting amplifier output |
| 13 | $V_{IN+}$ | Non-inverting amplifier input |
| 14 | $\overline{PD}$ | Powerdown, $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or open for normal operation |
| 1, 2, 15, 16 | $V_{S-}$ | Negative amplifier power supply input |

## TYPICAL CHARACTERISTICS

### TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 5$ V

Test conditions unless otherwise noted: $V_{S+} = +2.5$ V, $V_{S-} = -2.5$V, CM = open, $V_{OD} = 2$ Vpp, $R_F = 348\ \Omega$, $R_L = 200\ \Omega$ Differential, G = 14 dB, Single-Ended Input, Input and Output Referenced to Mid-Supply

| | | | |
|---|---|---|---|
| Small-Signal Frequency Response | G = 6 dB, $V_{OD} = 100$ $mV_{PP}$ | | Figure 1 |
| | G = 10 dB, $V_{OD} = 100$ $mV_{PP}$ | | Figure 2 |
| | G = 14 dB, $V_{OD} = 100$ $mV_{PP}$ | | Figure 3 |
| Large-Signal Frequency Response | G = 6 dB, $V_{OD} = 2$ $V_{PP}$ | | Figure 4 |
| | G = 10 dB, $V_{OD} = 2$ $V_{PP}$ | | Figure 5 |
| | G = 14 dB, $V_{OD} = 2$ $V_{PP}$ | | Figure 6 |
| Harmonic Distortion | $HD_2$, G = 14 dB, $V_{OD} = 2$ $V_{PP}$ | vs Frequency | Figure 7 |
| | $HD_3$, G = 14 dB, $V_{OD} = 2$ $V_{PP}$ | vs Frequency | Figure 8 |
| | $HD_2$, G = 14 dB | vs Output Voltage | Figure 9 |
| | $HD_3$, G = 14 dB | vs Output Voltage | Figure 10 |
| Intermodulation Distortion | $IMD_2$, G = 14dB | vs Frequency | Figure 11 |
| | $IMD_3$, G = 14dB | vs Frequency | Figure 12 |
| Output Intercept Point | $OIP_2$ | vs Frequency | Figure 13 |
| | $OIP_3$ | vs Frequency | Figure 14 |
| Transition Rate | | vs Output Voltage | Figure 15 |
| Transient Response | | | Figure 16 |
| Rejection Ratio | | vs Frequency | Figure 17 |
| Overdrive Recovery | | | Figure 18 |
| Output Voltage Swing | | vs Load Resistance | Figure 19 |
| Turn-Off Time | | | Figure 20 |
| Turn-On Time | | | Figure 21 |
| Input Offset Voltage | | vs Input Common-Mode Voltage | Figure 22 |
| Input Referred Noise | | vs Frequency | Figure 23 |
| Noise Figure | | vs Frequency | Figure 24 |
| Quiescent Current | | vs Supply Voltage | Figure 25 |
| Power Down Quiescent Current | | vs Supply Voltage | Figure 26 |
| Output Balance Error | | vs Frequency | Figure 27 |
| CM Input Bias Current | | vs CM Input Voltage | Figure 28 |
| Differential Output Offset Voltage | | vs CM Input Voltage | Figure 29 |
| Common-Mode Output Offset Voltage | | vs CM Input Voltage | Figure 30 |

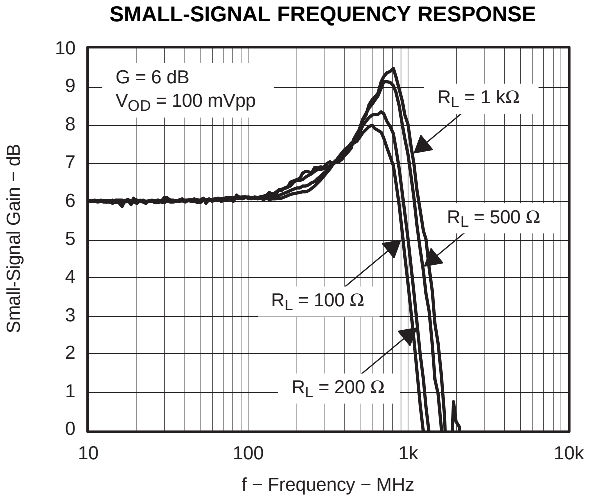


Figure 1.

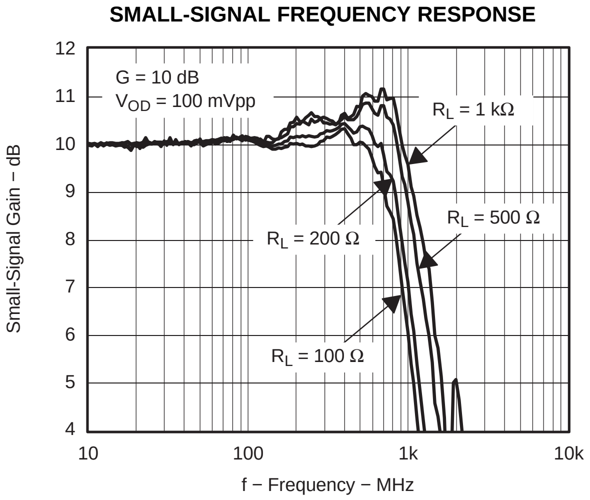


Figure 2.

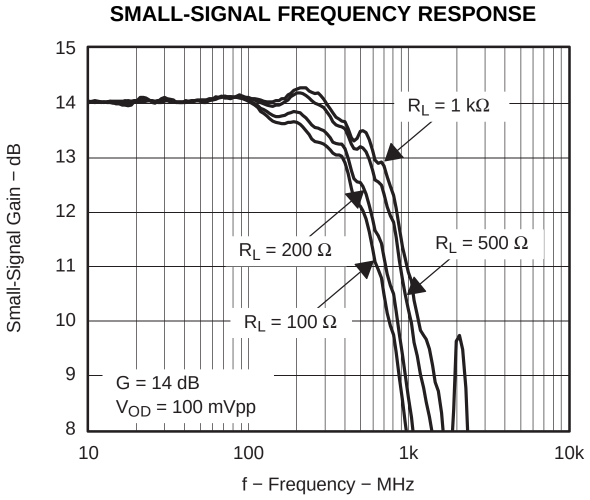


Figure 3.

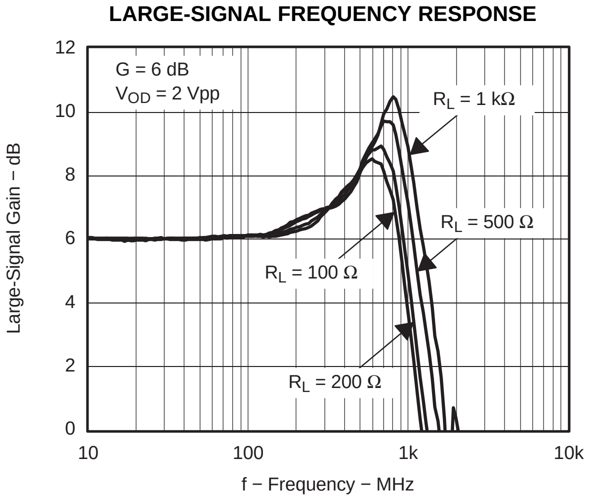


Figure 4.

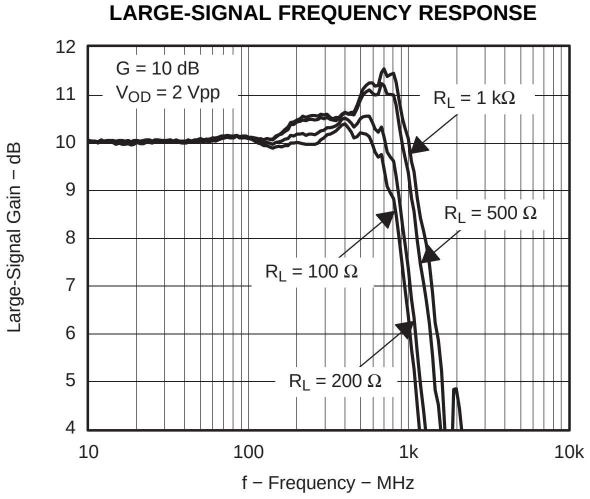


Figure 5.

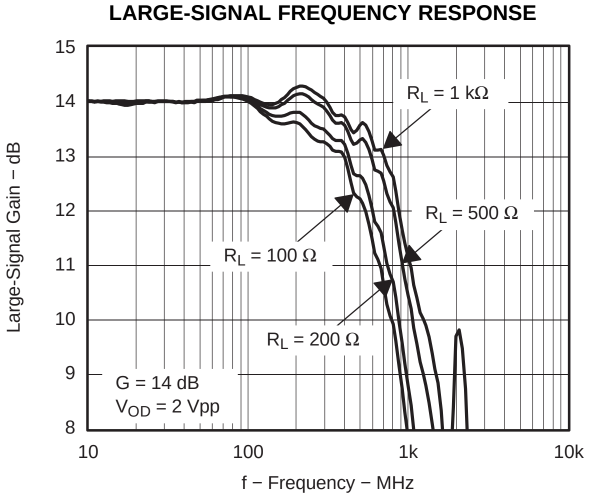


Figure 6.

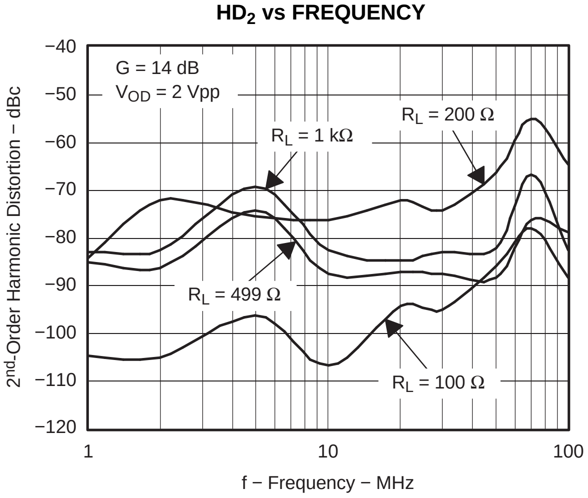


Figure 7.

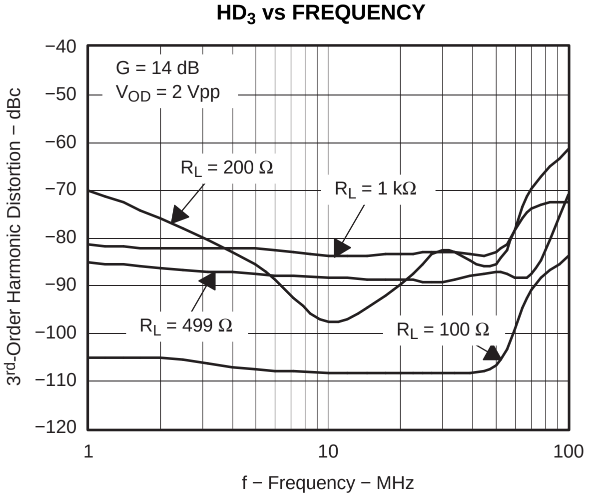


Figure 8.

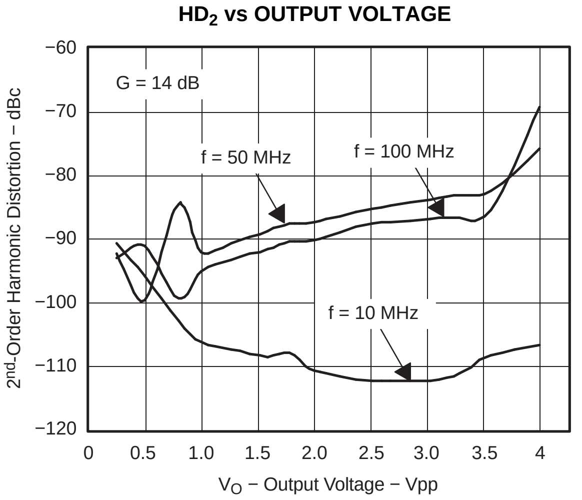


Figure 9.

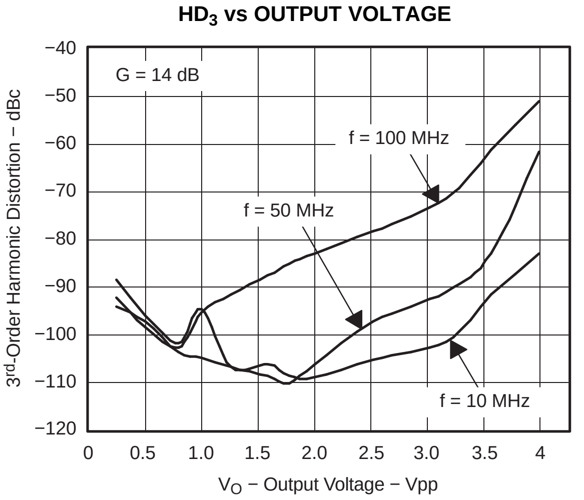
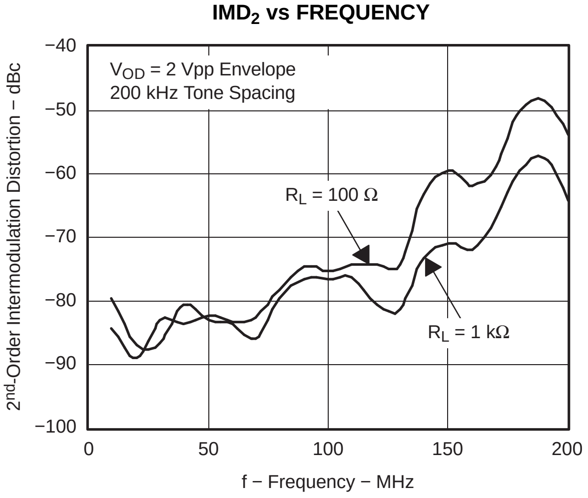


Figure 10.



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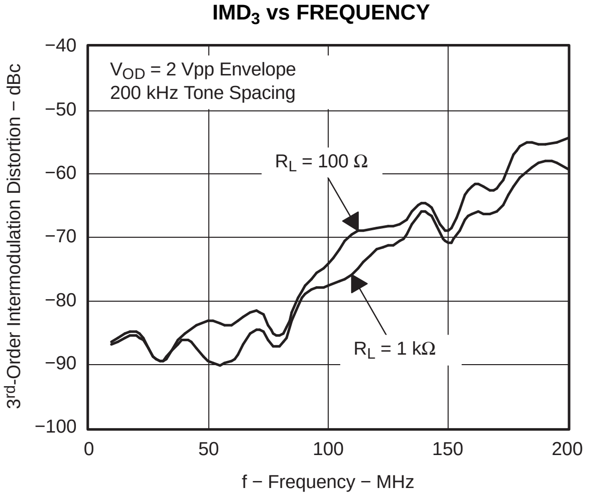

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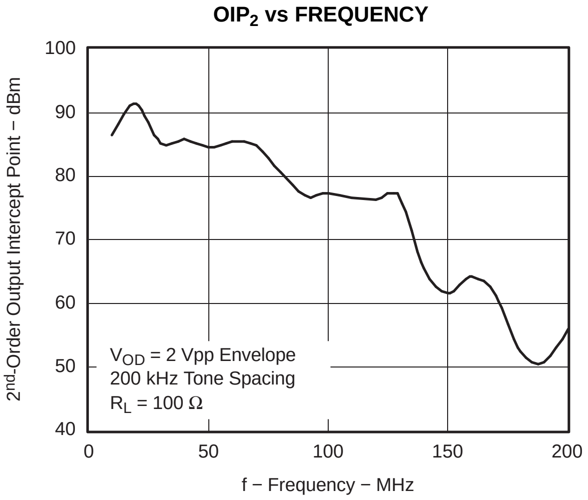

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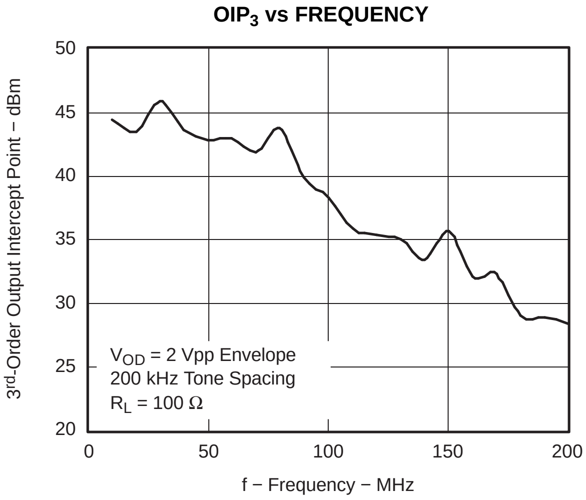

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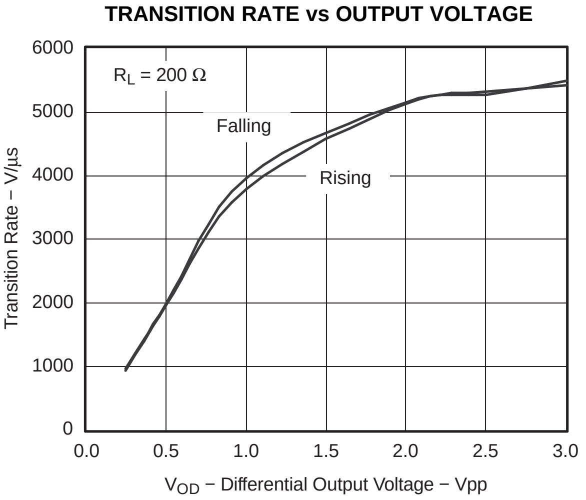

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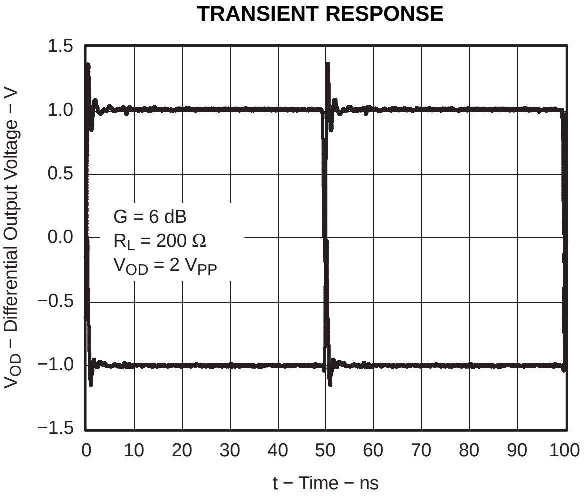

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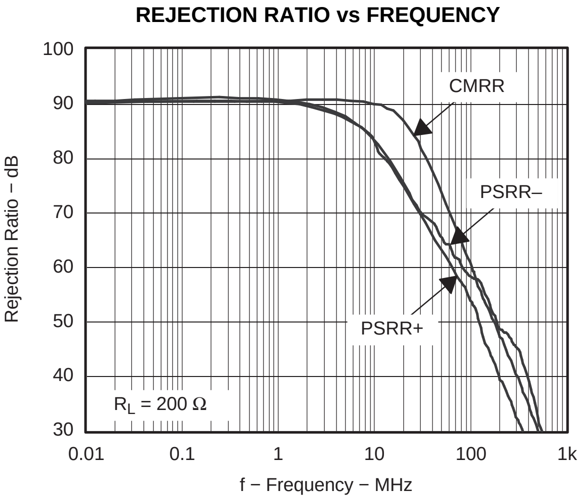

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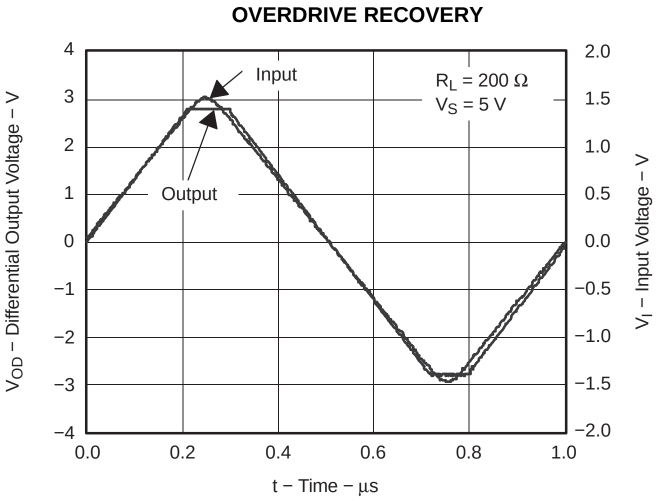

Figure 18.

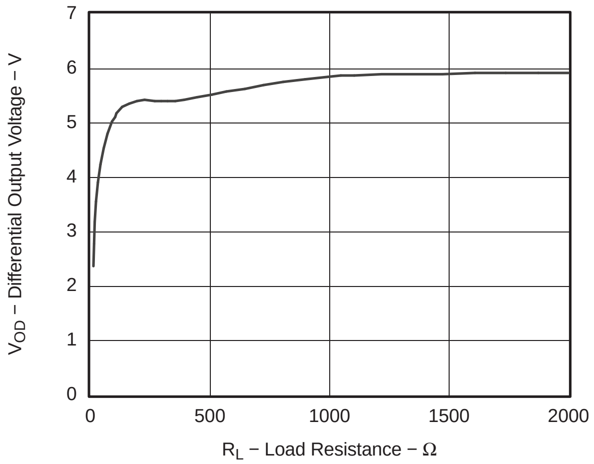
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

**Figure 19.**

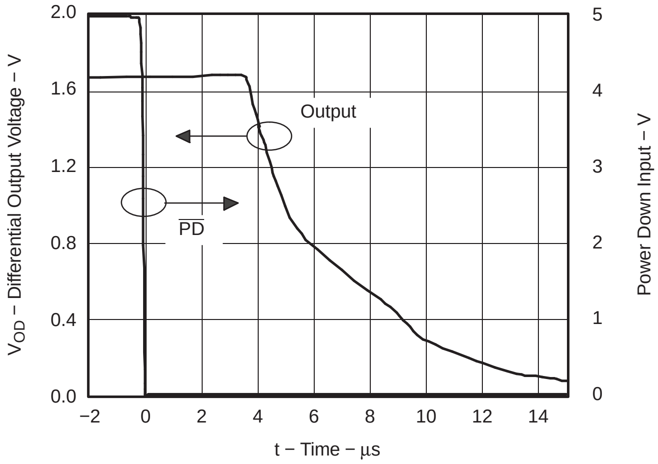
TURN-OFF TIME

**Figure 20.**

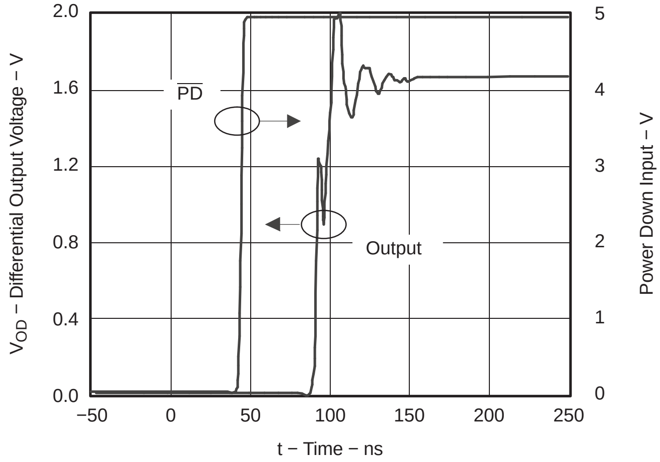
TURN-ON TIME

**Figure 21.**

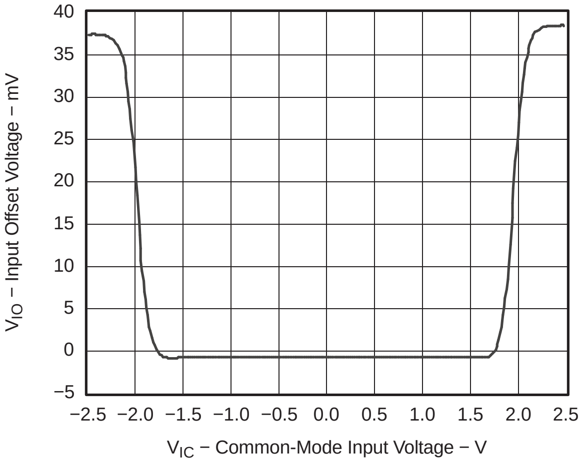
INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

**Figure 22.**

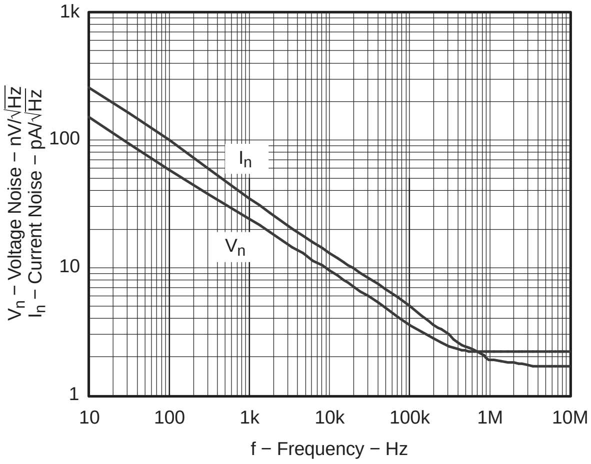
INPUT REFERRED NOISE vs FREQUENCY

**Figure 23.**

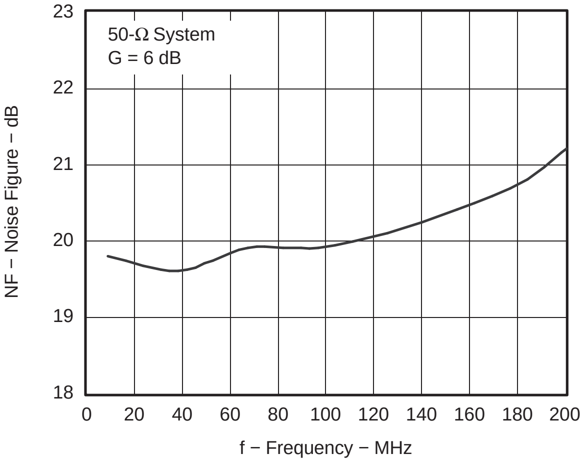
NOISE FIGURE vs FREQUENCY

**Figure 24.**

QUIESCENT CURRENT vs SUPPLY VOLTAGE

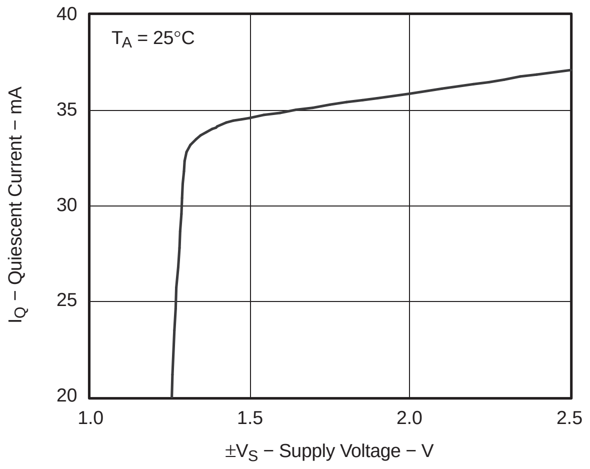

Figure 25.

POWERDOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

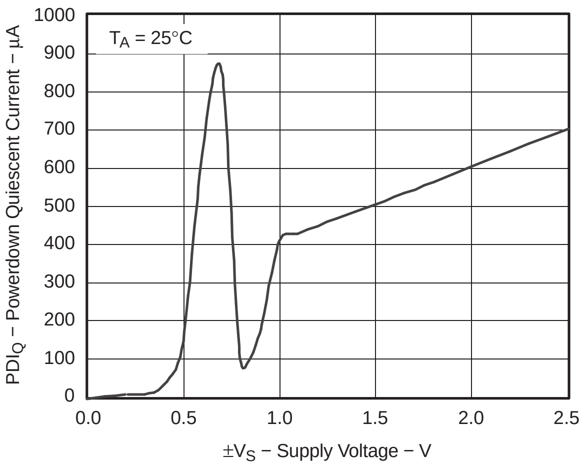

Figure 26.

OUTPUT BALANCE ERROR RESPONSE vs FREQUENCY

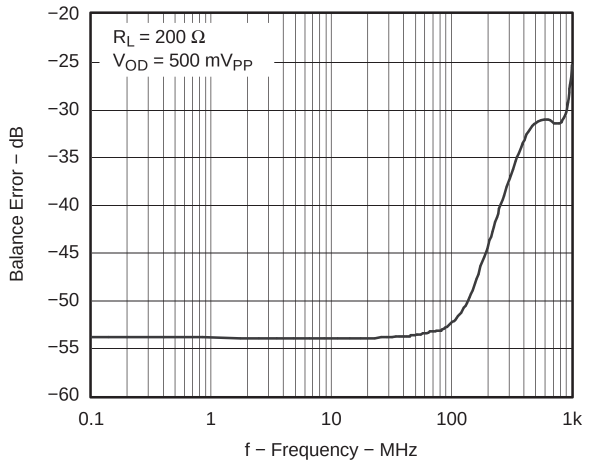

Figure 27.

CM INPUT BIAS CURRENT vs CM INPUT VOLTAGE

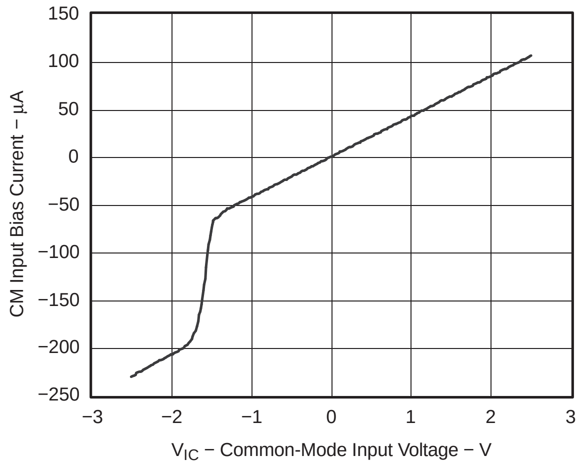

Figure 28.

DIFFERENTIAL OUTPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

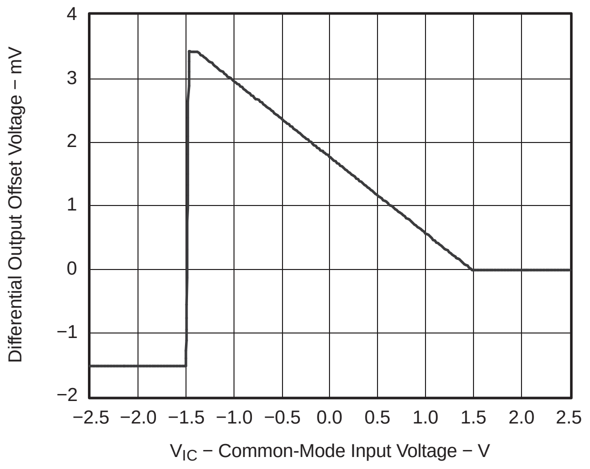

Figure 29.

COMMON-MODE OUTPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

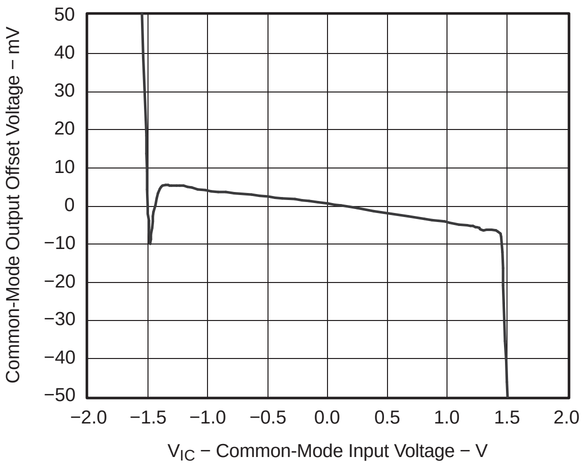

Figure 30.

## TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 3$ V

Test conditions unless otherwise noted: $V_{S+} = +1.5$ V, $V_{S-} = -1.5$ V, CM = open, $V_{OD} = 1$ Vpp, $R_F = 348\ \Omega$, $R_L = 200\ \Omega$ Differential, G = 14 dB, Single-Ended Input, Input and Output Referenced to Mid-Supply

| | | | |
|---|---|---|---|
| Small-Signal Frequency Response | G = 6 dB, $V_{OD} = 100\ mV_{PP}$ | | Figure 31 |
| | G = 10 dB, $V_{OD} = 100\ mV_{PP}$ | | Figure 32 |
| | G = 14 dB, $V_{OD} = 100\ mV_{PP}$ | | Figure 33 |
| Large Signal Frequency Response | G = 6 dB, $V_{OD} = 1\ V_{PP}$ | | Figure 34 |
| | G = 10 dB, $V_{OD} = 1\ V_{PP}$ | | Figure 35 |
| | G = 14 dB, $V_{OD} = 1\ V_{PP}$ | | Figure 36 |
| Harmonic Distortion | $HD_2$, G = 14 dB, $V_{OD} = 1\ V_{PP}$ | vs Frequency | Figure 37 |
| | $HD_3$, G = 14 dB, $V_{OD} = 1\ V_{PP}$ | vs Frequency | Figure 38 |
| | $HD_2$, G = 14 dB | vs Output Voltage | Figure 39 |
| | $HD_3$, G = 14 dB | vs Output Voltage | Figure 40 |
| Intermodulation Distortion | $IMD_2$, G = 14dB | vs Frequency | Figure 41 |
| | $IMD_3$, G = 14 dB | vs Frequency | Figure 42 |
| Output Intercept Point | $OIP_2$ | vs Frequency | Figure 43 |
| | $OIP_3$ | vs Frequency | Figure 44 |
| Transition Rate | | vs Output Voltage | Figure 45 |
| Transient Response | | | Figure 46 |
| Rejection Ratio | | vs Frequency | Figure 47 |
| Output Voltage Swing | | vs Load Resistance | Figure 48 |
| Turn-Off Time | | | Figure 49 |
| Turn-On Time | | | Figure 50 |
| Noise Figure | | vs Frequency | Figure 51 |
| Output Balance Error | | vs Frequency | Figure 52 |
| Differential Output Offset Voltage | | vs CM Input Voltage | Figure 53 |
| Output Common-Mode Offset | | vs CM Input Voltage | Figure 54 |

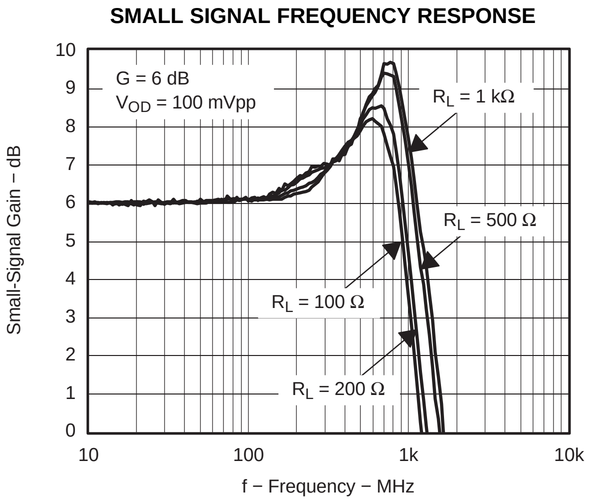

**Figure 31.**

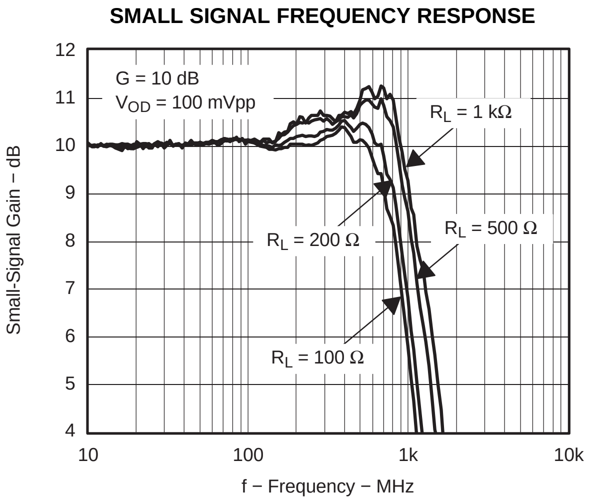

**Figure 32.**

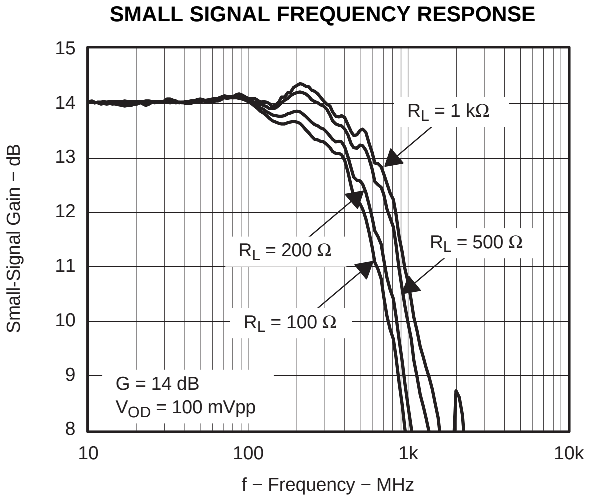

**Figure 33.**

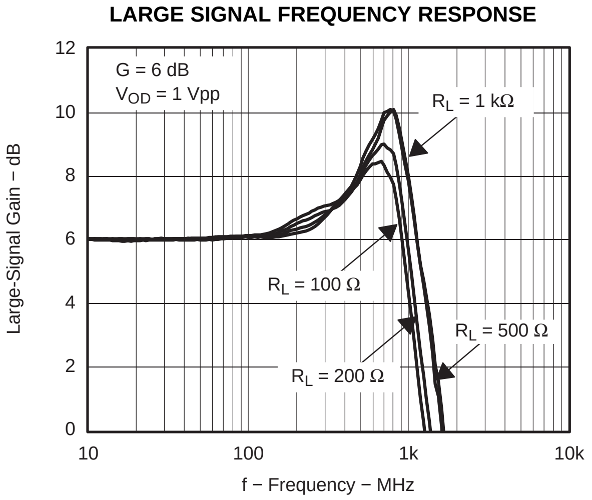

**Figure 34.**

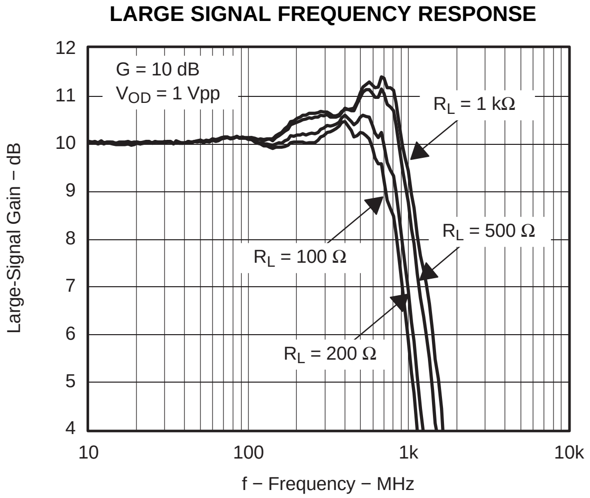

**Figure 35.**

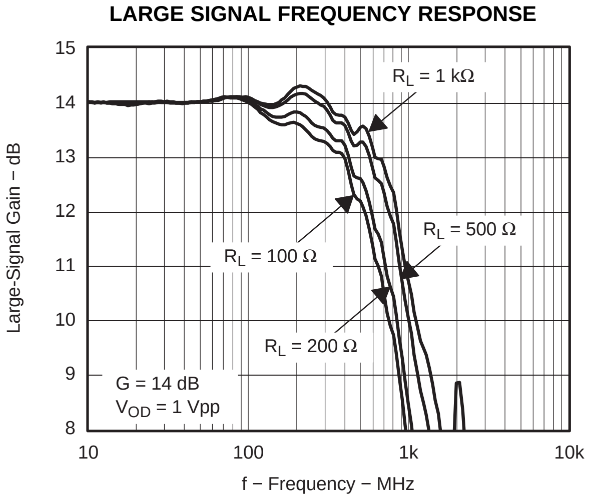

**Figure 36.**

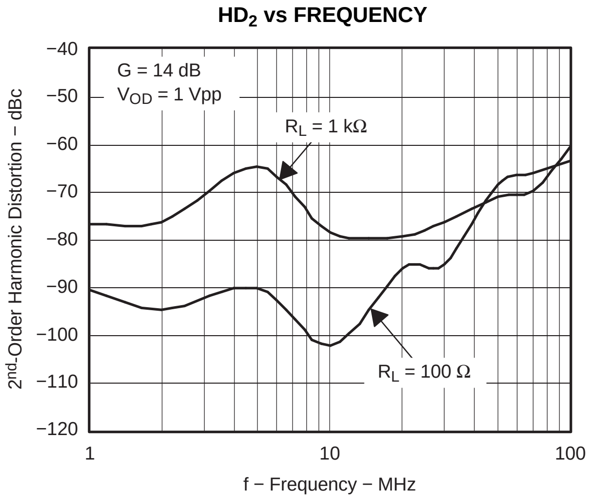

**Figure 37.**

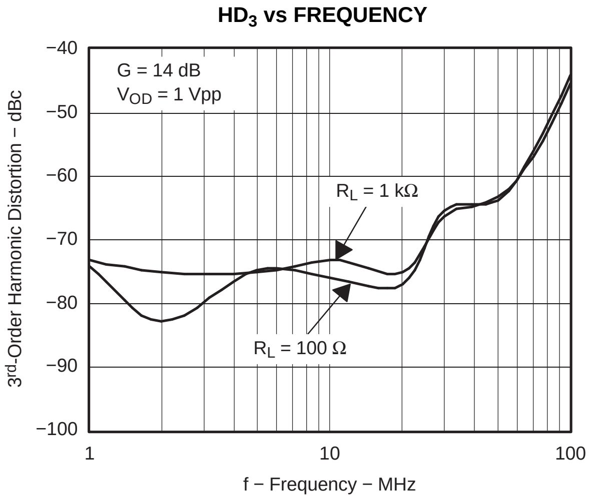

**Figure 38.**

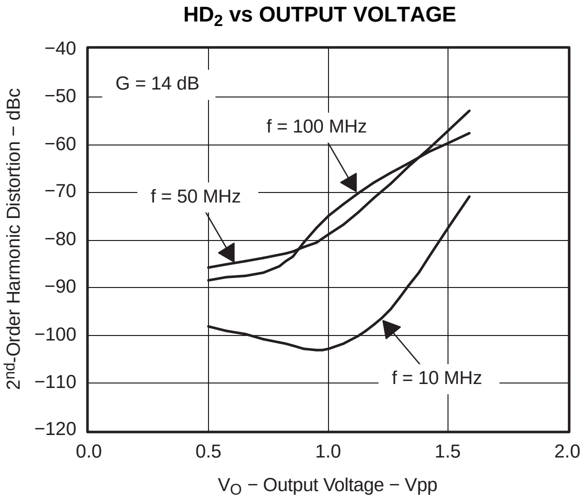
$HD_2$ vs OUTPUT VOLTAGE

**Figure 39.**

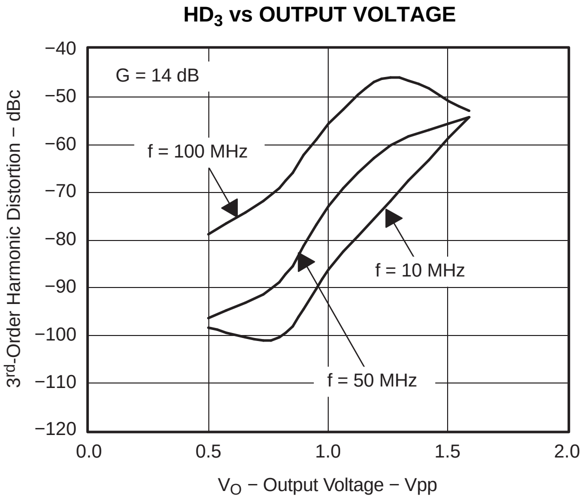
$HD_3$ vs OUTPUT VOLTAGE

**Figure 40.**

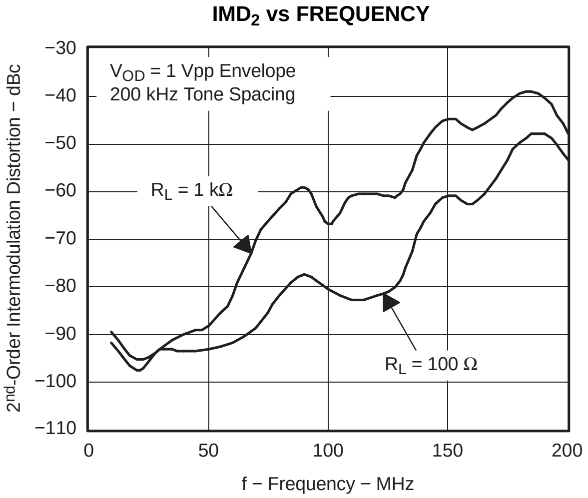
$IMD_2$ vs FREQUENCY

**Figure 41.**

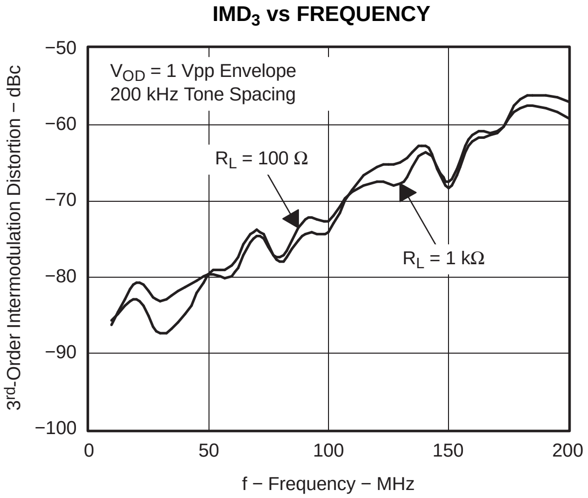
$IMD_3$ vs FREQUENCY

**Figure 42.**

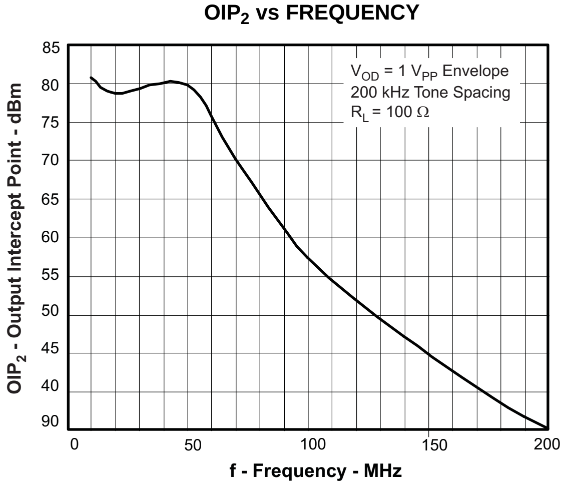
$OIP_2$ vs FREQUENCY

**Figure 43.**

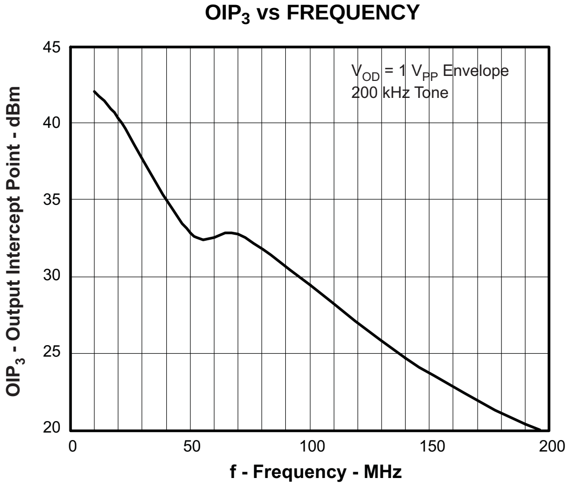
$OIP_3$ vs FREQUENCY

**Figure 44.**

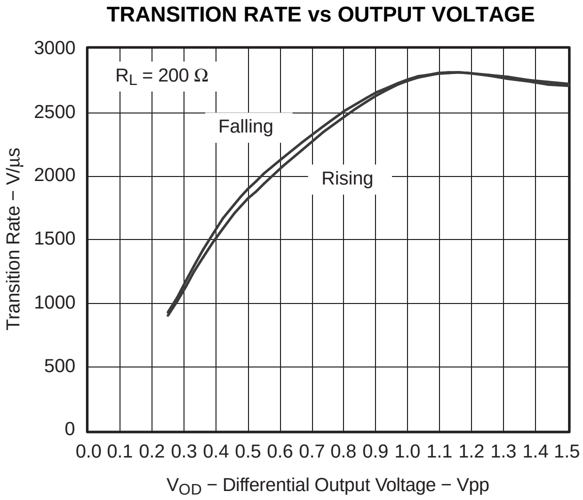

Figure 45.

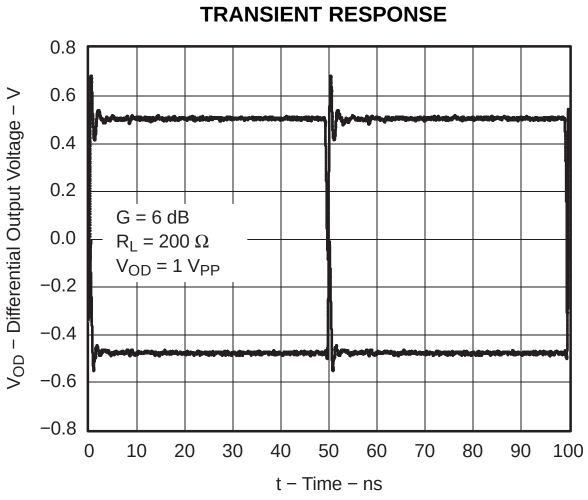

Figure 46.

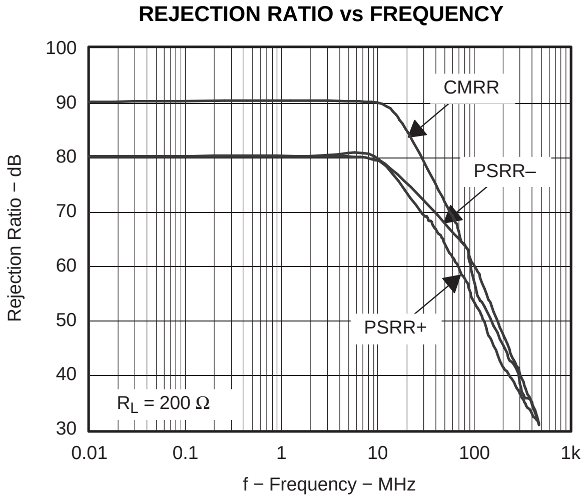

Figure 47.

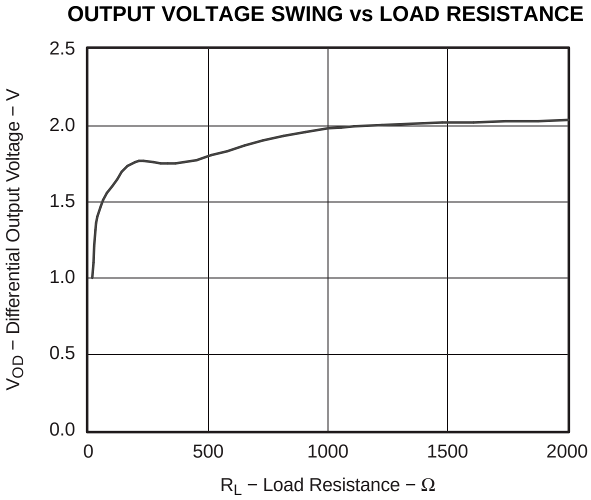

Figure 48.

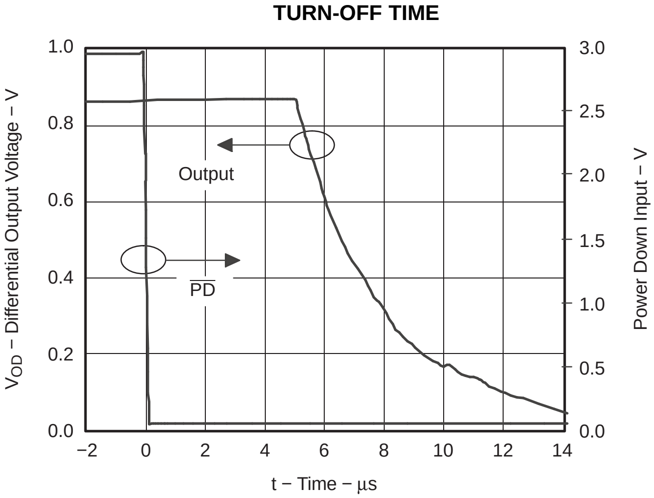

Figure 49.

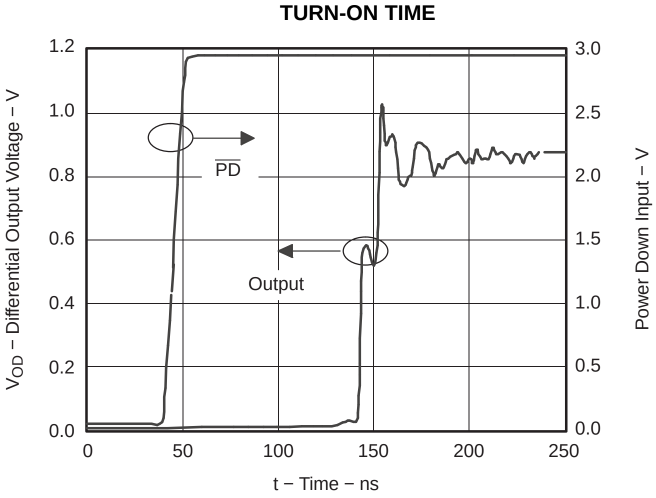

Figure 50.

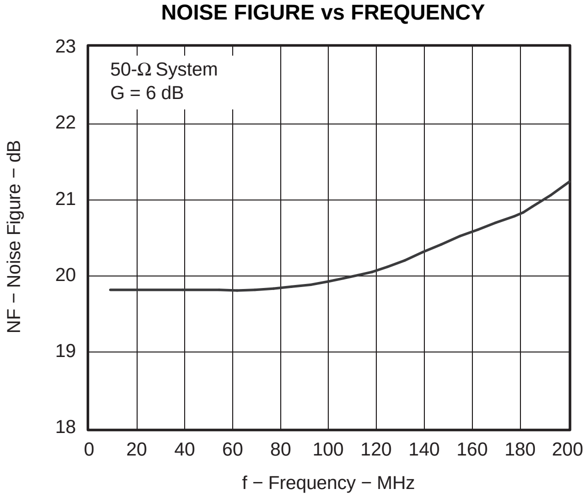

Figure 51.

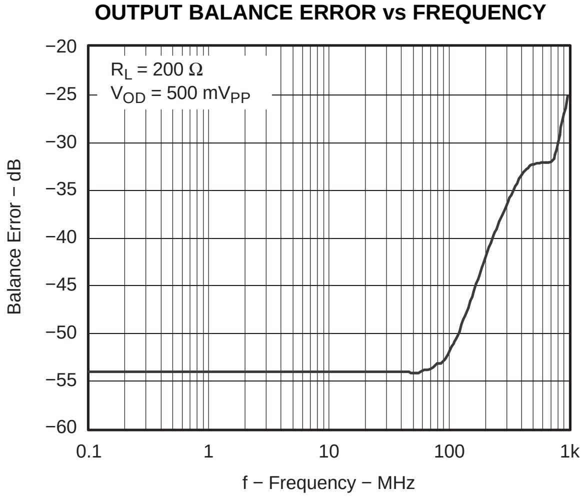

Figure 52.

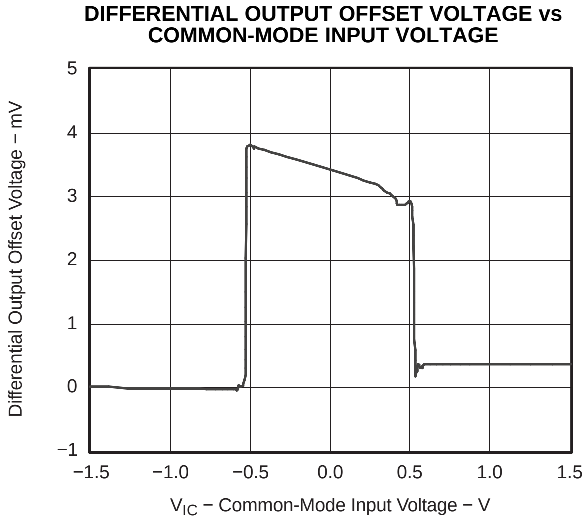

Figure 53.

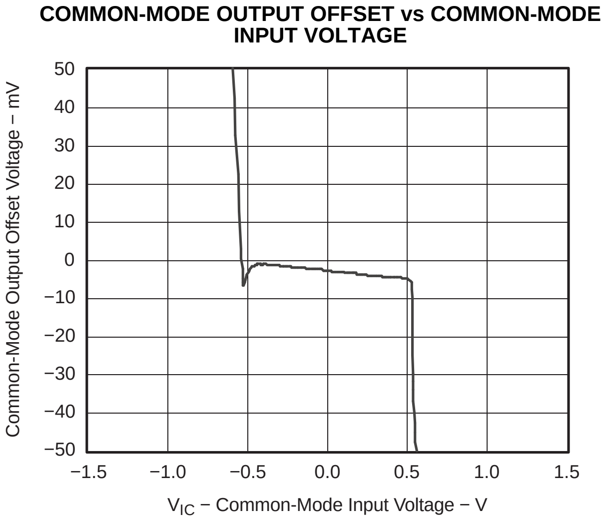

Figure 54.

## TEST CIRCUITS

The THS4513 is characterized with the following test circuits. For simplicity, power supply decoupling is not shown – see layout in the *Application Information* section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac coupled 50 Ω sources and a 0.22 μF capacitor and a 49.9 Ω resistor to ground are inserted across $R_{IT}$ on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single-supply as described in the *Application Information* section with no impact on performance.

**Table 1. Gain Component Values**

| GAIN | $R_F$ | $R_G$ | $R_{IT}$ |
|---|---|---|---|
| 6 dB | 348 Ω | 165 Ω | 61.9 Ω |
| 10 dB | 348 Ω | 100 Ω | 69.8 Ω |
| 14 dB | 348 Ω | 56.2 Ω | 88.7 Ω |
| 20 dB | 348 Ω | 16.5 Ω | 287 Ω |

**Note: the gain setting includes 50 Ω source impedance. Components are chosen to achieve gain and 50 Ω input termination.**

**Table 2. Load Component Values**

| $R_L$ | $R_O$ | $R_{OT}$ | Atten |
|---|---|---|---|
| 100 Ω | 25 Ω | open | 6 dB |
| 200 Ω | 86.6 Ω | 69.8 Ω | 16.8 dB |
| 499 Ω | 237 Ω | 56.2 Ω | 25.5 dB |
| 1k Ω | 487 Ω | 52.3 Ω | 31.8 dB |

**Note: the total load includes 50 Ω termination by the test equipment. Components are chosen to achieve load and 50 Ω line termination through a 1:1 transformer.**

Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 56, the signal will see slightly more loss, and these numbers will be approximate.

### Frequency Response

The circuit shown in Figure 55 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. $R_{IT}$ and $R_G$ are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22 μF capacitor and 49.9 Ω resistor to ground are inserted across $R_{IT}$ on the alternate input.

The output is probed using a high-impedance differential probe across the 100 Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

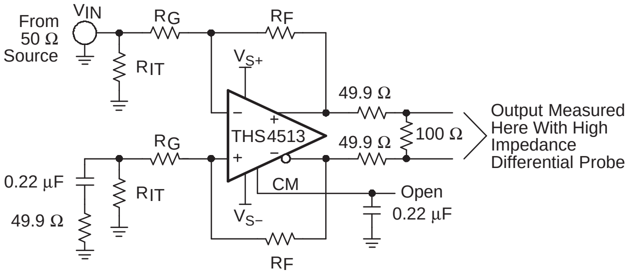

**Figure 55. Frequency Response Test Circuit**

### Distortion

The circuit shown in Figure 56 is used to measure harmonic distortion and intermodulation distortion of the amplifier. A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. $R_{IT}$ and $R_G$ are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22 μF capacitor and 49.9 Ω resistor to ground are inserted across $R_{IT}$ on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

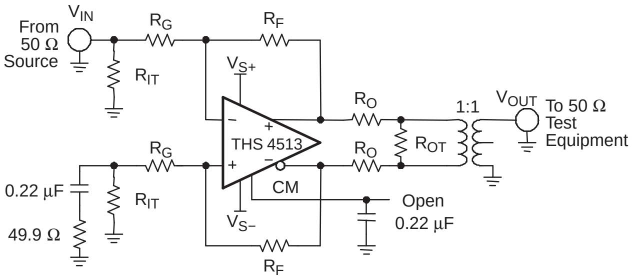

**Figure 56. Distortion Test Circuit**

### Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Off Time

The circuit shown in Figure 57 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at $V_{OUT}$ with $V_{IN}$ left open, and the drop across the 49.9 Ω resistor is used to calculate the impedance seen looking into the amplifier's output.

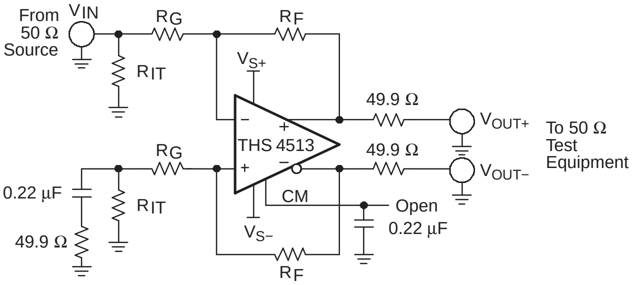

Figure 57. SR, Transient Response, Settling Time, $Z_O$, Overdrive Recovery, $V_{OUT}$ Swing, and Turn-On/Off Test Circuit

### CM Input

The circuit shown in Figure 58 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at $V_{OUT+}$ or $V_{OUT-}$ with the input injected at $V_{IN}$, $R_{CM}$ = 0 Ω and $R_{CMT}$ = 49.9 Ω. The input impedance is measured with $R_{CM}$ = 49.9 Ω with $R_{CMT}$ = open, and calculated by measuring the voltage drop across $R_{CM}$ to determine the input current.

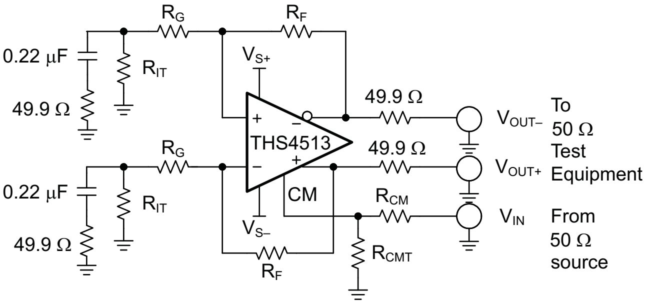

Figure 58. CM Input Test Circuit

### CMRR and PSRR

The circuit shown in Figure 59 is used to measure the CMRR and PSRR of $V_{S+}$ and $V_{S-}$. The input is switched appropriately to match the test being performed.

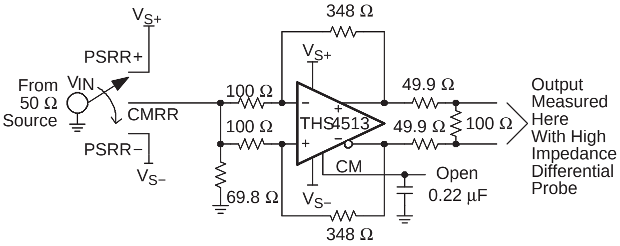

Figure 59. CMRR and PSRR Test Circuit

# APPLICATION INFORMATION

## APPLICATIONS

The following circuits show application information for the THS4513. For simplicity, power supply decoupling capacitors are not shown in these diagrams. Please see the THS4513 EVM section for recommendations. For more detail on the use and operation of fully differential op amps refer to application report *Fully-Differential Amplifiers* (SLOA054) .

### Differential Input to Differential Output Amplifier

The THS4513 is a fully differential op amp and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 60 (CM input not shown). The gain of the circuit is set by $R_F$ divided by $R_G$.

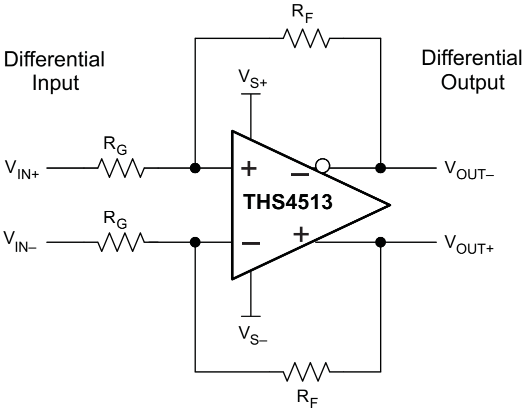

**Figure 60. Differential Input to Differential Output Amplifier**

Depending on the source and load, input and output termination can be accomplished by adding $R_{IT}$ and $R_O$.

### Single-Ended Input to Differential Output Amplifier

The THS4513 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 61 (CM input not shown). The gain of the circuit is again set by $R_F$ divided by $R_G$.

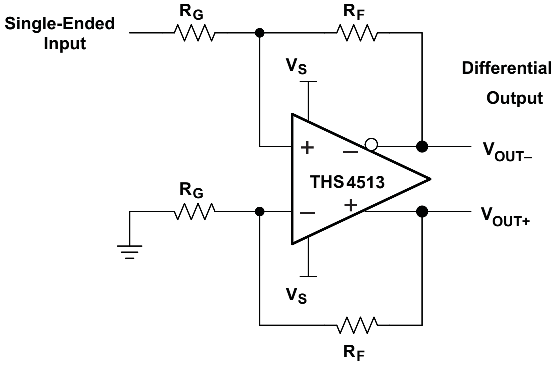

**Figure 61. Single-Ended Input to Differential Output Amplifier**

### Input Common-Mode Voltage Range

The input common-mode voltage of a fully differential op amp is the voltage at the '+' and '–' input pins of the op amp.

It is important to not violate the input common-mode voltage range ($V_{ICR}$) of the op amp. Assuming the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin will determine the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F}\right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F}\right) \quad (1)$$

To determine the $V_{ICR}$ of the op amp, the voltage at the negative input is evaluated at the extremes of $V_{OUT+}$.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

### Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 3 mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4 mV differential offset voltage. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 62 is representative of the CM input. The internal CM circuit has about 700 MHz of –3 dB bandwidth, which is required for best performance, but it is intended to be a DC bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - \left(V_{S+} - V_{S-}\right)}{50\ k\Omega} \qquad (2)$$

where $V_{CM}$ is the voltage applied to the CM pin.

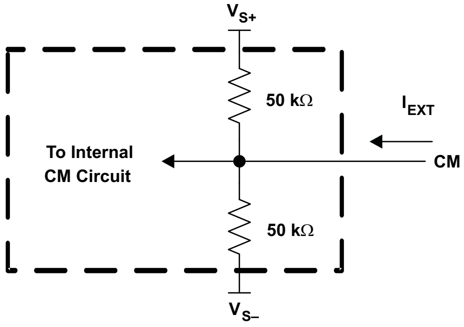

Figure 62. CM Input Circuit

## Single-Supply Operation (3 V to 5 V)

To facilitate testing with common lab equipment, the THS4513 EVM allows split-supply operation, and the characterization data presented in this data sheet was taken with split-supply power inputs. The device easily can be used with a single-supply power input without degrading the performance. Figure 63, Figure 64, and Figure 65 show DC and AC-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to mid-supply allowing for optimum performance. The information presented here also can be applied to differential input sources.

In Figure 63, the signal source is referenced to a voltage derived from the CM pin via a unity-gain wideband buffer such as the BUF602. $V_{CM}$ is set to mid-supply by THS4513 internal circuitry. $R_T$ along with the input impedance of the amplifier provides input termination, which also is referenced to $V_{CM}$.

Note that $R_S$ and $R_T$ are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value $R_G + R_S || R_T$ on this input. This is also true of the circuits shown in Figure 64 and Figure 65.

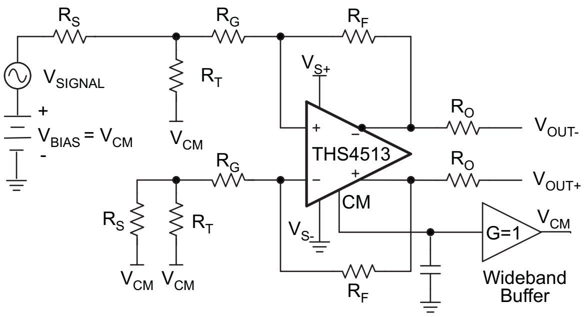

Figure 63. THS4513 DC Coupled Single-Supply with Input Biased to $V_{CM}$

In Figure 64 the source is referenced to ground and so is the input termination resistor. $R_{PU}$ is added to the circuit to avoid violating the $V_{ICR}$ of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} = \frac{\left(V_{IC} - V_{S+}\right)}{V_{CM}\left(\frac{1}{R_F}\right) - V_{IC}\left(\frac{1}{R_{IN}} + \frac{1}{R_F}\right)} \qquad (3)$$

$V_{IC}$ is the desired input common-mode voltage, $V_{CM}$ = CM, and $R_{IN} = R_G + R_S || R_T$. To set to mid-supply, make the value of $R_{PU} = R_G + R_S || R_T$.

Table 3 is a modification of Table 1 to add the proper values with $R_{PU}$ assuming a 50 Ω source impedance and setting the input and output common-mode voltage to mid-supply.

There are two drawbacks to this configuration. One is that it requires additional current from the power supply. Using the values shown for a gain of 10 dB requires 37 mA more current with 5 V supply, and 22 mA more current with 3 V supply.

The other drawback is this configuration also increases the noise gain of the circuit. In the 10 dB gain case, noise gain increases by a factor of 1.5.

Table 3. RPU Values for Various Gains

| Gain | $R_F$ | $R_G$ | $R_{IT}$ | $R_{PU}$ |
|---|---|---|---|---|
| 6 dB | 348 Ω | 169 Ω | 64.9 Ω | 200 Ω |
| 10 dB | 348 Ω | 102 Ω | 78.7 Ω | 133 Ω |
| 14 dB | 348 Ω | 61.9 Ω | 115 Ω | 97.6 Ω |
| 20 dB | 348 Ω | 40.2 Ω | 221 Ω | 80.6 Ω |

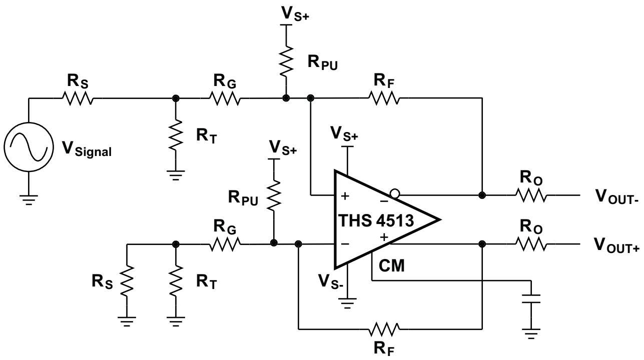

Figure 64. THS4513 DC Coupled Single-Supply With $R_{PU}$ Used to Set $V_{IC}$

Figure 65 shows AC coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self-bias both input and output to mid-supply.

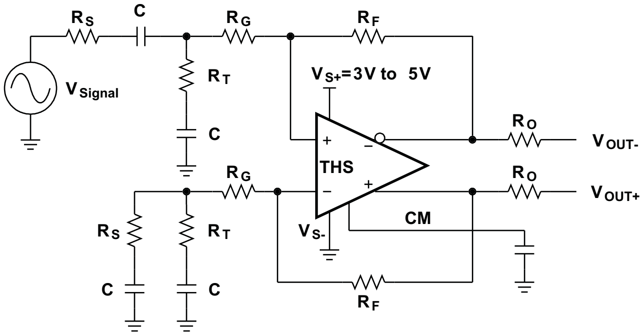

Figure 65. THS4513 AC Coupled Single-Supply

### THS4513 + ADS5500 Combined Performance

The THS4513 is designed to be a high-performance drive amplifier for high-performance data converters like the ADS5500 14 bit 125 MSPS ADC. Figure 66 shows a circuit combining the two devices. The THS4513 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5500. The 100 Ω resistors and 2.7 pF capacitor between the THS4513 outputs and ADS5500 inputs, along with the input capacitance of the ADS5500, limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an AC-coupled 50 Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8 Ω resistor and 0.22 μF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22 μF capacitor and 49.9 Ω resistor is inserted to ground across the 69.8 Ω resistor and 0.22 μF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348 Ω feedback resistor. Refer to Table 3 for component values to set proper 50 Ω termination for other common gains. A split power supply of 4 V and –1 V is used to set the input and output common-mode voltages to approximately mid-supply while setting the input common-mode of the ADS5500 to the recommended 1.55 V. This maintains maximum headroom on the internal transistors of the THS4513 to ensure optimum performance.

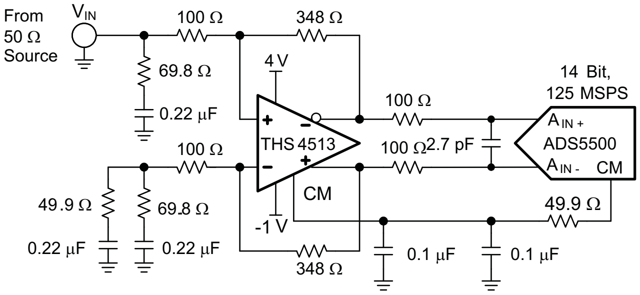

Figure 66. THS4513 + ADS5500 Circuit

Figure 67 shows the 2-tone FFT of the THS4513 + ADS5500 circuit with 65 MHz and 70 MHz input frequencies. The SFDR is 90 dBc.

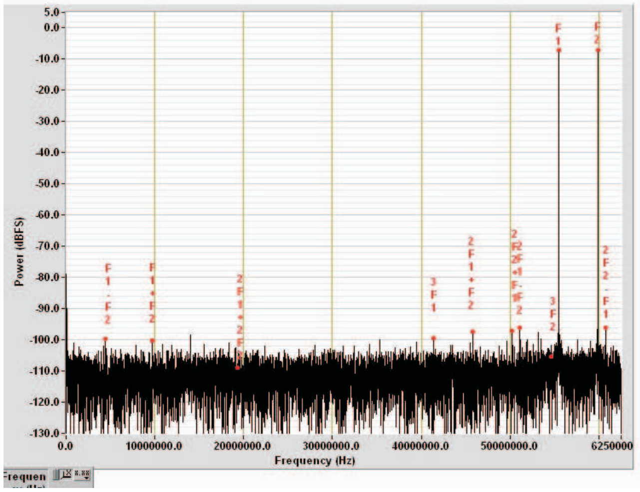

Figure 67. THS4513 + ADS5500 2-Tone FFT With 65 MHz and 70 MHz Input

### THS4513 + ADS5424 Combined Performance

Figure 68 shows the THS4513 driving the ADS5424 ADC.

The THS4513 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4513 + ADS5500 circuit.

The 225 Ω resistors and 2.7 pF capacitor between the THS4513 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (–3 dB).

Because the ADS5424s recommended input common-mode voltage is 2.4 V, the THS4513 is operated from a single power supply input with $V_{S+}$ = 5 V and $V_{S-}$ = 0 V (ground).

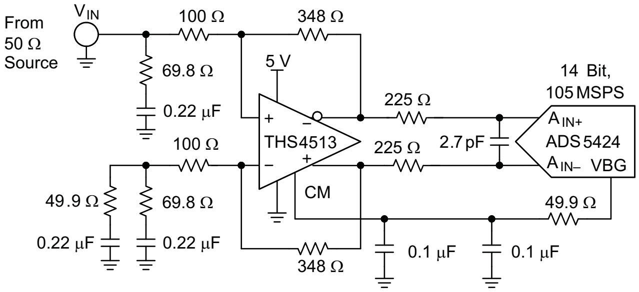

Figure 68. THS4513 + ADS5424 Circuit

### Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the opamp circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10 μF and two 0.1 μF power-supply decoupling capacitors should be placed as near the power-supply pins as possible.
6. Two 0.1 μF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.

## THS4513 EVM

Figure 69 is the THS4513 EVAL1 EVM schematic for the plastic QFN (RGT) package. Layers 1 through 4 of the PCB are shown in Figure 70, and Table 4 is the bill of materials for the EVM as supplied from TI. The same layout recommendations should be followed for the THS4513 ceramic flatpack devices. Contact your TI representative for availability of the THS4513 EVM.

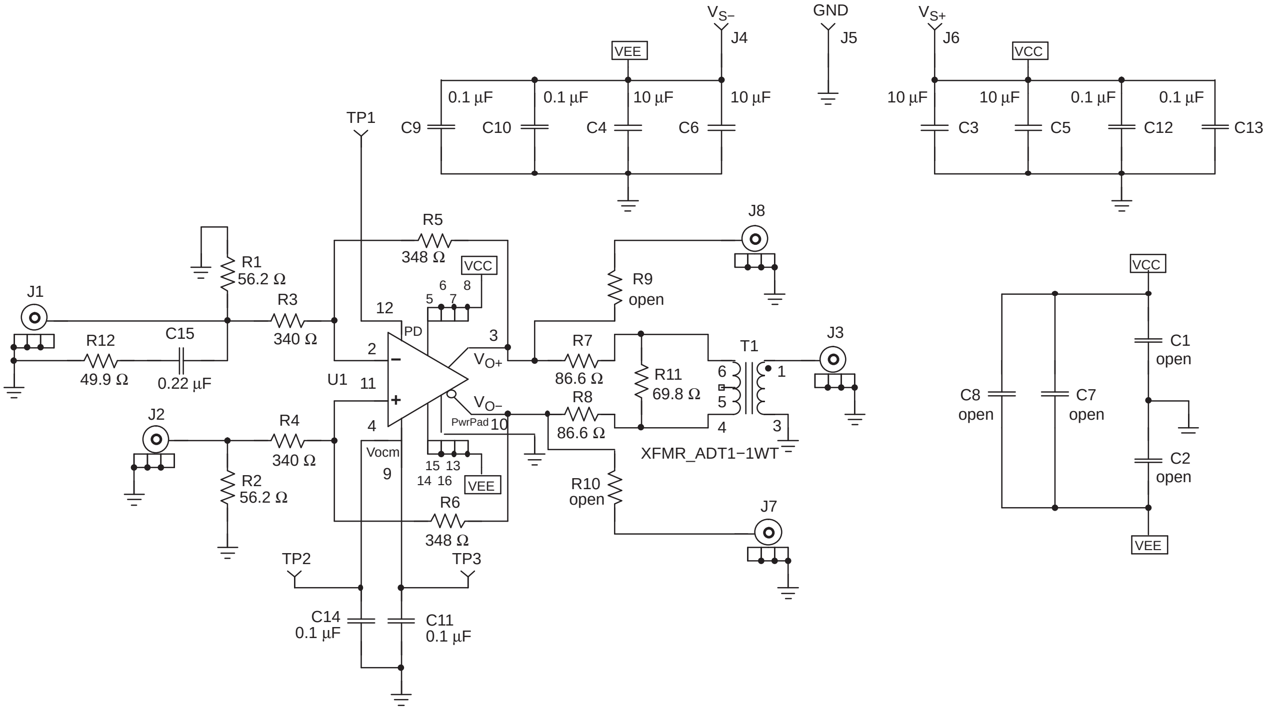

Figure 69. THS4513 EVAL1 EVM Schematic

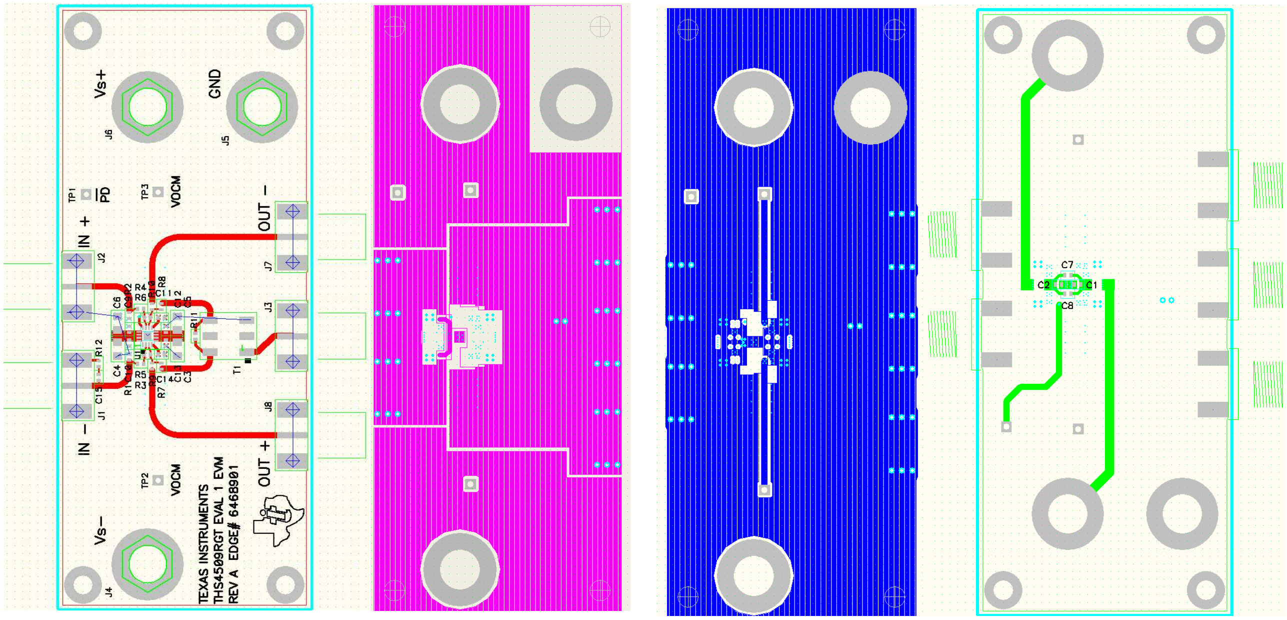

Figure 70. THS4513 EVAL1 EVM Layer 1 Through 4

### Table 4. THS4513 EVAL1 EVM Bill of Materials

| ITEM | DESCRIPTION | SMD SIZE | REFERENCE DESIGNATOR | PCB QTY | MANUFACTURER'S PART NUMBER |
|---|---|---|---|---|---|
| 1 | CAP, 10.0 µF, Ceramic, X5R, 6.3 V | 0805 | C3, C4, C5, C6 | 4 | (AVX) 08056D106KAT2A |
| 2 | CAP, 0.1 µF, Ceramic, X5R, 10 V | 0402 | C9, C10, C11, C12, C13, C14 | 6 | (AVX) 0402ZD104KAT2A |
| 3 | CAP, 0.22 µF, Ceramic, X5R, 6.3 V | 0402 | C15 | 1 | (AVX) 04026D224KAT2A |
| 4 | OPEN | 0402 | C1, C2, C7, C8 | 4 | |
| 5 | OPEN | 0402 | R9, R10 | 2 | |
| 6 | Resistor, 49.9 Ω, 1/16W, 1% | 0402 | R12 | 1 | (KOA) RK73H1ETTP49R9F |
| 7 | Resistor, 56.2 Ω, 1/16W, 1% | 0402 | R1,R2 | 2 | (KOA) RK73H1ETTP56R2F |
| 8 | Resistor, 69.8 Ω, 1/16W, 1% | 0402 | R11 | 1 | (KOA) RK73H1ETTP69R8F |
| 9 | Resistor, 86.6 Ω, 1/16W, 1% | 0402 | R7, R8 | 2 | (KOA) RK73H1ETTP86R6F |
| 10 | Resistor, 340 Ω, 1/16W, 1% | 0402 | R3, R4 | 2 | (KOA) RK73H1ETTP3400F |
| 11 | Resistor, 348 Ω, 1/16W, 1% | 0402 | R5, R6 | 2 | (KOA) RK73H1ETTP3480F |
| 12 | Transformer, RF | | T1 | 1 | (MINI-CIRCUITS) ADT1-1WT |
| 13 | Jack, banana receptance, 0.25" diameter hole | | J4, J5, J6 | 3 | (HH SMITH) 101 |
| 14 | OPEN | | J1, J7, J8 | 3 | |
| 15 | Connector, edge, SMA PCB Jack | | J2, J3 | 2 | (JOHNSON) 142-0701-801 |
| 16 | Test point, Red | | TP1, TP2, TP3 | 3 | (KEYSTONE) 5000 |
| 17 | IC, THS4513 | | U1 | 1 | (TI) THS4513RGT |
| 18 | Standoff, 4-40 HEX, 0.625" length | | | 4 | (KEYSTONE) 1808 |
| 19 | Screw, Phillips, 4-40, 0.250" | | | 4 | SHR-0440-016-SN |
| 20 | Printed circuit board | | | 1 | (TI) EDGE# 6475514 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-0722301VFA | ACTIVE | CFP | HKT | 16 | 1 | RoHS & Green | Call TI | N / A for Pkg Type | -55 to 125 | 5962-0722301VF<br>A<br>THS4513M | Samples |
| THS4513HKT/EM | ACTIVE | CFP | HKT | 16 | 1 | RoHS & Green | Call TI | N / A for Pkg Type | 25 to 25 | THS4513HKT/EM<br>EVAL ONLY | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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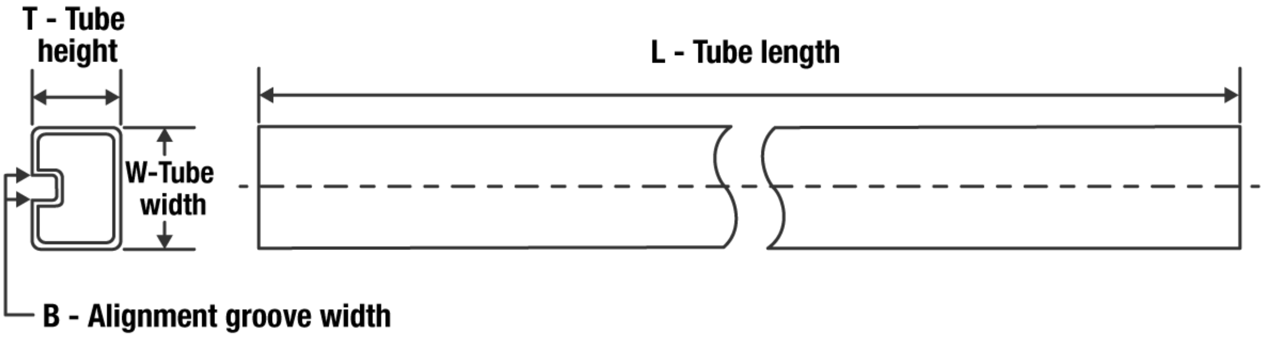
**OTHER QUALIFIED VERSIONS OF THS4513-SP :**

- Catalog : THS4513

NOTE: Qualified Version Definitions:

  - Catalog - TI's standard catalog product

## TUBE



*All dimensions are nominal

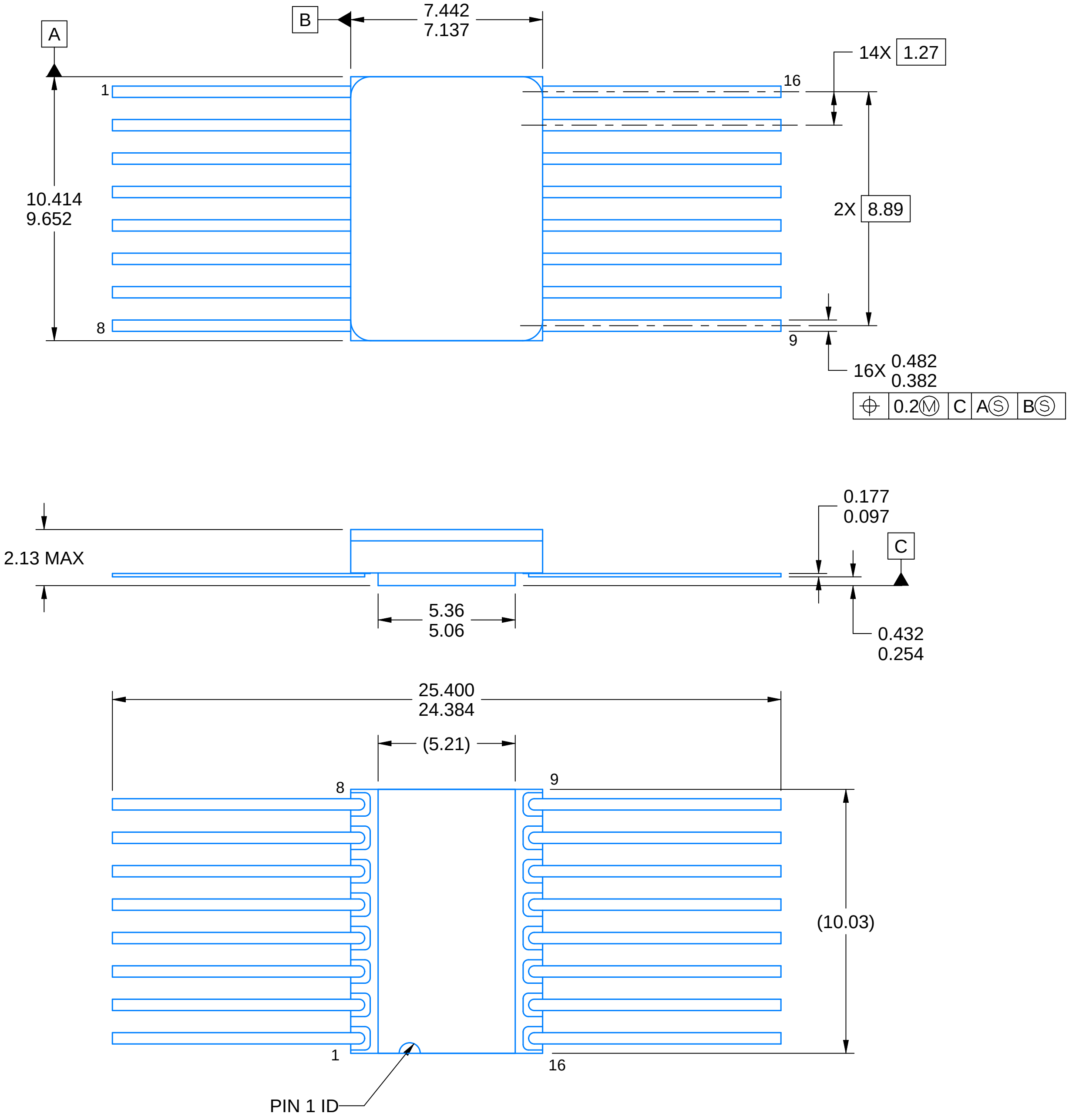
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-0722301VFA | HKT | CFP (HSL) | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| THS4513HKT/EM | HKT | CFP (HSL) | 16 | 1 | 506.98 | 26.16 | 6220 | NA |

# HKT0016A

# PACKAGE OUTLINE

## CFP - 2.13 mm max height

CERAMIC DUAL FLATPACK



4221021/B 06/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid and cavity are electrically isolated
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

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