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Vishay Siliconix

# N-Channel 100 V (D-S) MOSFET



PRODUCT SUMMARY					
V <sub>DS</sub> (V)	100				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0040				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.0045				
Q <sub>g</sub> typ. (nC)	84				
I <sub>D</sub> (A)	150 <sup>d</sup>				
Configuration	Single				

#### **FEATURES**

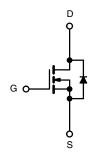
- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature



- $\bullet$  Very low  $Q_{gd}$  reduces power loss from passing through  $V_{\text{plateau}}$
- 100 % R<sub>a</sub> and UIS tested
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912">www.vishay.com/doc?99912</a>

### **APPLICATIONS**

- Switching power supply
- DC/DC converter
- Power tools
- · Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing / e-fuse



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free and halogen-free	SUP70042E-GE3

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage		V <sub>DS</sub>	100	V	
Gate-source voltage		$V_{GS}$	± 20		
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	1	150 <sup>d</sup>	A	
	T <sub>C</sub> = 70 °C	- I <sub>D</sub>	139		
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	200	A	
Avalanche current		I <sub>AS</sub>	50		
Single avalanche energy <sup>a</sup> L = 0.1 mH		E <sub>AS</sub>	125	mJ	
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	Pn	278 b	- w	
	T <sub>C</sub> = 125 °C		178 <sup>b</sup>		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction-to-ambient (PCB mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-case (drain)	R <sub>thJC</sub>	0.55	- C/VV	

#### Notes

- a. Duty cycle ≤ 1 %
- b. See SOA curve for voltage derating
- c. When mounted on 1" square PCB (FR4 material)
- d. Package limited



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = 10 \text{ mA}$	100	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	-	4	4 V	
Gate-body leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	=	-	± 250	nA	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	-	-	1		
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	150	- μA	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	5	mA	
On-state drain current a	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	50	-	-	Α	
<b>D</b>	_	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	0.0033	0.0040	Ω	
Drain-source on-state resistance a	R <sub>DS(on)</sub>	V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 15 A	=	0.0036	0.0045		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	-	60	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	6490	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}$	-	570	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	20	-		
Total gate charge <sup>c</sup>	Qg		-	84	110		
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	33.5	-	nC	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	9.5	-		
Gate resistance	Rg	f = 1 MHz	0.26	1.3	2.6	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>		-	25	50		
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega$	-	18	36		
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	45	90	ns	
Fall time <sup>c</sup>	t <sub>f</sub>		-	14	28		
Drain-Source Body Diode Ratings and Characteristics <sup>b</sup> (T <sub>C</sub> = 25 °C)							
Pulsed current (t = 100 μs)	I <sub>SM</sub>		-	-	200	Α	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V	1	0.8	1.5	V	
Reverse recovery time	t <sub>rr</sub>		1	58	116	ns	
Peak reverse recovery charge	I <sub>RM(REC)</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs	-	3.9	5.9	Α	
Reverse recovery charge	Q <sub>rr</sub>		-	126	189	μC	
Reverse recovery fall time	ta		-	42	-	ns	
Reverse recovery rise time	t <sub>b</sub>		-	16	-	119	

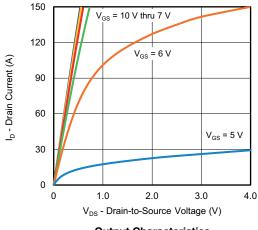
#### **Notes**

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

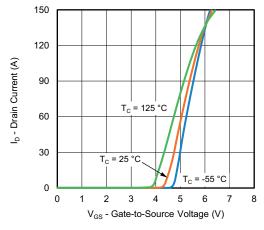
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



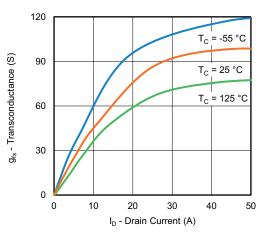
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



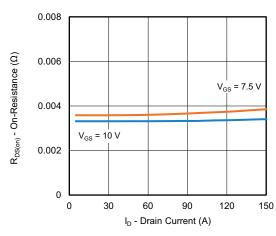
### **Output Characteristics**



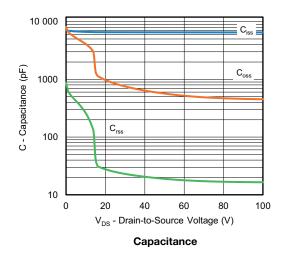
**Transfer Characteristics** 

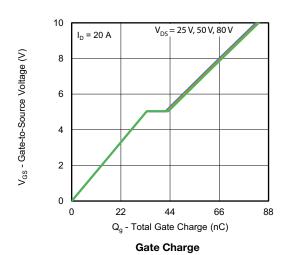


Transconductance



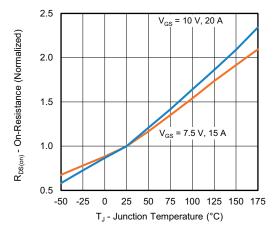
On-Resistance vs. Drain Current



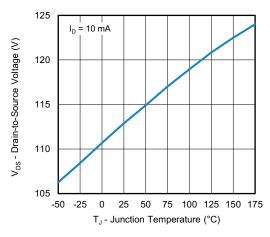




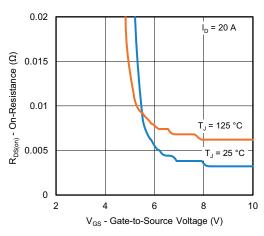
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



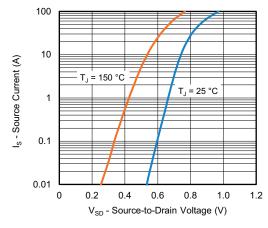
On-Resistance vs. Junction Temperature



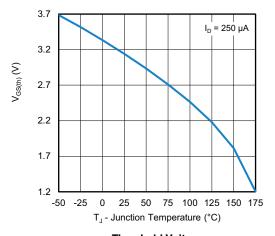
**Drain Source Breakdown vs. Junction Temperature** 



On-Resistance vs. Gate-to-Source Voltage



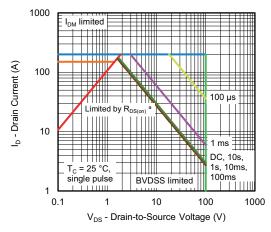
Source Drain Diode Forward Voltage



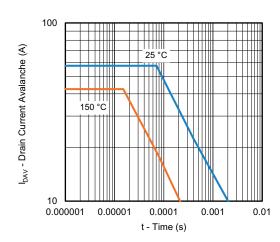
Threshold Voltage



### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



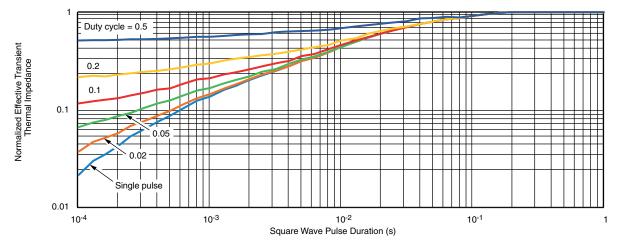
Safe Operating Area



Single Pulse Avalanche Current Capability vs. Time

#### Note

a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?63051">www.vishay.com/ppg?63051</a>.



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## **TO-220AB**



	D2

	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
С	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
Е	10.04	10.51	0.395	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
ØΡ	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: T14-0413-Rev. P, 16-Jun-14 DWG: 5471				

### Note

 $<sup>^{\</sup>star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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