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Vishay Siliconix

# N-Channel 200 V (D-S) MOSFET



PRODUCT SUMMARY						
V <sub>DS</sub> (V)	200					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = 10 V	0.0114					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.0129					
Q <sub>g</sub> typ. (nC)	56.7					
I <sub>D</sub> (A)	150 <sup>d</sup>					
Configuration	Single					

#### **FEATURES**

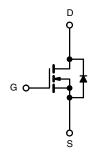
- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature



- $\bullet$  Very low  $Q_{gd}$  reduces power loss from passing through  $V_{\text{plateau}}$
- 100 % R<sub>a</sub> and UIS tested
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

### **APPLICATIONS**

- Switching power supply
- DC/DC converter
- Power tools
- · Motor drive switch
- DC/AC inverter
- · Battery management
- OR-ing / e-fuse



N-Channel MOSFET

ORDERING INFORMATION			
Package	TO-263		
Lead (Pb)-free and halogen-free	SUM90100E-GE3		

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-source voltage	Drain-source voltage			V		
Gate-source voltage		$V_{GS}$	± 20	V		
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	150 <sup>d</sup>			
	T <sub>C</sub> = 70 °C		150 <sup>d</sup>	A		
Pulsed drain current (t = 100 μs)	I <sub>DM</sub>	250	^			
Avalanche current		I <sub>AS</sub>	70			
Single avalanche energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	245	mJ		
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	Pn	375 b	w		
	T <sub>C</sub> = 125 °C	] [	125 <sup>b</sup>	]		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-ambient (PCB mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W		
Junction-to-case (drain)	R <sub>thJC</sub>	0.4	G/VV		

#### Notes

- a. Duty cycle ≤ 1 %
- b. See SOA curve for voltage derating
- c. When mounted on 1" square PCB (FR4 material)
- d. Package limited



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	-	4	V	
Gate-body leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 250	nA	
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V	-	-	1	μА	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	150		
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	5	mA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	120	-	-	Α	
During a second of the second	_	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 16 A	-	0.0095	0.0114	Ω	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 13 A	-	0.0099	0.0129		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 13 A	-	85	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	3930	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}$	-	450	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	12	-		
Total gate charge <sup>c</sup>	Qg		-	72.8	110	nC	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$	-	19.4	-		
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	19.0	-		
Gate resistance	Rg	f = 1 MHz	0.7	3.5	7.0	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>		-	20	40		
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 80 \text{ V}, R_1 = 6.2 \Omega$	-	50	100		
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 13 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	60	120	ns	
Fall time <sup>c</sup>	t <sub>f</sub>		-	18	36		
Drain-Source Body Diode Ratings	and Characte	ristics <sup>b</sup> (T <sub>C</sub> = 25 °C)					
Pulsed current (t = 100 μs)	I <sub>SM</sub>		-	-	250	Α	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.8	1.5	V	
Reverse recovery time	t <sub>rr</sub>		-	118	177	ns	
Peak reverse recovery charge	I <sub>RM(REC)</sub>		-	9.4	14.1	Α	
Reverse recovery charge	Q <sub>rr</sub>	$I_F = 13 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$	-	0.632	0.948	μC	
Reverse recovery fall time	t <sub>a</sub>		-	94	-	ns	
Reverse recovery rise time	t <sub>b</sub>		-	24	-	110	

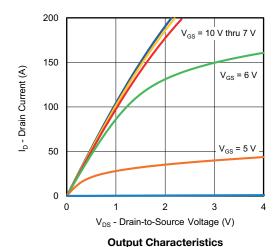
#### Notes

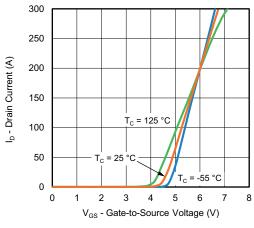
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

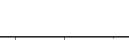
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



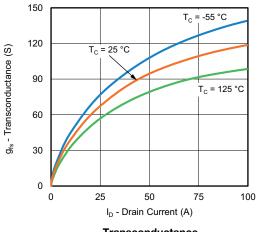
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

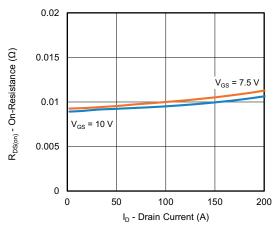






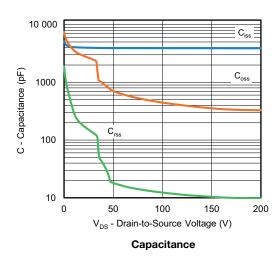


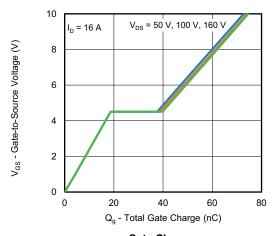




**Transconductance** 

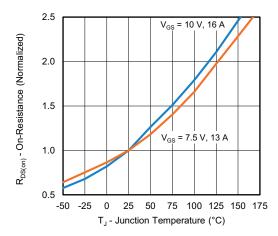
On-Resistance vs. Drain Current



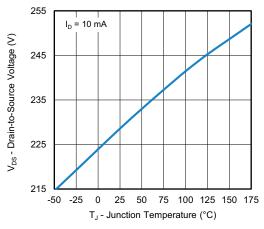




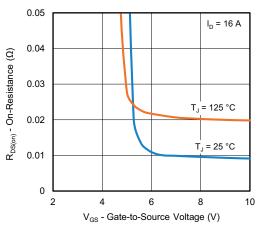
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



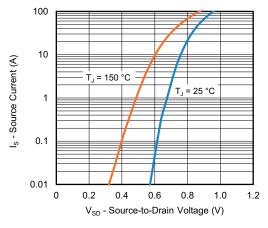
On-Resistance vs. Junction Temperature



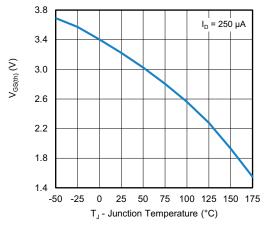
**Drain Source Breakdown vs. Junction Temperature** 



On-Resistance vs. Gate-to-Source Voltage

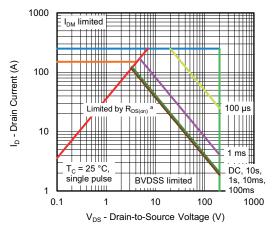


**Source Drain Diode Forward Voltage** 





### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



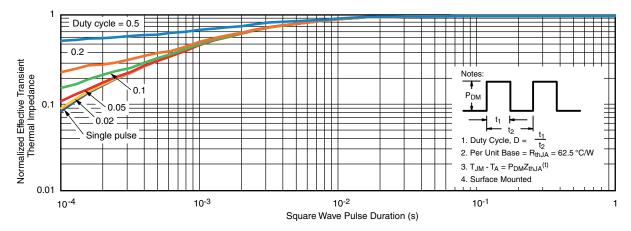
#### Safe Operating Area

# 

Single Pulse Avalanche Current Capability vs. Time

#### Note

a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

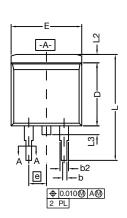


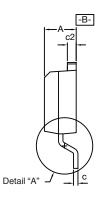
Normalized Thermal Transient Impedance, Junction-to-Case

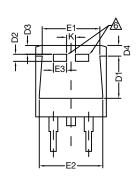
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# TO-263 (D<sup>2</sup>PAK): 3-LEAD









DETAIL A (ROTATED 90°)



_	,	—b <del>-</del> -b	 1			1
2	T			C	_ (	<u>-</u>
	SE	^TIC	M	ا م		1

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6 This feature is for thick lead.

		INCHES		MILLIMETERS	
	DIM.	MIN.	MAX.	MIN.	MAX.
Α		0.160	0.190	4.064	4.826
	b	0.020	0.039	0.508	0.990
	b1	0.020	0.035	0.508	0.889
	b2	0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
CI	Thick lead	0.023	0.027	0.584	0.685
	c2	0.045	0.055	1.143	1.397
	D	0.340	0.380	8.636	9.652
	D1	0.220	0.240	5.588	6.096
	D2	0.038	0.042	0.965	1.067
	D3	0.045	0.055	1.143	1.397
	D4	0.044	0.052	1.118	1.321
	Е	0.380	0.410	9.652	10.414
	E1	0.245	-	6.223	-
	E2	0.355	0.375	9.017 9.52	
	E3	0.072	0.078	1.829	1.981
	е	0.100	BSC	2.54 BSC	
	K	0.045	0.055	1.143	1.397
	L	0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
	L2	0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
	L4	0.010 BSC		0.254	BSC
М		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					

DWG: 5843





### RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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