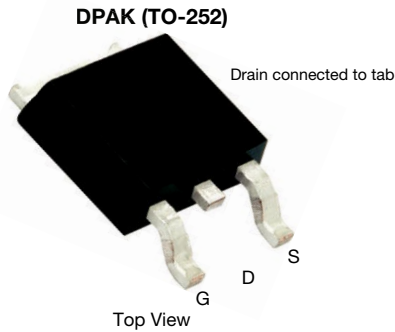


P-Channel 60 V (D-S) MOSFET

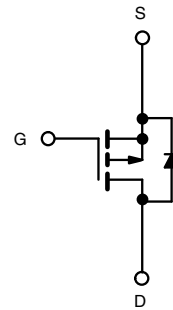


FEATURES

- TrenchFET® power MOSFETs
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-60
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.155
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.280
Q_g typ. (nC)	12.5
I_D (A)	-8.4
Configuration	Single

ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SUD08P06-155L-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	-8.2	A
	$T_C = 100^\circ\text{C}$		-5.2	
Pulsed drain current		I_{DM}	-18	
Continuing source current (diode conduction)		I_S	-8.4	
Avalanche current		I_{AS}	-12	
Single pulse avalanche energy	$L = 0.1$ mH	E_{AS}	7.2	mJ
Maximum power dissipation	$T_C = 25^\circ\text{C}$	P_D	20.8 ^a	W
	$T_A = 25^\circ\text{C}$		1.7 ^b	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-ambient ^b	$t \leq 10$ s	R_{thJA}	20	25	$^\circ\text{C/W}$
	Steady state		62	75	
Junction-to-case		R_{thJC}	5	6	

Notes

- See SOA curve for voltage derating
- Surface mounted on 1" x 1" FR-4 board



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-60	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1	-2	-	
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 125 °C	-	-	-50	
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 150 °C	-	-	-150	
On-state drain current ^b	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-10	-	-	A
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = -10 V, I _D = -5 A	-	0.125	0.155	Ω
		V _{GS} = -10 V, I _D = -5 A, T _J = 125 °C	-	-	0.280	
		V _{GS} = -10 V, I _D = -5 A, T _J = 150 °C	-	-	0.350	
		V _{GS} = -4.5 V, I _D = -2 A	-	0.158	0.280	
Forward transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -5 A	-	8	-	S
Dynamic						
Input capacitance	C _{ISS}	V _{DS} = -25 V, V _{GS} = 0 V, f = 1 MHz	-	450	-	pF
Output capacitance	C _{OSS}		-	65	-	
Reverse transfer capacitance	C _{RSS}		-	40	-	
Total gate charge	Q _g	V _{DS} = -30 V, V _{GS} = -10 V, I _D = -8.4 A	-	12.5	19	nC
Gate-source charge	Q _{gs}		-	2.3	-	
Gate-drain charge	Q _{gd}		-	3.2	-	
Gate resistance	R _g	f = 1 MHz	-	8	-	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = -30 V, R _L = 3.57 Ω I _D ≅ -8.4 A, V _{GEN} = -10 V, R _g = 2.5 Ω	-	5	10	ns
Rise time ^c	t _r		-	14	25	
Turn-off delay time ^c	t _{d(off)}		-	15	25	
Fall time ^c	t _f		-	7	12	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)^b						
Pulsed current	I _{SM}		-	-	-20	A
Forward voltage ^b	V _{SD}	I _F = -2 A, V _{GS} = 0 V	-	-0.9	-1.3	V
Reverse recovery time	t _{rr}	I _F = -8 A, di/dt = 100 A/μs	-	50	80	ns
Reverse recovery time	Q _{rr}		-	80	120	nC

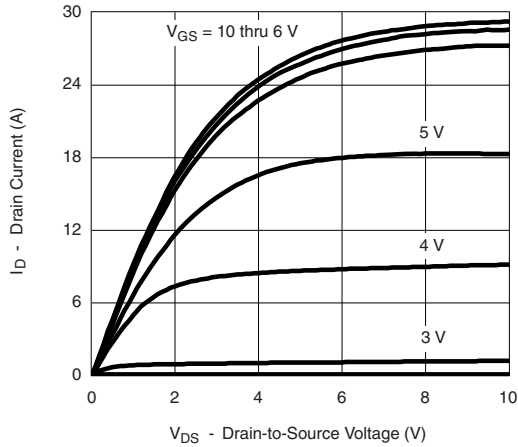
Notes

- Guaranteed by design, not subject to production testing
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- Independent of operating temperature

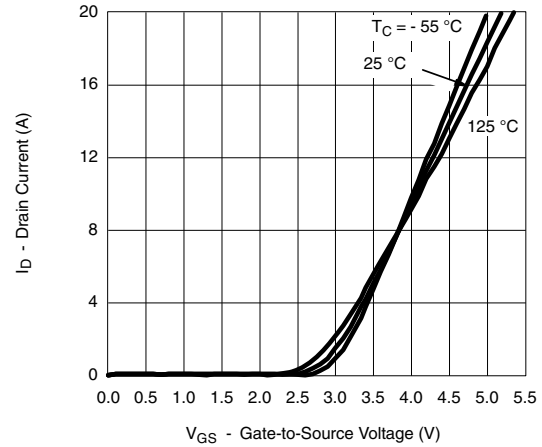
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



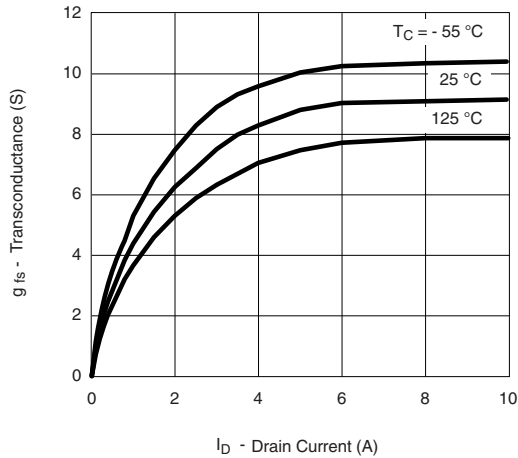
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



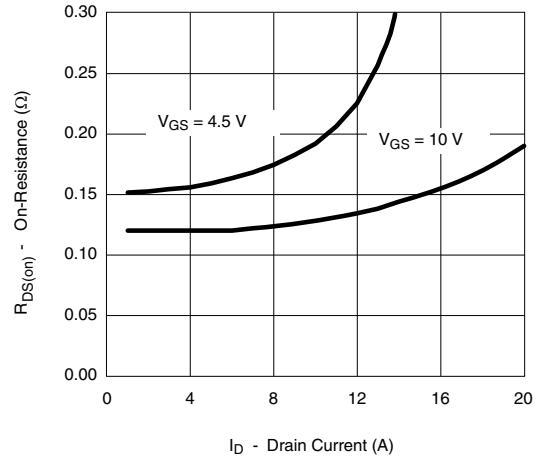
Output Characteristics



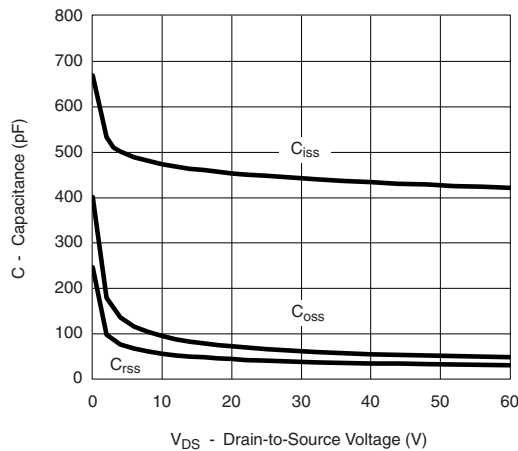
Transfer Characteristics



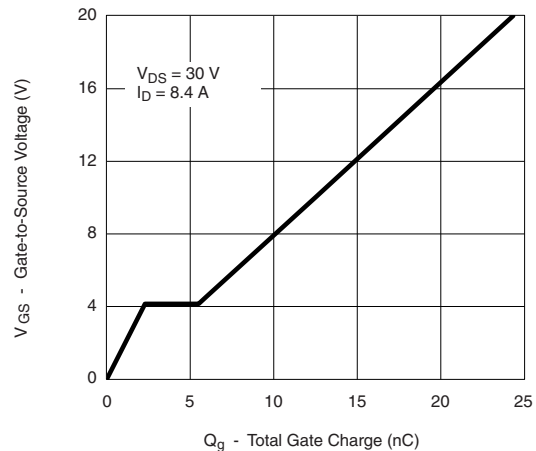
Transconductance



On-Resistance vs. Drain Current



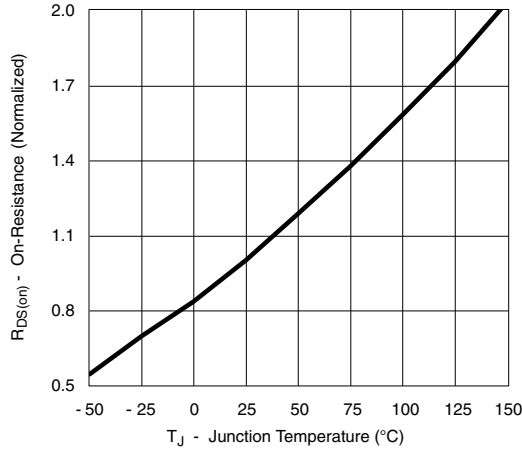
Capacitance



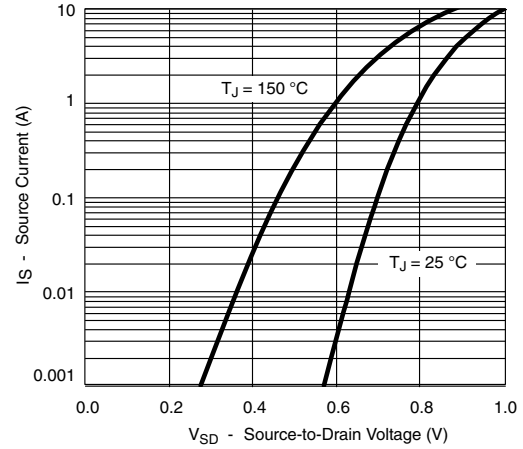
Gate Charge



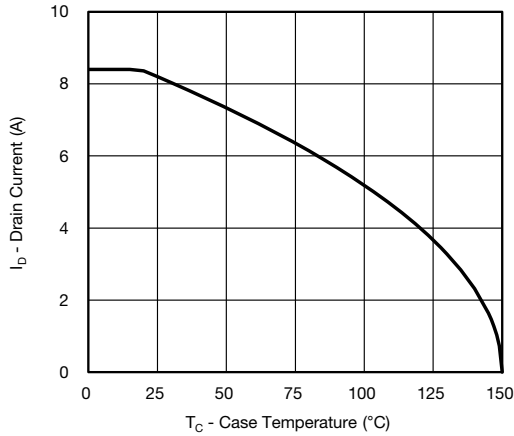
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



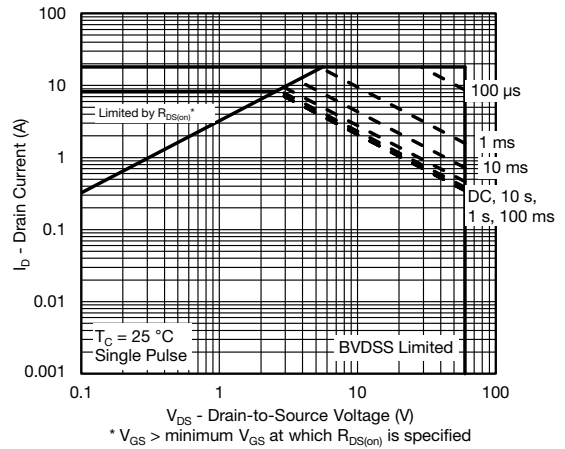
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



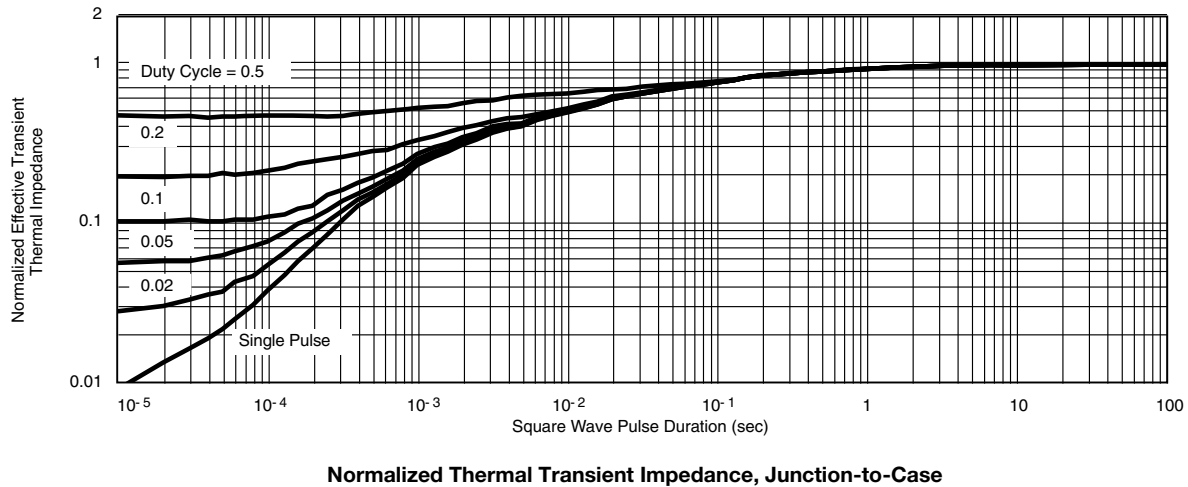
Drain Current vs. Case Temperature



Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62843.



TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



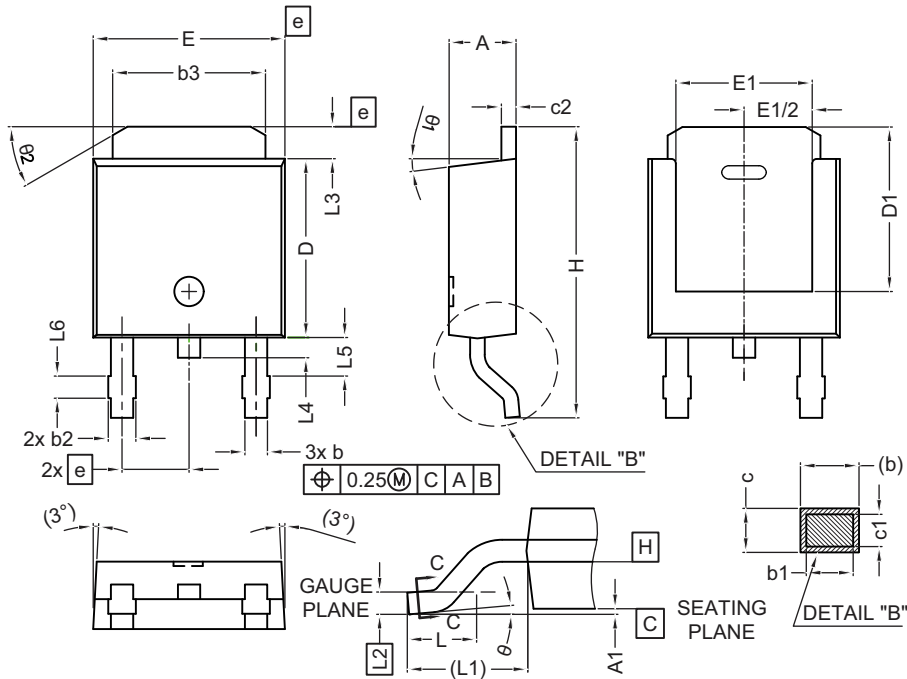
DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
 DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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