Off-Line PWM Controllers with Integrated Power MOSFET

STR4A100 Series

Data Sheet

Description

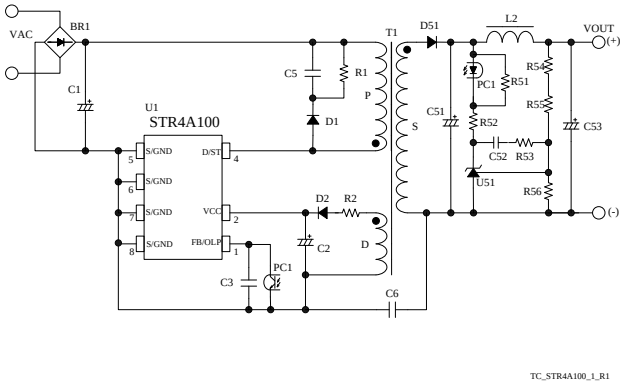
The STR4A100 series are power ICs for switching power supplies, incorporating a sense MOSFET and a current mode PWM controller IC.

The low standby power is accomplished by the automatic switching between the PWM operation in normal operation and the burst-oscillation under light load conditions. The product achieves high cost-performance power supply systems with few external components.

Features

- Current Mode Type PWM Control
- Auto Standby Function
  No Load Power Consumption < 10 mW
- Operation Mode
  Normal Operation: PWM Mode
  Standby : Burst Oscillation Mode
- Random Switching Function
- Slope Compensation Function
- Leading Edge Blanking Function
- Bias Assist Function
- Soft Start Function
- Protections
  − Overcurrent Protection (OCP) : Pulse-by-Pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  − Overload Protection (OLP) : Aauto-restart
  − Overvoltage Protection (OVP) : Auto-restart
  − Thermal Shutdown (TSD) : Auto-restart with hysteresis

Typical Application



TC_STR4A100_1_R1

Package

DIP8

SOIC8

Not to Scale

Lineup

- Electrical Characteristics

$V_{D/ST}$(max.) = 730 V

Products	Package	$f_{OSC(AVG)}$	$R_{DS(ON)}$ (max.)	$I_{DLIM(H)}$
STR4A162S	SOIC8	65kHz	24.6 Ω	0.365 A
STR4A162D	DIP8			
STR4A164D			12.9 Ω	0.520 A
STR4A164HD	DIP8	100kHz	12.9 Ω	0.485 A

- Output Power, P_{OUT}*

Products	Adapter		Open frame	
	AC230V	AC85 ~265V	AC230V	AC85 ~265V
STR4A162S	5 W	4 W	7 W	5.5 W
STR4A162D	5.5 W	4.5 W	7.5 W	6 W
STR4A164D	8 W	6 W	10 W	8.5 W
STR4A164HD	9 W	7 W	13 W	10.5 W

* The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, duty cycle, and thermal design affect the output power. It may be less than the value stated here.

Application

- White goods
- Auxiliary power for Flat TVs
- Low power AC/DC adapter
- Battery Chargers
- Other SMPS

Contents

1. Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified T_A = 25 °C, pin 5 = pin 6 = pin 7 = pin 8

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Remarks
FB/OLP Pin Voltage	V_{FB}		1 – 8	−0.3 to 14	V	
FB/OLP Pin Sink Current	I_{FB}		1 – 8	1.0	mA	
VCC Pin Voltage	V_{CC}		2 – 8	32	V	
D/ST Pin Voltage	$V_{D/ST}$		4 – 8	−0.3 to 730	V	
Drain Peak Current	I_{DP}	Positive: Single pulse Negative: Within 2μs of pulse width	4 – 8	−0.2 to 0.66	A	4A162S
				−0.2 to 0.7		4A162D
				−0.2 to 0.98		4A164D 4A164HD
Power Dissipation(1)	P_D	(2)	4 – 8	1.34	W	4A162S
				1.49		4A162D
				1.55		4A164D 4A164HD
Operating Ambient Temperature	T_{OP}		—	−40 to 125	°C	
Storage Temperature	T_{stg}		—	−40 to 125	°C	
Junction Temperature	T_j		—	150	°C	

(1) Refer to Section 4 MOSFET Temperature versus Power Dissipation Curve
(2) When embedding this hybrid IC onto the printed circuit board (cupper area in a 15mm×15mm)

2. Recommended Operating Conditions

Recommended operating conditions means the operation conditions maintained normal function shown in electrical characteristics.

Parameter	Symbol	Min.	Max.	Units	Remarks
D/ST Pin Voltage in Operation	$V_{D/ST(OP)}$	−0.3	584	V	
VCC Pin Voltage in Operation	$V_{CC(OP)}$	11	27	V	

3. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC
- Unless otherwise specified, T_A = 25 °C, V_{CC} = 18 V,pin 5 = pin 6 = pin 7 = pin 8, V_{FB} = 3 V, $V_{D/ST}$ = 10 V

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$	V_{FB} = 0 V	2 − 8	13.8	15.2	16.8	V	
Operation Stop Voltage(1)	$V_{CC(OFF)}$		2 − 8	7.3	8.1	8.9	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	2 − 8	—	—	2.5	mA	
Startup Circuit Operation Voltage	$V_{STARTUP}$	V_{FB} = 0 V V_{CC} = 13.5 V	4 − 8	19	29	39	V	
Startup Current	$I_{STARTUP}$	V_{FB} = 0 V V_{CC} = 13.5 V $V_{D/ST}$ = 100 V	2 − 8	−3.7	−2.1	−0.9	mA	
Startup Current Biasing Threshold Voltage(1)	$V_{CC(BIAS)}$	V_{FB} = 0 V	2 − 8	7.9	9.4	10.5	V	
PWM Operation								
Average PWM Switching Frequency	$f_{OSC(AVG)}$		4 − 8	58	65	72	kHz	4A162S / 62D/ 64D
				90	100	110		4A164HD
PWM Frequency Modulation Deviation	Δf		4 − 8	—	5	—	kHz	4A162S / 62D/ 64D
				—	7	—		4A164HD
Maximum Duty Cycle	D_{MAX}		4 − 8	65	74	83	%	4A162S / 62D/ 64D
				65	73	82		4A164HD
Protection Function								
Leading Edge Blanking Time(2)	t_{BW}		—	—	290	—	ns	4A162S / 62D/ 64D
				—	250	—		4A164HD
Drain Current Limit Compensation Duty Cycle(2)	D_{DPC}		—	—	36	—	%	
Drain Current Limit (Duty Cycle = 0 %)	$I_{DLIM(L)}$		4 − 8	0.290	0.322	0.354	A	4A162S/ 62D
				0.413	0.459	0.505		4A164D
				0.385	0.428	0.471		4A164HD
Drain Current Limit (Duty Cycle ≥ 36 %)	$I_{DLIM(H)}$		4 − 8	0.336	0.365	0.394	A	4A162S/ 62D
				0.478	0.520	0.562		4A164D
				0.446	0.485	0.524		4A164HD
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V V_{FB} = 0 V	1 − 8	−120	−77	−45	µA	
Minimum Feedback Current	$I_{FB(MIN)}$	V_{FB} = 6.8 V	1 − 8	−28	−13	−6	µA	
FB/OLP Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		1 − 8	0.98	1.23	1.48	V	
OLP Threshold Voltage	$V_{FB(OLP)}$		1 − 8	7.3	8.1	8.9	V	
OLP Operation Current	$I_{CC(OLP)}$		2 − 8	—	230	—	µA	

(1) $V_{CC(BIAS)} > V_{CC(OFF)}$ always
(2) Design assurance

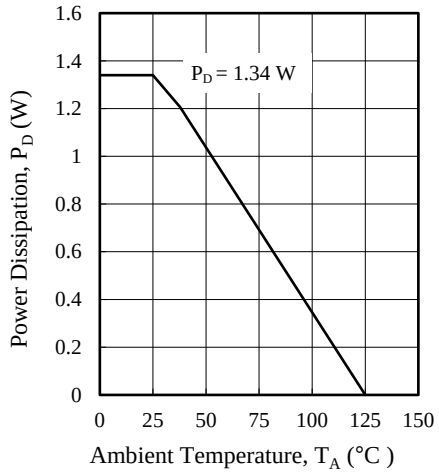
Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
OLP Delay Time	t_{OLP}		—	58	76	94	ms	
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		1 − 8	10.5	12.0	13.5	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		2 − 8	27.5	29.5	31.5	V	
Thermal Shutdown Operating Temperature(2)	$T_{j(TSD)}$		—	135	—	—	°C	
Thermal Shutdown Hysteresis(2)	$T_{j(TSDHYS)}$		—	—	70	—	°C	
MOSFET								
Drain Leakage Current	I_{DSS}	Ta = 125 °C V_{FB} = 0 V $V_{D/ST}$ = 584 V	4 − 8	—	—	50	μA	
On Resistance	$R_{DS(ON)}$	I_D = 37 mA	4 − 8	—	21.0	24.6	Ω	4A162××
		I_D = 52 mA		—	11.0	12.9		4A164××
Switching Time	t_f		4 − 8	—	—	250	ns	
Thermal Characteristics								
Thermal Resistance(2)	θ_{j-F}	(3)	—	—	—	18	°C/W	4A162D
				—	—	21		4A162S
				—	—	16		4A164D / 64HD
	θ_{j-C}	(4)	—	—	—	15	°C/W	4A162D
				—	—	16		4A162S
				—	—	15		4A164D / 64HD

(3) θ_{j-F} is thermal resistance between junction of MIC and frame. Frame temperature (T_F) is measured at the root of the pin 7 (S/GND).
(4) θ_{j-C} is thermal resistance between junction of MIC and case. Case temperature (T_C) is measured at the center of the case top surface

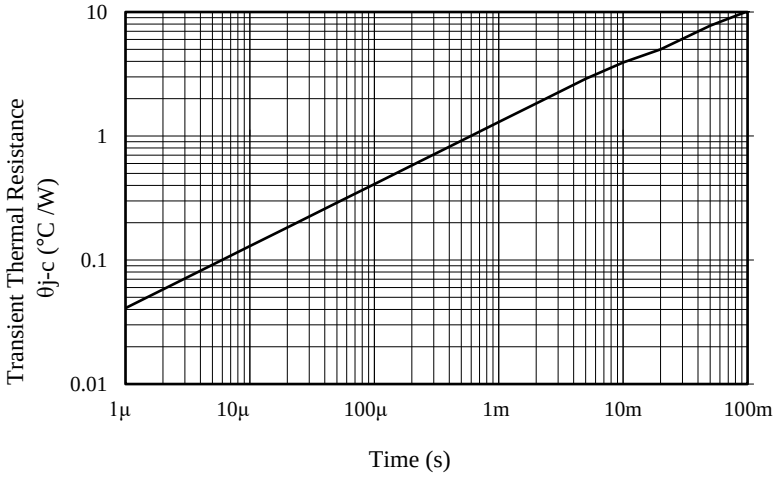
4. Performance Curves

● **STR4A162S**

Ambient Temperature versus Power Dissipation Curve

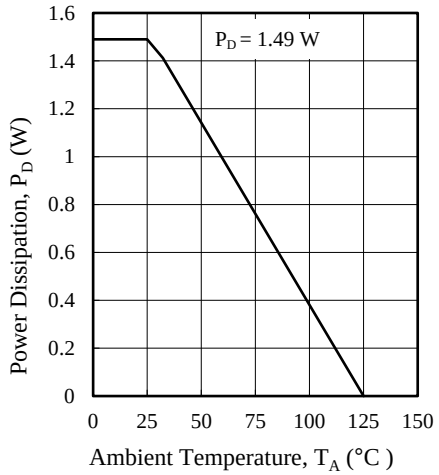


Transient Thermal Resistance Curve

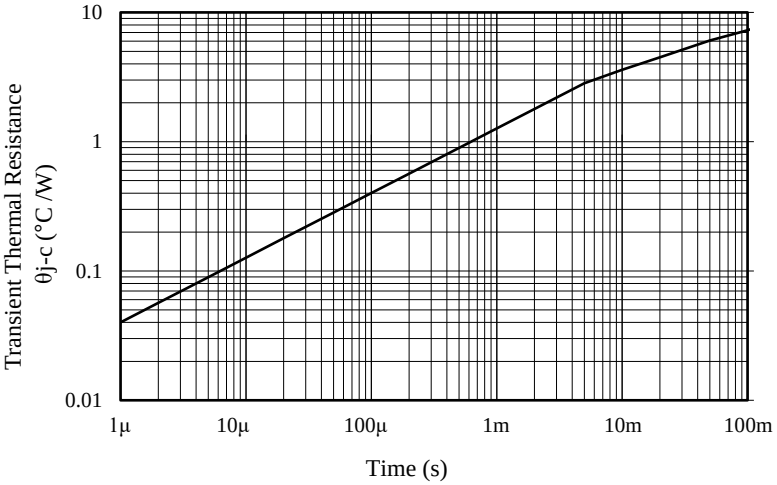


● **STR4A162D**

Ambient Temperature versus Power Dissipation Curve

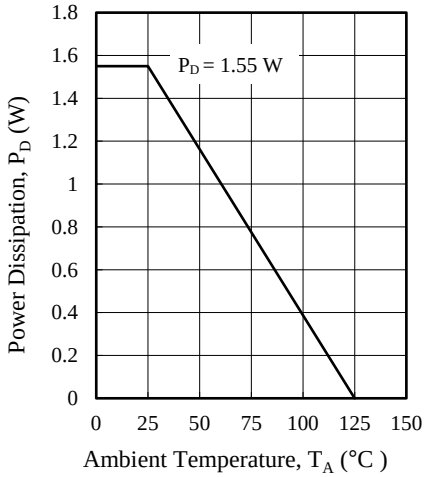


Transient Thermal Resistance Curve

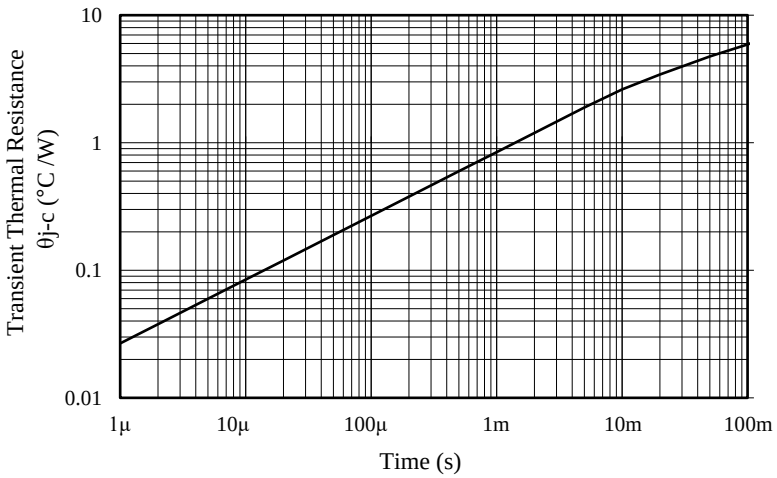


● **STR4A164D / 64HD**

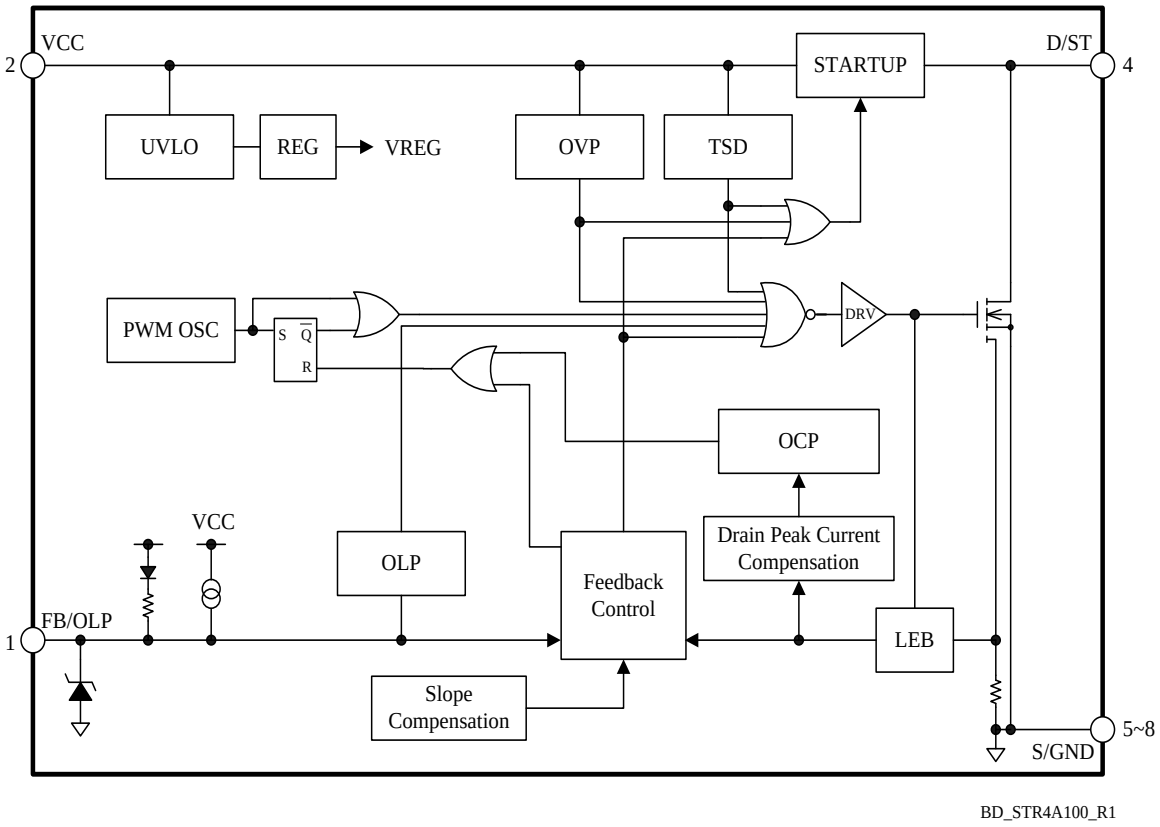
Ambient Temperature versus Power Dissipation Curve



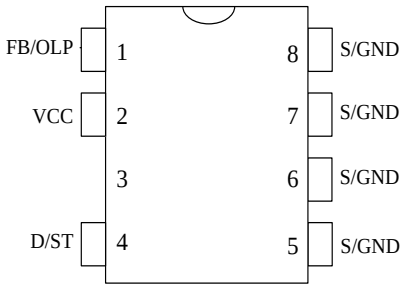
Transient Thermal Resistance Curve



5. Block Diagram



6. Pin Configuration Definitions



Pin	Name	Descriptions
1	FB/OLP	Input of constant voltage control signal and Overload Protection (OLP) signal
2	VCC	Power supply voltage input for Control Part and Overvoltage Protection (OVP) signal input
3	—	(Pin removed)
4	D/ST	MOSFET drain and startup current input
5	S/GND	MOSFET source and ground
6		
7		
8		

7. Typical Application

The PCB traces of the S/GND pins should be as wide as possible, in order to enhance thermal dissipation.

In applications having a power supply specified such that D/ST pin has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/GND pin.

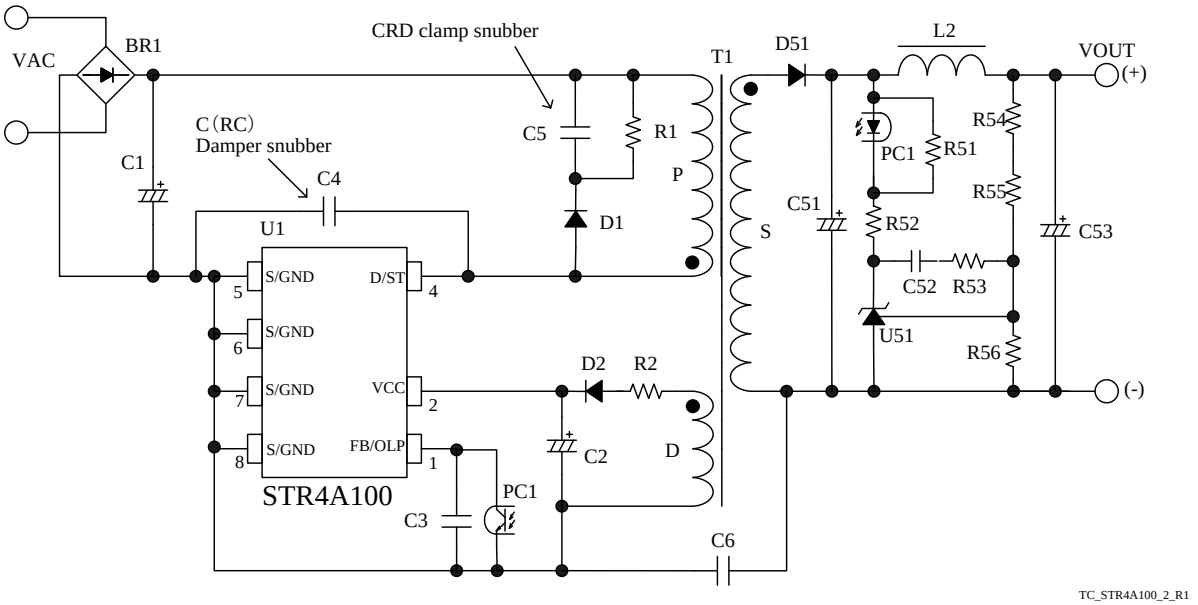
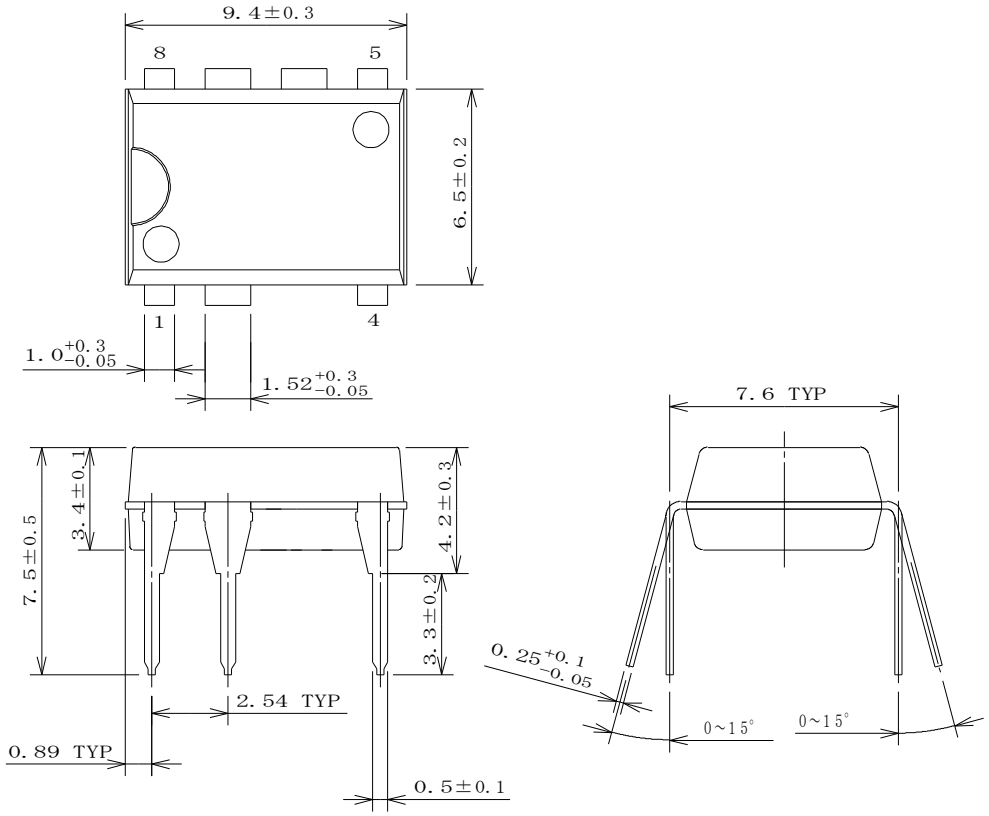


Figure 7-1. Typical Application

8. Physical Dimensions and Marking Diagrams

8.1 DIP8

● Physical Dimensions

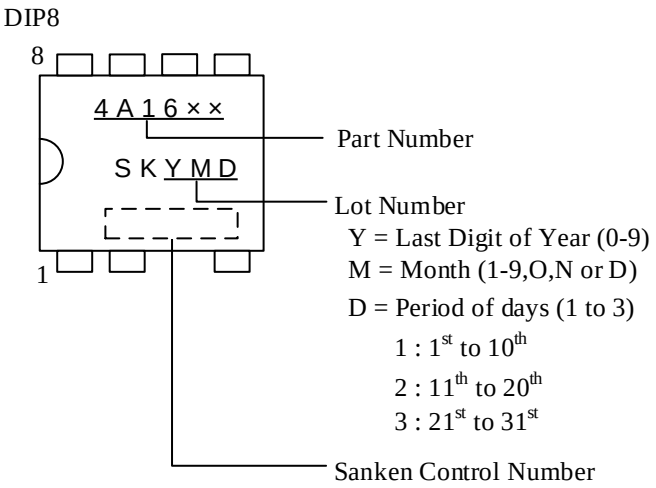


NOTES:

1) Units: mm

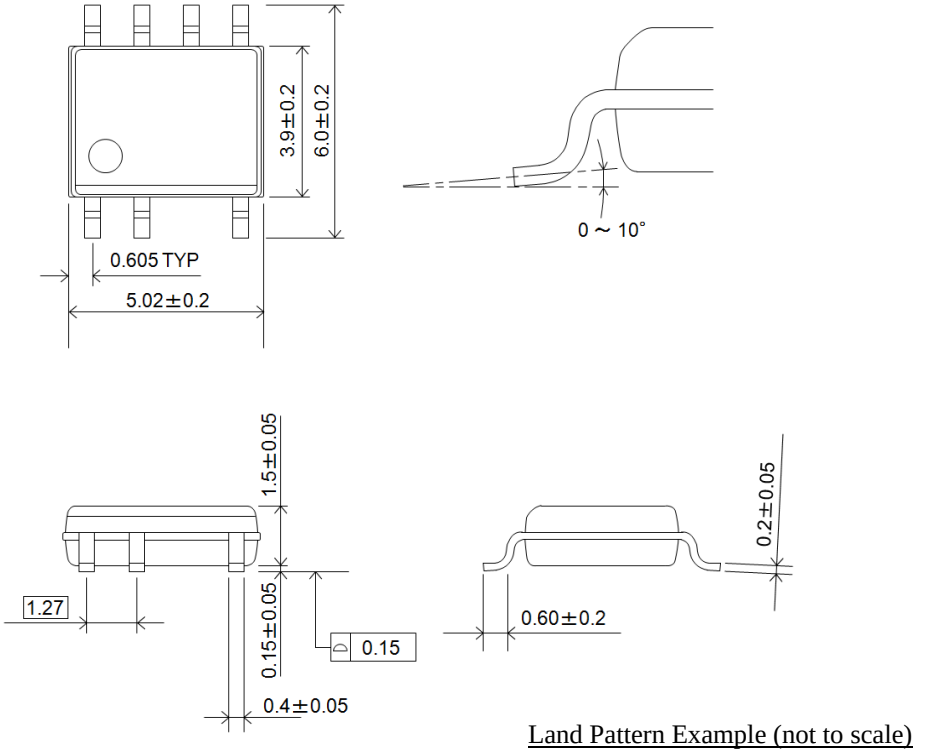
2) Pb-free. Device composition compliant with the RoHS directive

● Marking Diagram

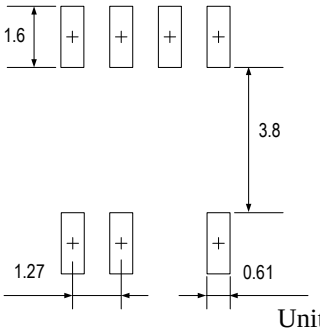


8.2 SOIC8

● Physical Dimensions



Land Pattern Example (not to scale)

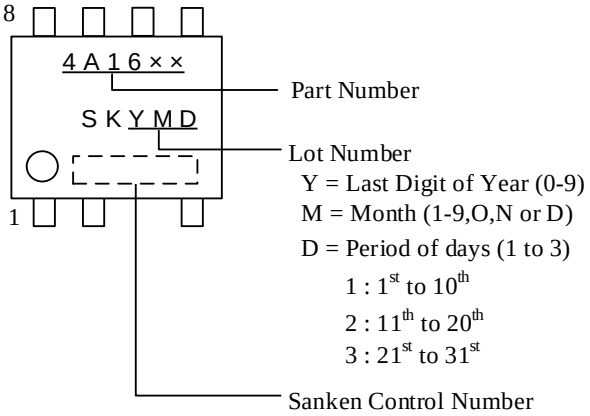


Unit: mm

NOTES:
1) Units: mm
2) Pb-free. Device composition compliant with the RoHS directive

● Marking Diagram

SOIC8



9. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.

With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

9.1 Startup Operation

Figure 9-1 shows the circuit around the VCC pin.

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When the D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{STARTUP}$ = 29 V, the startup circuit starts operation. During the startup process, the constant current, $I_{STARTUP}$ = −2.1 mA, charges C2 at the VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.2 V, the control circuit starts switching operation. During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 9-1 becomes a power source to the VCC pin. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

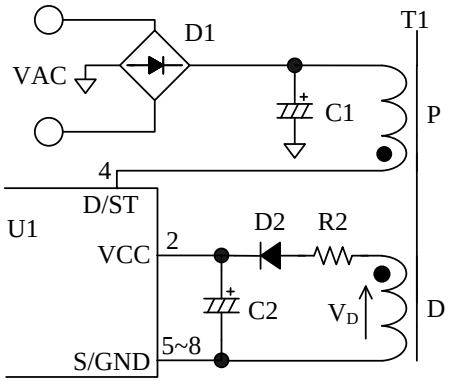


Figure 9-1. VCC Pin Peripheral Circuit

The approximate value of auxiliary winding voltage is 15 to 20 V, taking account of the winding turns of D winding so that the VCC pin voltage becomes Equation (1) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.})$$

$$\Rightarrow 10.5\ (\text{V}) < V_{CC} < 27.5\ (\text{V}) \quad (1)$$

The startup time of the IC is determined by C2 capacitor value. The approximate startup time t_{START} is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STARTUP}|} \quad (2)$$

Where,

t_{START} : Startup time of the IC (s)

$V_{CC(INT)}$: Initial voltage on the VCC pin (V)

9.2 Undervoltage Lockout (UVLO)

Figure 9-2 shows the relationship of the VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

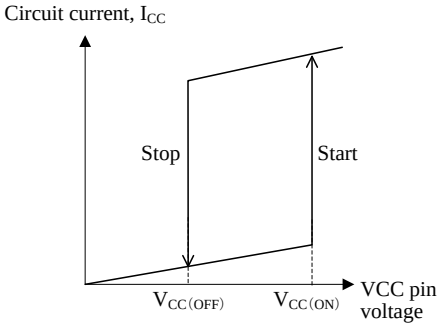


Figure 9-2. Relationship between VCC Pin Voltage and I_{CC}

9.3 Bias Assist Function

By the Bias Assist Function, the startup failure is prevented.

When FB pin voltage is the FB/OLP Pin Oscillation Stop Threshold Voltage, $V_{FB(OFF)}$= 1.23 V or less and VCC pin voltage decreases to the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)}$ = 9.4 V, the Bias Assist Function is activated.

When the Bias Assist Function is activated, the VCC pin voltage is kept almost constant voltage, $V_{CC(BIAS)}$ by providing the startup current, $I_{STARTUP}$, from the startup circuit. Thus, the VCC pin voltage is kept more than $V_{CC(OFF)}$.

Since the startup failure is prevented by the Bias Assist Function, the value of C2 connected to the VCC pin can be small. Thus, the startup time and the response time of the Overvoltage Protection (OVP) become shorter.

The operation of the Bias Assist Function in startup is as follows. It is necessary to check and adjust the startup

process based on actual operation in the application, so that poor starting conditions may be avoided.

Figure 9-3 shows the VCC pin voltage behavior during the startup period.

After the VCC pin voltage increases to $V_{CC(ON)}$ = 15.2 V at startup, the IC starts the operation. Then circuit current increases and the VCC pin voltage decreases. At the same time, the auxiliary winding voltage, V_D, increases in proportion to output voltage. These are all balanced to produce the VCC pin voltage.

When the VCC pin voltage is decrease to $V_{CC(OFF)}$ = 8.1 V in startup operation, the IC stops switching operation and a startup failure occurs.

When the output load is light at startup, the output voltage may become more than the target voltage due to the delay of feedback circuit. In this case, the FB pin voltage is decreased by the feedback control. When the FB pin voltage decreases to $V_{FB(OFF)}$ or less, the IC stops switching operation and the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist function is activated and the startup failure is prevented.

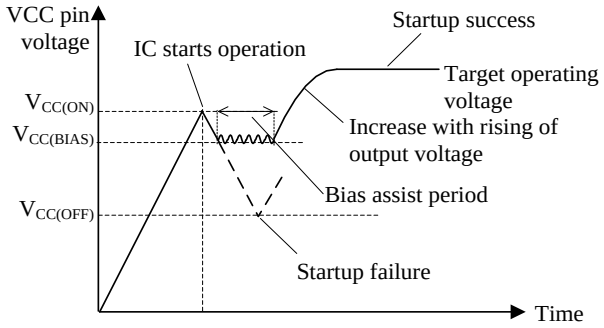


Figure 9-3. VCC Pin Voltage During Startup Period

9.4 Soft Start Function

Figure 9-4 shows the behavior of VCC pin voltage and drain current during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 6 ms. during the soft start period, overcurrent threshold is increased step-wisely (5 steps). This function reduces the voltage and the current stress of a power MOSFET and the secondary side rectifier diode.

Since the Leading Edge Blanking Function (refer to Section 9.6) is deactivated during the soft start period, there is the case that on time is less than the Leading Edge Blanking Time, t_{BW}. After the soft start period, D/ST pin current, I_D, is limited by the Drain Current Limit, I_{DLIM}, until the output voltage increases to the target operating voltage. This period is given as t_{LIM}. In case t_{LIM} is longer than the OLP Delay Time, t_{OLP}, the output power is limited by the Overload Protection (OLP) operation. Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{OLP} = 58 ms (min.).

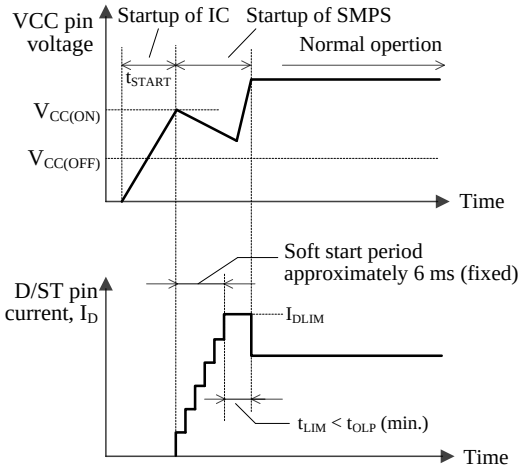


Figure 9-4. V_{CC} and I_D Behavior During Startup

9.5 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (refer to Section 5.Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 9-5 and Figure 9-6.

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases. This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.This control prevents the output voltage from decreasing.

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the

target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 9-7. This is called the subharmonics phenomenon. In order to avoid this, the IC incorporates the Slope Compensation Function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the duty cycle gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed. Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

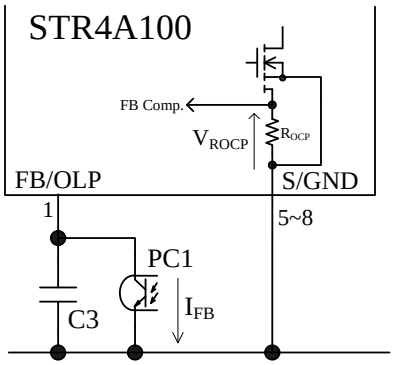


Figure 9-5. FB/OLP Pin Peripheral Circuit

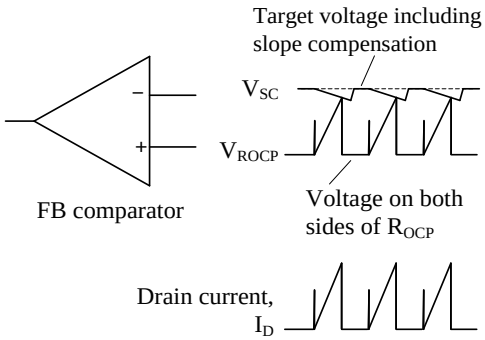


Figure 9-6. Drain Current, I_D, and FB Comparator Operation in Steady Operation

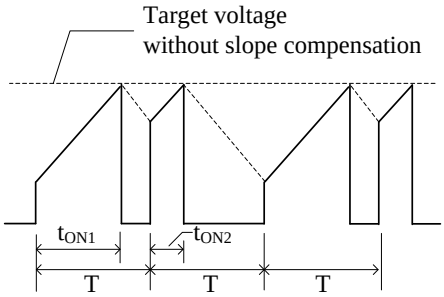


Figure 9-7. Drain Current, I_D, Waveform in Subharmonic Oscillation

9.6 Leading Edge Blanking Function

The constant voltage control of output of the IC uses the peak-current-mode control method.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of a FB comparator or Overcurrent Protection (OCP) circuit to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking Time, t_{BW}, is built-in.

9.7 Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

9.8 Automatic Standby Mode Function

In light load, FB/OLP pin voltage according to decreasing drain current, I_D.

Automatic standby mode is activated automatically when FB/OLP pin voltage decreases to $V_{FB(OFF)}$.

The operation mode becomes burst oscillation, as shown in Figure 9-8.

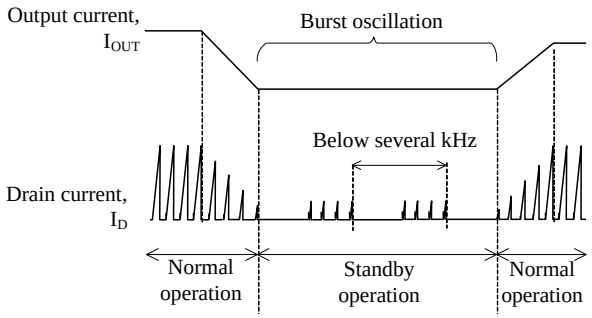


Figure 9-8. Auto-standby Mode Timing

Burst oscillation mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals. Generally, in order to improve efficiency under light load conditions, the frequency of the burst oscillation mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst oscillation mode, audible noises can be reduced. If VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.4 V during the transition to the burst oscillation mode, the Bias Assist Function is activated and stabilizes the Standby mode operation, because the Startup Current, $I_{STARTUP}$ is provided to the VCC pin so that the VCC pin

voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist Function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and the secondary-side winding and/or reducing the value of R2 in Figure 10-2 (refer to Section 10.1 Peripheral Components for a detail of R2)

9.9 Overcurrent Protection (OCP)

9.9.1 OCP Operation

Overcurrent Protection (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage.

9.9.2 OCP Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the actual drain peak current is, compared to the Drain Current Limit. Thus, the peak current has some variation depending on AC input voltage in OCP state. In order to reduce the variation of peak current in OCP state, the IC has Input Compensation Function. This function corrects the Drain Current Limit depending on AC input voltage, as shown in Figure 9-9.

When AC input voltage is low (Duty cycle is broad), the Drain Current Limit is controlled to become high. The difference of peak drain current become small compared with the case where the AC input voltage is high (Duty cycle is narrow). The compensation signal depends on the duty cycle. The relation between the Duty cycle and the Drain Current Limit after compensation, I_{DLIM}', is expressed as Equation エラー! 参照元が見つかりません。. When duty cycle is broader than 36 %, the Drain Current Limit becomes a constant value $I_{DLIM(H)}$.

$$I_{DLIM}' = \frac{I_{DLIM(H)} - I_{DLIM(L)}}{36\ (\%)} \times \mathrm{Duty} + I_{DLIM(L)} \qquad (3)$$

where,
Duty : MOSFET duty cycle (%)
$I_{DLIM(H)}$: Drain current limit (Duty cycle ≥ 36 %)
$I_{DLIM(L)}$: Drain current limit (Duty cycle = 0 %)

Products	$I_{DLIM(H)}$	$I_{DLIM(L)}$
4A162D / 62S	0.365 A	0.322 A
4A164HD	0.485 A	0.428A
4A164D	0.520 A	0.459 A

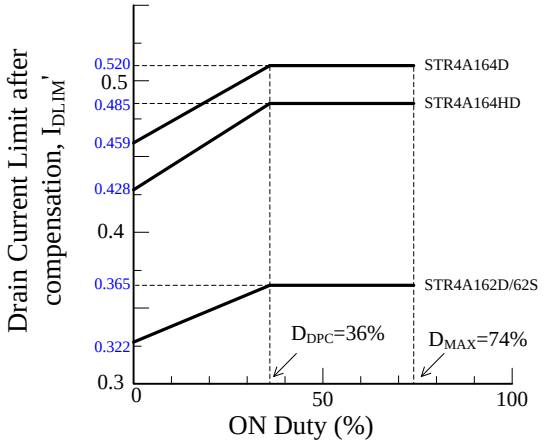


Figure 9-9. Relationship between Duty Cycle and Drain Current Limit after Compensation

9.10 Overload Protection (OLP)

Figure 9-10 shows the FB/OLP pin peripheral circuit, and Figure 9-11 shows each waveform for Overload Protection (OLP) operation. When the peak drain current of I_D is limited by Overcurrent Protection operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 8.1 V or more for the OLP delay time, t_{OLP} = 76 ms or more, the OLP is activated, the IC stops switching operation.

During OLP operation, Bias Assist Function is disabled. Thus, VCC pin voltage decreases to $V_{CC(OFF)}$, the control circuit stops operation. After that, the IC reverts to the initial state by UVLO circuit, and the IC starts operation when VCC pin voltage increases to $V_{CC(ON)}$ by startup current. Thus, the intermittent operation by UVLO is repeated in OLP state.

This intermittent operation reduces the stress of parts such as a power MOSFET and secondary side rectifier diodes. In addition, this operation reduces power consumption because the switching period in this intermittent operation is short compared with oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

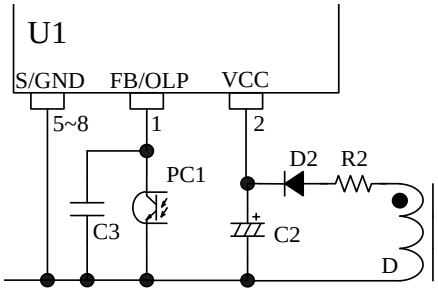


Figure 9-10. FB/OLP Pin Peripheral Circuit

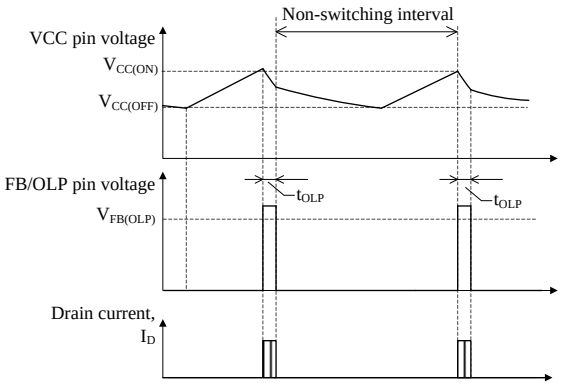


Figure 9-11. OLP Operational Waveforms

9.11 Overvoltage Protection (OVP)

When a voltage between the VCC pin and the S/GND pin increases to $V_{CC(OVP)}$ = 29.5 V or more, Overvoltage Protection (OVP) is activated and the IC stops switching operation. During OVP operation, the Bias Assist Function is disabled, the intermittent operation by UVLO is repeated (refer to Section 9.10). When the fault condition is removed, the IC returns to normal operation automatically (refer to Figure 9-12).

Figure 9-13 shows OVP operational waveforms at high temperature.

If OVP is activated in the condition that the junction temperature, T_j, of IC is higher than $T_{j(TSD)}-T_{j(TSD)HYS}$, the OVP operations as below.

When the VCC pin voltage decreases to $V_{CC(OFF)}$, the Bias Assist Function is activated. When T_j reduces to less than $T_{j(TSD)}-T_{j(TSD)HYS}$, the Bias Assist Function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$.

Release condition of OVP at high temperature is $T_j \leq (T_{j(TSD)}-T_{j(TSD)HYS})$ and VCC pin voltage $\leq V_{CC(OFF)}$.

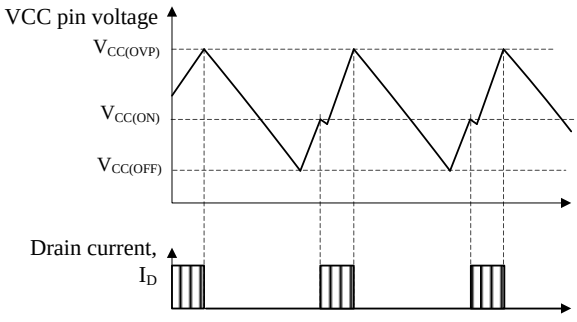


Figure 9-12. OVP Operational Waveforms

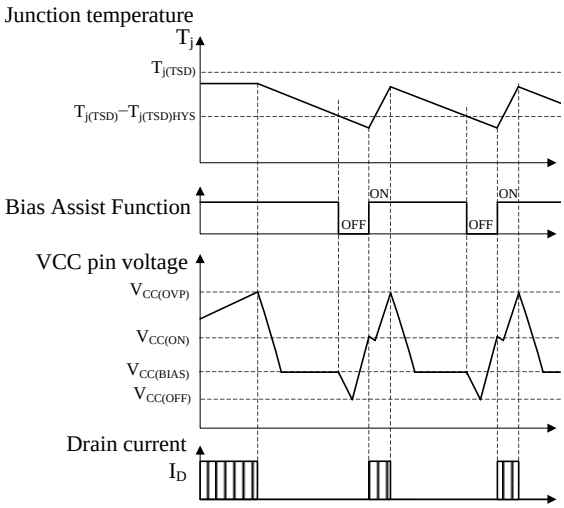


Figure 9-13. OVP Operational Waveforms in High Temperature

When VCC pin voltage is provided by using auxiliary winding of transformer, the VCC pin voltage is proportional to output voltage. Thus, the VCC pin can detect the overvoltage conditions such as output voltage detection circuit open. The approximate value of the output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.5\ (V) \quad (4)$$

Where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

9.12 Thermal Shutdown (TSD)

Figure 9-14 shows the TSD operational waveforms. When the temperature of control circuit increases to $T_{j(TSD)}$ = 135 °C or more, Thermal Shutdown (TSD) is activated and the IC stops switching operation. After that, VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and the VCC pin voltage is kept to over the $V_{CC(OFF)}$.

When the temperature reduces to less than $T_{j(TSD)}-T_{j(TSD)HYS}$, the Bias Assist Function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$. At that time, the IC stops operation and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$, and the IC starts switching operation again.

In this way, the intermittent operation by the TSD and the UVLO is repeated while there is an excess thermal condition. When the fault condition is removed, the IC returns to normal operation automatically.

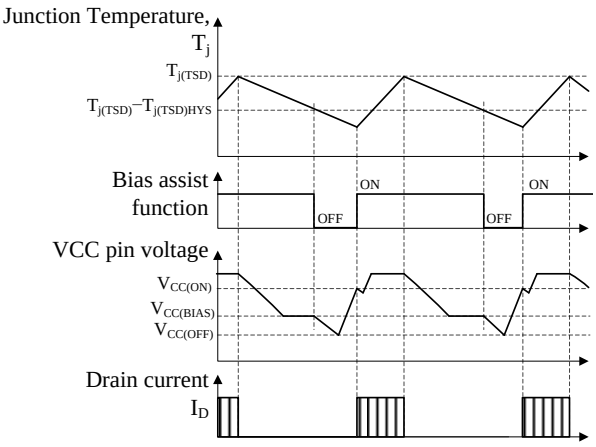


Figure 9-14. TSD Operational Waveforms

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

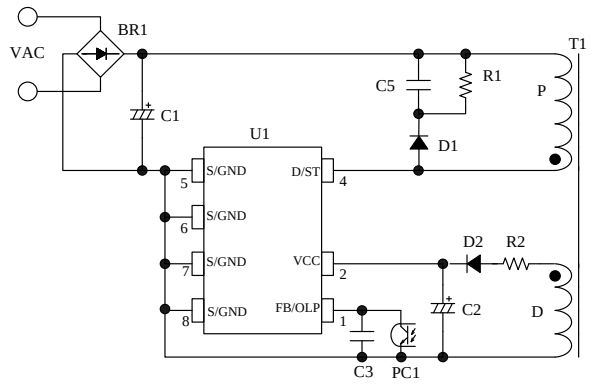


Figure 10-1. IC Peripheral Circuit

10.1.1 Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

10.1.2 FB/OLP Pin Peripheral Circuit

C3 (see Figure 10-1) is for high frequency noise rejection and phase compensation, and should be connected close to the FB/OLP pin and the S/GND pin. The value of C3 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

10.1.3 VCC Pin Peripheral Circuit

The value of C2 in Figure 10-1 is generally recommended to be 10 µF to 47 µF (refer to Section 9.1 Startup Operation, because the startup time is determined by the value of C2)

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 10-2), and the Overvoltage Protection (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 10-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

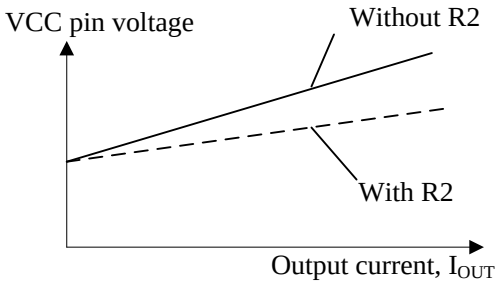


Figure 10-2. Variation of VCC Pin Voltage and Power

10.1.4 D/ST Pin

Figure 10-3 shows D/ST pin peripheral circuit and Figure 10-4 shows D/ST pin waveform in normal operation.

The internal power MOSFET connected to D/ST pin is permanently damaged when the D/ST pin voltage and the current exceed the Absolute Maximum Ratings. The D/ST pin voltage is tuned to be less than about 90 % of the Absolute Maximum Ratings (657 V) in all condition of actual operation, and the value of transformer and components should be selected based on actual operation in the application. And the D/ST pin voltage in normal operation is tuned to be the Recommended Operating Conditions, $V_{D/ST(OP)}$ < 584 V.

The fast recovery diodes are recommended for using as D1, D2 and D51. (for D1, SARS is also recommended)

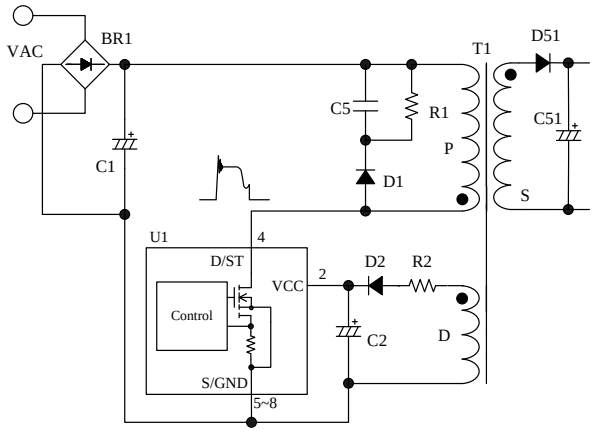


Figure 10-3. D/ST Pin Peripheral Circuit

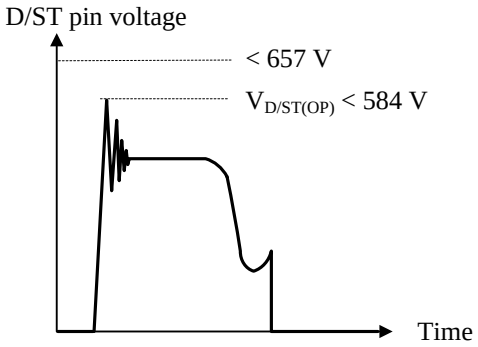


Figure 10-4. D/ST Pin Voltage Waveform in Normal Operation

10.1.5 Peripheral circuit of secondary side shunt regulator

Figure 10-5 shows the secondary side detection circuit with the standard shunt regulator IC (U51).

C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047 µF to 0.47 µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

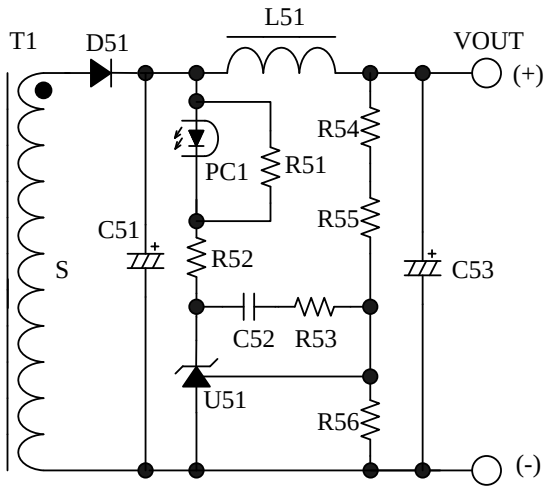


Figure 10-5. Peripheral Circuit of Secondary Side Shunt Regulator (U51)

10.1.6 Transformer

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage

Protection (OVP) may be activated. In transformer design, the following should be considered;

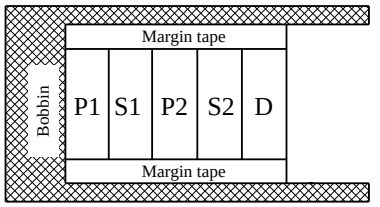
- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3···) should be maximized to improve the line-regulation of those outputs.

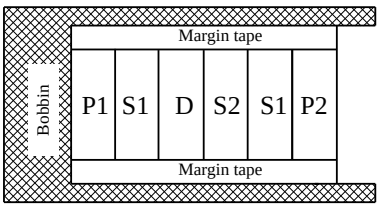
Figure 10-6 shows the winding structural examples of two outputs.

- Winding structural example (a):
  S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.
  D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

- Winding structural example (b)
  P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.
  D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.



Winding structural example (a)



Winding structural example (b)

Figure 10-6. Winding Structural Examples

10.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 10-7 shows the circuit design example.

(1) Main Circuit Trace Layout:
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.
If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout
Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point as close to the S/GND pin as possible.

(3) VCC Trace Layout:
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the S/GND pin is recommended.

(4) FB/OLP Trace Layout
The components connected to FB/OLP pin should be as close to FB/OLP pin as possible. The trace between the components and FB/OLP pin should be as short as possible.

(5) Secondary Rectifier Smoothing Circuit Trace Layout:
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(6) Thermal Considerations
Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
Since the copper area under the IC and the S/GND pin trace act as a heatsink, its traces should be as wide as possible.

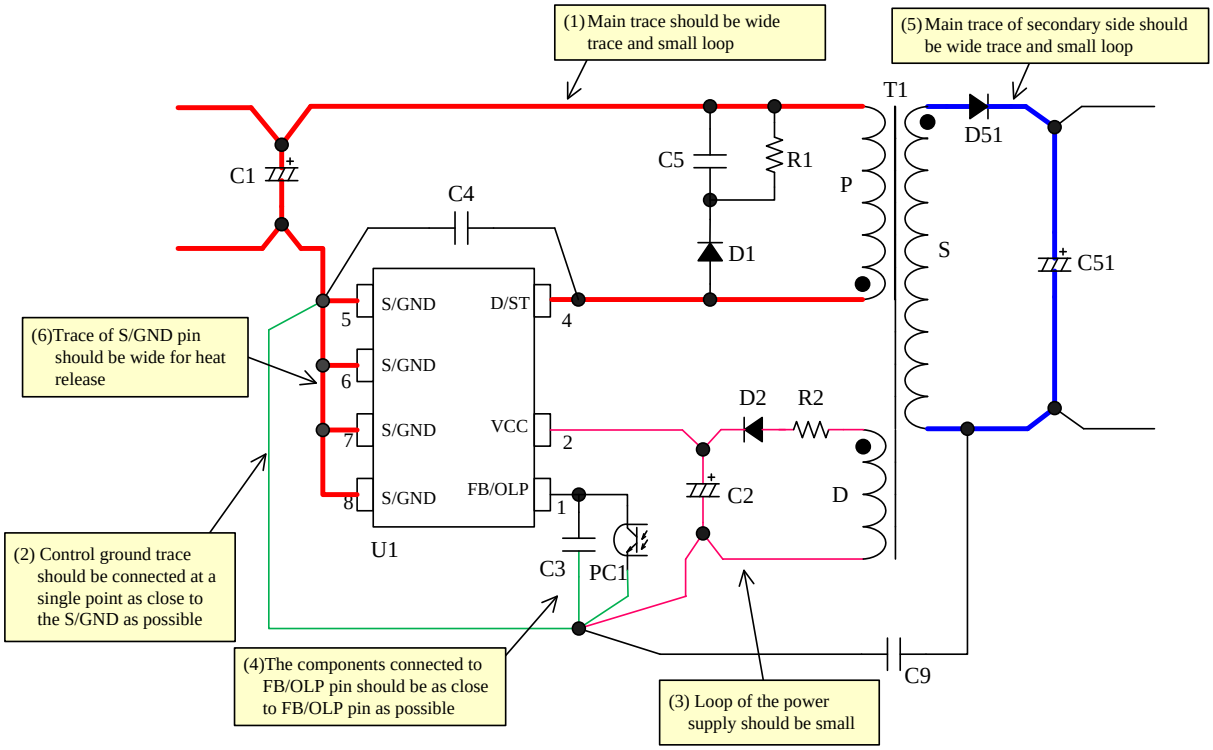


Figure 10-7. Peripheral Circuit Example Around IC

11. Pattern Layout Example

The following show the two outputs PCB layout example and the schematic of circuit using SOIC8 type of STR4A100 series.

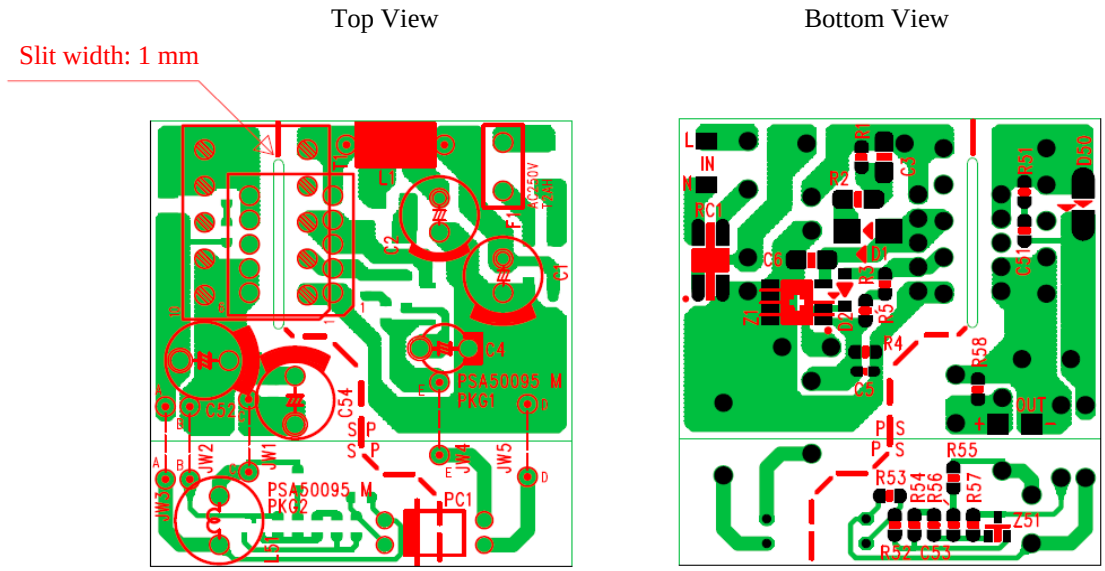


Figure 11-1. PCB Layout Example (SOIC8 Type)

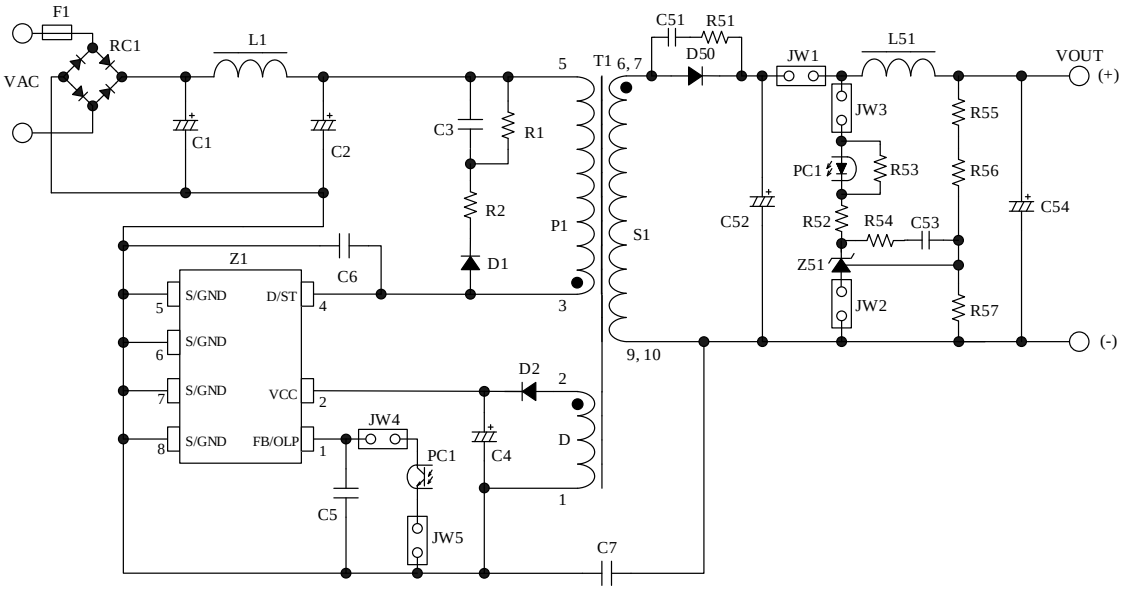


Figure 11-2. Circuit Schematic for PCB Layout

12. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

- Power Supply Specification

IC	STR4A162S
Input Voltage	AC85V to AC265V
Maximum Output Power	5 W (peak)
Output Voltage	5 V
Output Current	1 A (max.)

- Circuit Schematic
  Refer to Figure 11-2

- Bill of Materials

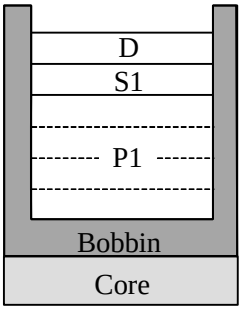
Symbol	Part Type	Ratings(1)	Recommended Sanken Parts	Symbol	Part Type	Ratings(1)	Recommended Sanken Parts
RC1	General, chip	800 V, 1 A		D50	Schottky	60 V, 3 A	SJPB-L6
F1	Fuse	AC 250 V, 1 A		R1 (3)	Metal oxide, chip	680 kΩ	
L1 (2)	CM inductor	470 μH		R2	General, chip	47 Ω	
C1 (2)	Electrolytic	400 V, 6.8 μF		R51	General, chip	Open	
C2 (2)	Electrolytic	400 V, 6.8 μF		R52	General, chip	560 Ω	
C3	Ceramic, chip	630 V, 680 pF		R53	General, chip	6.8 kΩ	
C4	Electrolytic	50 V, 10 μF		R54	General, chip	5.6 kΩ	
C5	Ceramic, chip	50 V, 4700 pF		R55 (2)	General, chip	6.8 kΩ	
C6	Ceramic, chip	Open		R56 (2)	General, chip	0 Ω	
C7	Ceramic, chip	250 V,680 pF		R57	General, 1%	2.2 kΩ	
C51	Ceramic, chip	Open		L51	Inductor	Short	
C52	Electrolytic	16 V, 1000 μF		PC1	Photo-coupler	PC123 or equiv	
C53 (2)	Electrolytic	50 V, 0.47 μF		T1	Transformer	See the specification	
C54 (2)	Electrolytic	Open		Z1	IC		STR4A162S
D1	General, chip	800V, 1A	SARS05	Z51	Shunt regulator	V_{REF} = 1.24 V KIA2431AS or equiv	
D2	First recovery	250 V, 250 mA					

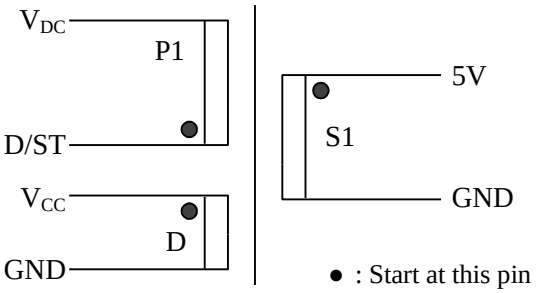
(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

● Transformer Specification

- Primary Inductance, L_P : 2.0 mH
- Core size : EI-16
- Al-value : 108 nH/N^2 (Center gap of about 0.15 mm)
- Winding Specification

Winding	Symbol	Number of Turns (T)	Wire Diameter (mm)	Construction
Primary Winding	P1	136	φ 0.20	Four layers, solenoid winding
Output Winding	S1	8	φ 0.32 × 2	Single-layer, solenoid winding
Auxiliary Winding	D	21	φ 0.20	Single-layer, solenoid winding





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