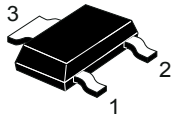
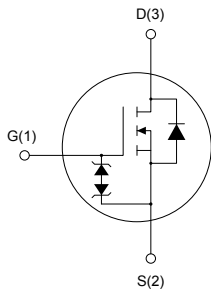


N-channel 600 V, 1.00 Ω typ., 5.5 A MDmesh M2 Power MOSFET in an SOT223-2 package


SOT223-2


NG1D3S2_SOT223

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STN6N60M2	600 V	1.25 Ω	5.5 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.



Product status link

[STN6N60M2](#)

Product summary

Order code	STN6N60M2
Marking	6N60M2
Package	SOT223-2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	8	A
P_{TOT}	Total power dissipation at $T_S = 25\text{ }^\circ\text{C}$	6	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 5.5\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$; $V_{DD} = 400\text{ V}$
- $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-s}	Thermal resistance junction-solder point	20	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	38	$^\circ\text{C}/\text{W}$

- When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax.}$)	0.8	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	83	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$; $T_C = 125\text{ °C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2\text{ A}$		1.00	1.25	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	220	-	pF
C_{oss}	Output capacitance		-	12.5	-	pF
C_{rss}	Reverse transfer capacitance		-	3.3	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	23	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	9	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 4\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$, (see Figure 15. Test circuit for gate charge behavior)	-	6.2	-	nC
Q_{gs}	Gate-source charge		-	1.3	-	nC
Q_{gd}	Gate-drain charge		-	2.7	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	6.4	-	ns
t_r	Rise time		-	6.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	18	-	ns
t_f	Fall time		-	15.8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		5.5	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		8	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 4\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	229		ns
Q_{rr}	Reverse recovery charge		-	721		nC
I_{RRM}	Reverse recovery current		-	6.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	288		ns
Q_{rr}	Reverse recovery charge		-	936		nC
I_{RRM}	Reverse recovery current		-	6.5		A

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

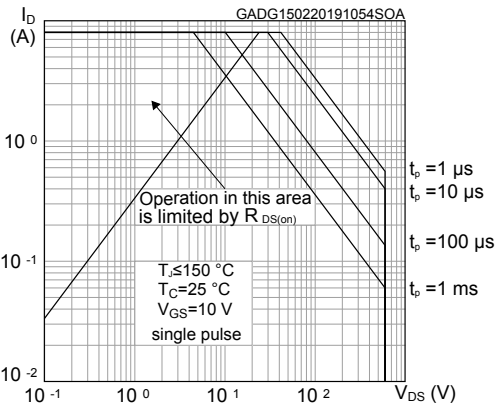


Figure 2. Thermal impedance

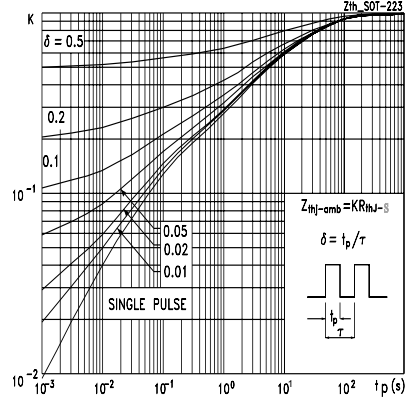


Figure 3. Output characteristics

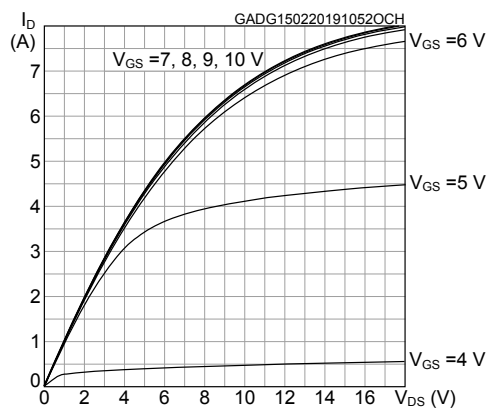


Figure 4. Transfer characteristics

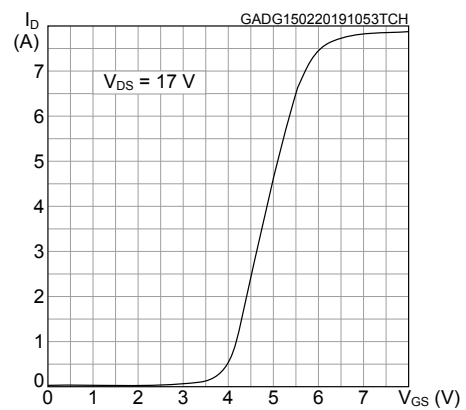


Figure 5. Normalized VBR(DSS) vs temperature

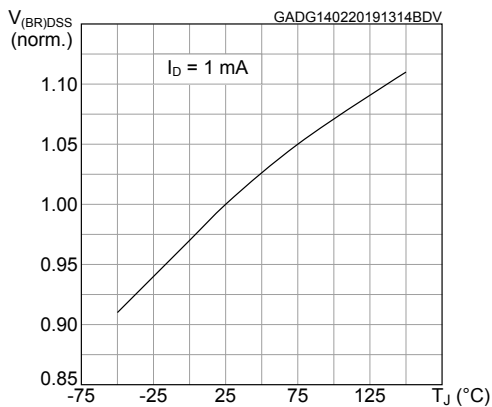


Figure 6. Static drain-source on-resistance

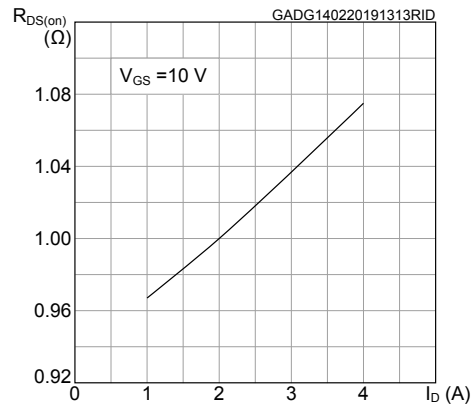


Figure 7. Gate charge vs gate-source voltage

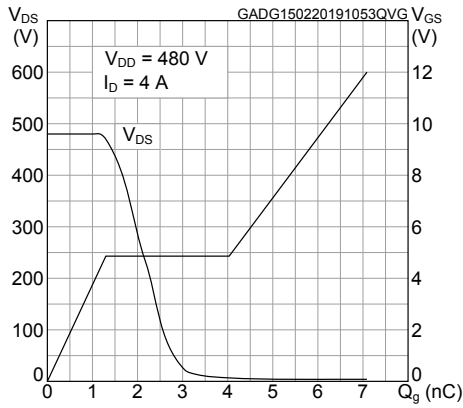


Figure 8. Capacitance variations

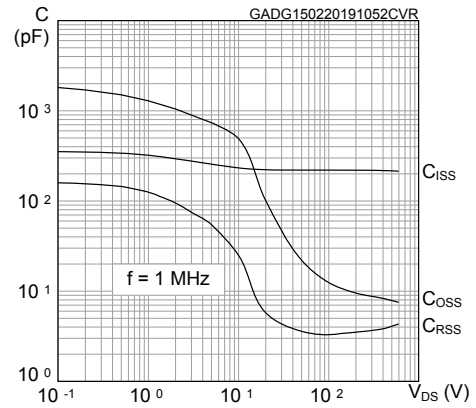


Figure 9. Normalized gate threshold voltage vs temperature

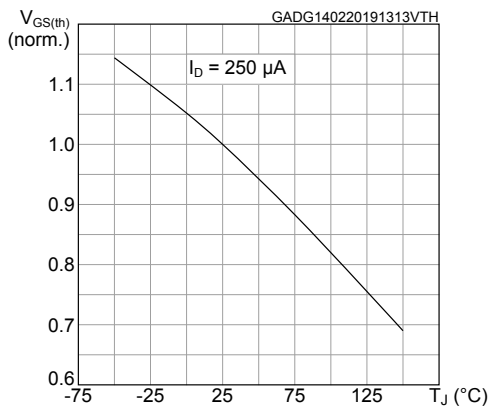


Figure 10. Normalized on-resistance vs temperature

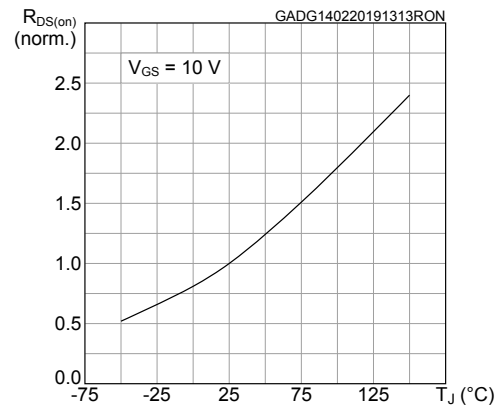


Figure 11. Source-drain diode forward characteristics

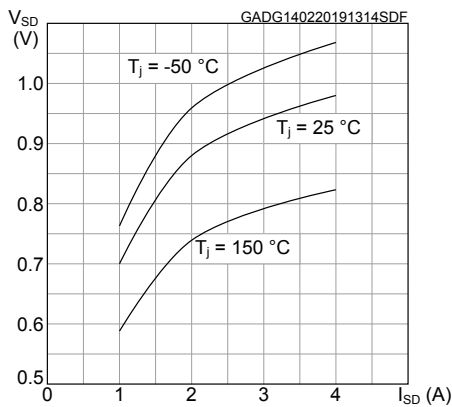
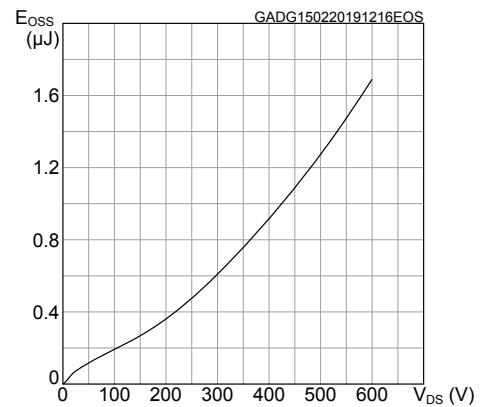
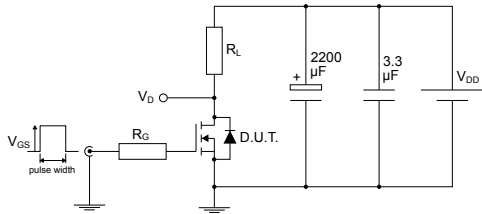


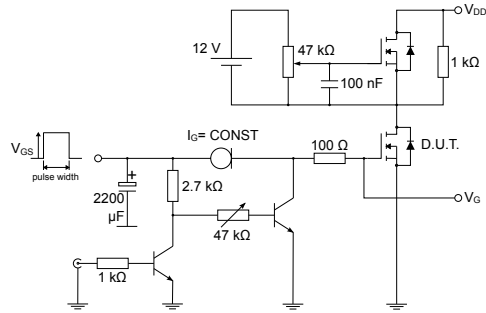
Figure 12. Output capacitance stored energy



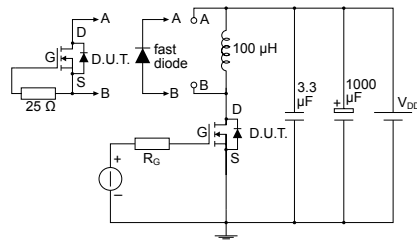
3 Test circuits

Figure 13. Test circuit for resistive load switching times


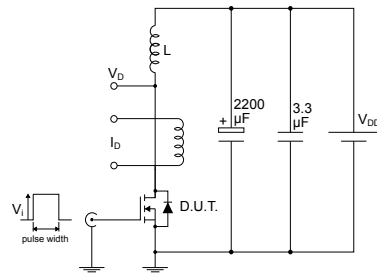
AM01468v1

Figure 14. Test circuit for gate charge behavior


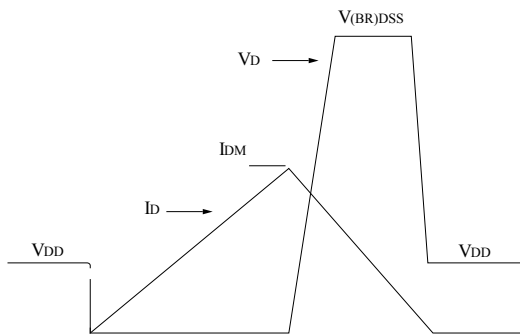
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Figure 15. Test circuit for inductive load switching and diode recovery times


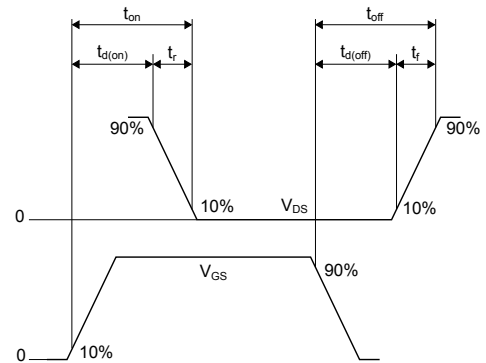
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Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


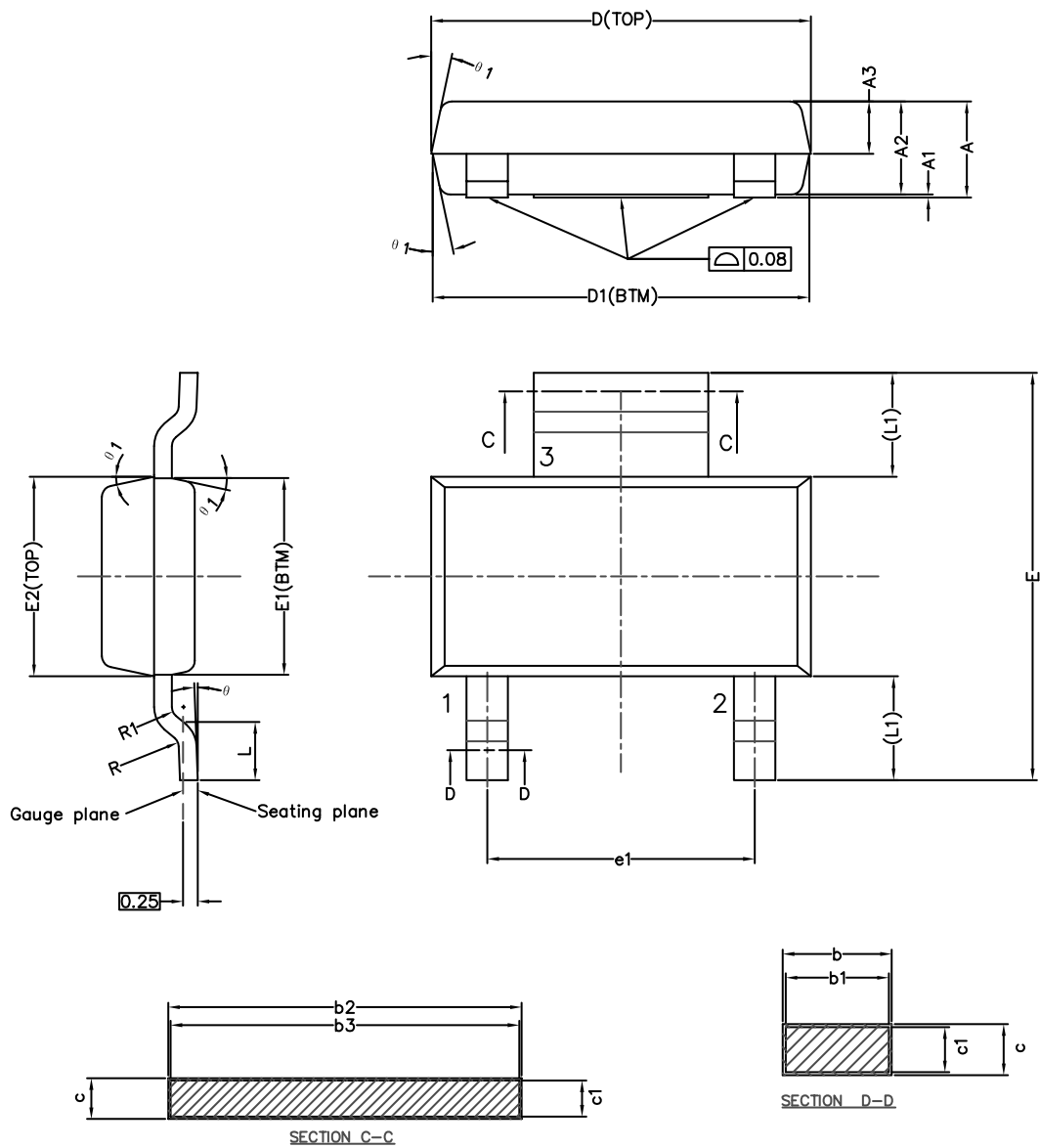
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT223-2 package information

Figure 19. SOT223-2 package outline

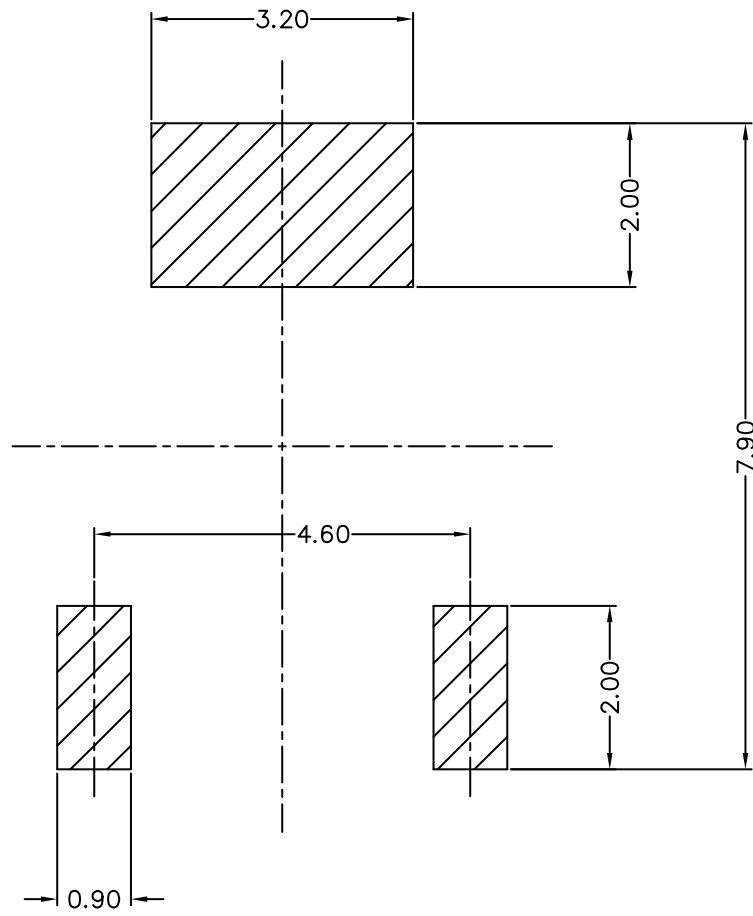


DM00320690_2

Table 8. SOT223-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.80
A1	0.02		0.10
A2	1.50	1.60	1.70
A3	0.80	0.90	1.00
b	0.67		0.80
b1	0.66	0.71	0.76
b2	2.96		3.09
b3	2.95	3.00	3.05
c	0.30		0.35
c1	0.29	0.30	0.31
D	6.48	6.53	6.58
D1	6.43	6.48	6.53
E	6.80		7.20
E1	3.30	3.38	3.48
E2	3.33	3.43	3.53
e1	4.50	4.60	4.70
L	0.80	1.00	1.20
L1	1.78 REF		
R	0.10		
R1	0.10		
θ	0°		8°
θ_1	10°	12°	14°

Figure 20. SOT223-2 recommended footprint (dimensions are in mm)



DM00320690_FP

Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Feb-2019	1	First release.
21-May-2020	2	Updated Table 1. Absolute maximum ratings and Table 7. Source-drain diode.

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