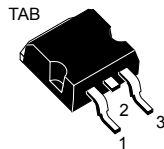
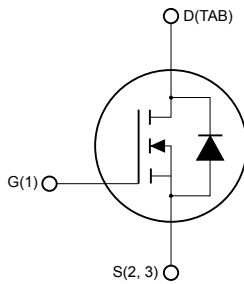


## Automotive-grade N-channel 1200 V, 1.45 $\Omega$ typ., 7 A, MDmesh K5 Power MOSFET in an H<sup>2</sup>PAK-2 package



 H<sup>2</sup>PAK-2


DTG1523NZ



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH12N120K5-2AG	1200 V	1.9 $\Omega$	7 A

- AEC-Q101 qualified 
- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STH12N120K5-2AG](#)

#### Product summary

Order code	STH12N120K5-2AG
Marking	12A120K5
Package	H <sup>2</sup> PAK-2
Packing	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current at $T_C = 25\text{ }^\circ\text{C}$	7	A
	Drain current at $T_C = 100\text{ }^\circ\text{C}$	4.6	
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	266	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_J$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 7\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ .
3.  $V_{DS} \leq 960\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.47	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of  $1\text{ inch}^2$ , 2oz Cu.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max)	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	1200	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	1200			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 1200\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 1200\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			50	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.5\text{ A}$		1.45	1.9	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	1364	-	pF
$C_{oss}$	Output capacitance		-	85	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }960\text{ V}$	-	82	-	pF
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance		-	32	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 960\text{ V}$ , $I_D = 7\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	36	-	nC
$Q_{gs}$	Gate-source charge		-	9.5	-	nC
$Q_{gd}$	Gate-drain charge		-	18.8	-	nC

1. Time-related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

2. Energy-related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 600\text{ V}$ , $I_D = 3.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	17	-	ns
$t_r$	Rise time		-	4	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	57	-	ns
$t_f$	Fall time		-	35.5	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}$	Source-drain current (pulsed)		-		12	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$	-	390		ns
$Q_{rr}$	Reverse recovery charge		-	5.0		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	24.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	542		ns
$Q_{rr}$	Reverse recovery charge		-	6.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	21.4	

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

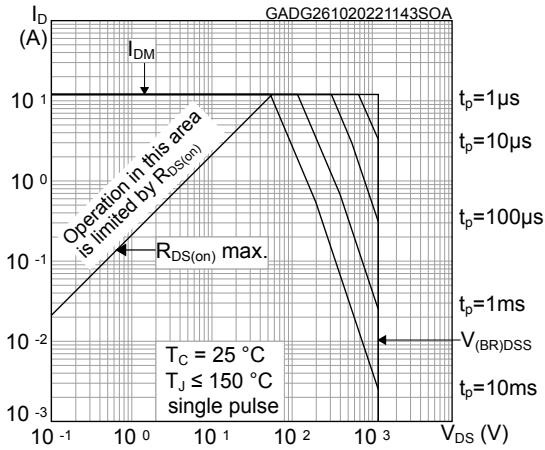


Figure 2. Maximum transient thermal impedance

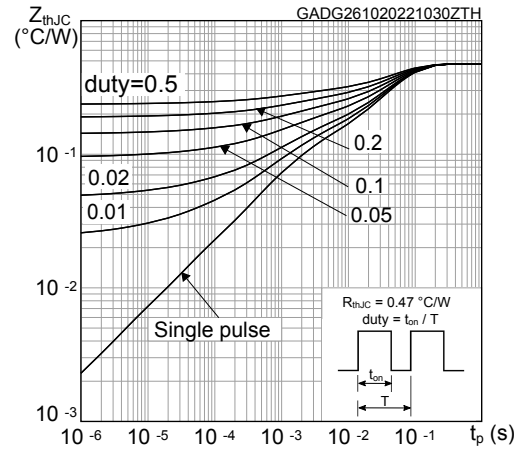


Figure 3. Typical output characteristics

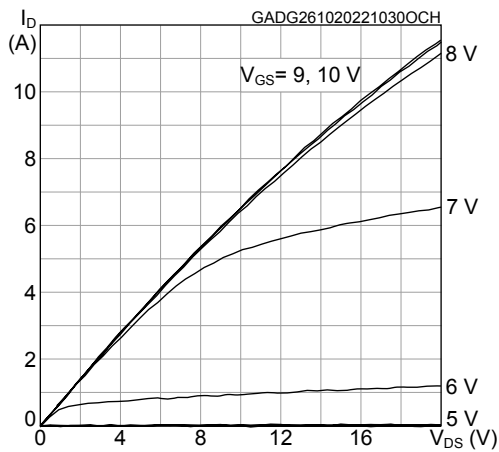


Figure 4. Typical transfer characteristics

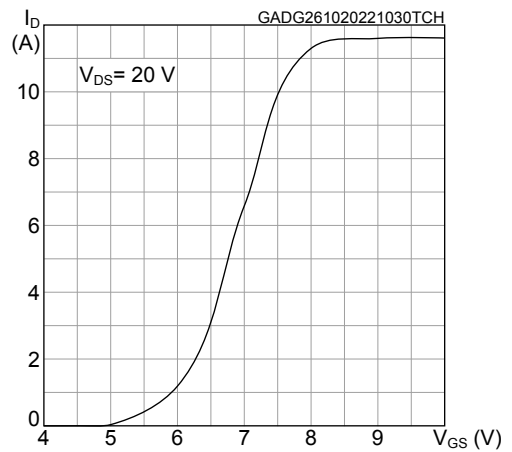


Figure 5. Typical gate charge characteristics

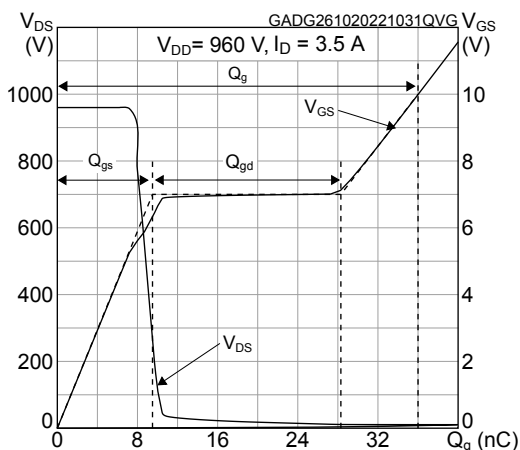
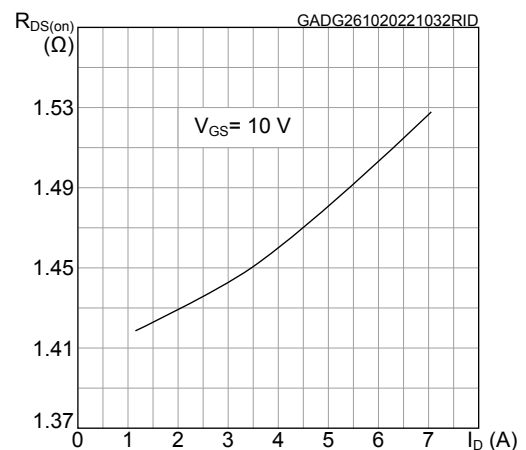
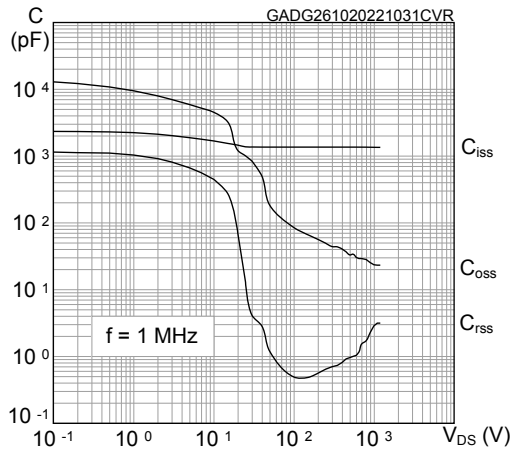


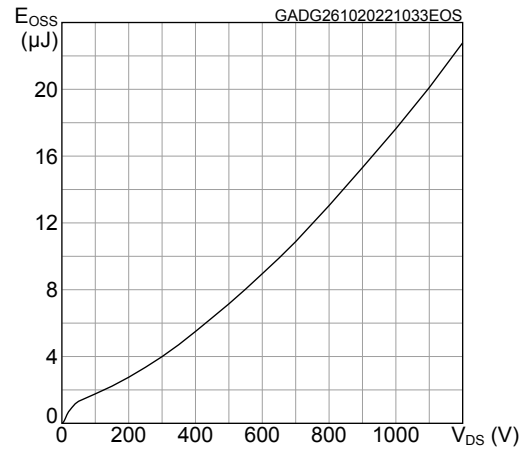
Figure 6. Typical drain-source on-resistance



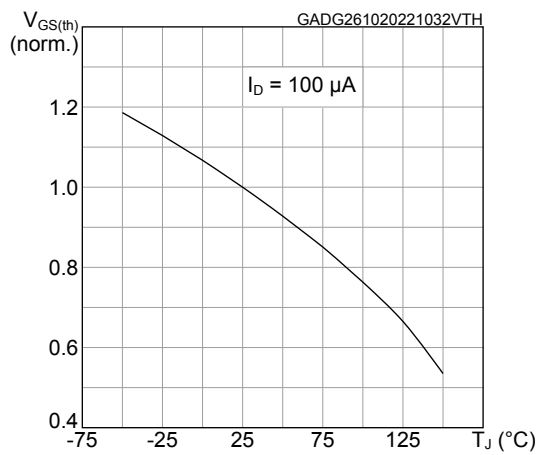
**Figure 7. Typical capacitance characteristics**



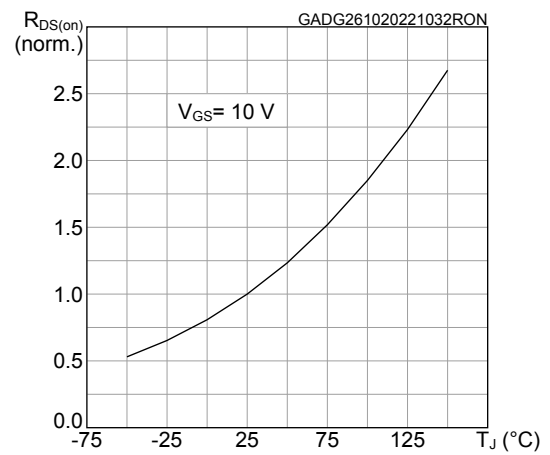
**Figure 8. Typical output capacitance stored energy**



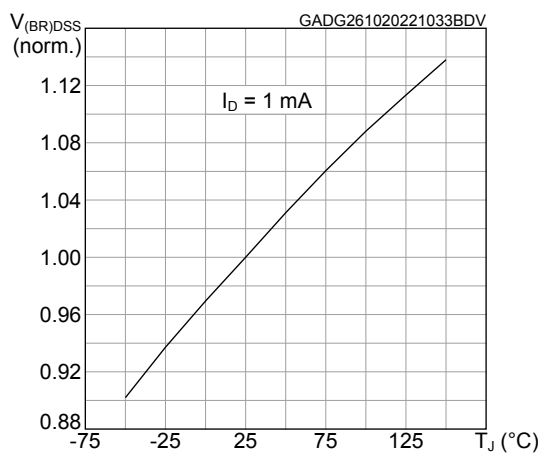
**Figure 9. Normalized gate threshold vs temperature**



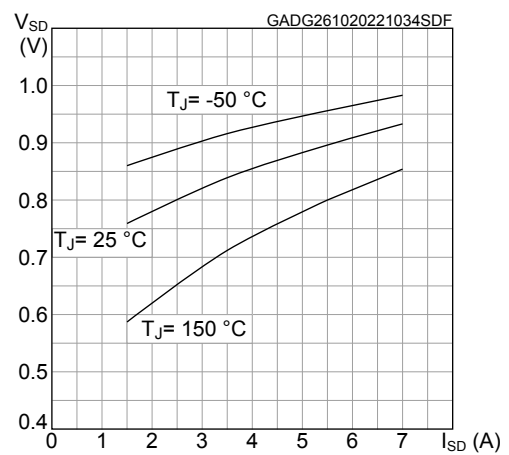
**Figure 10. Normalized on-resistance vs temperature**



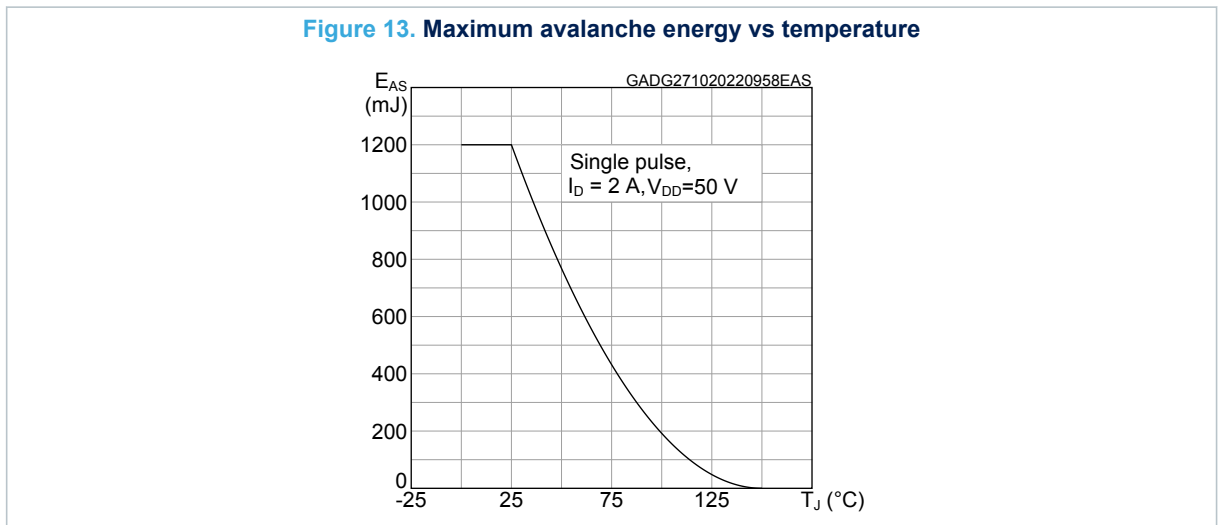
**Figure 11. Normalized breakdown voltage vs temperature**



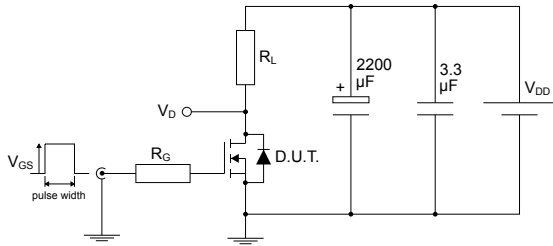
**Figure 12. Typical reverse diode forward characteristics**



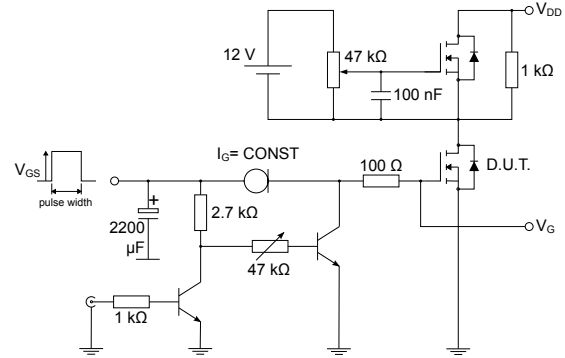
**Figure 13. Maximum avalanche energy vs temperature**



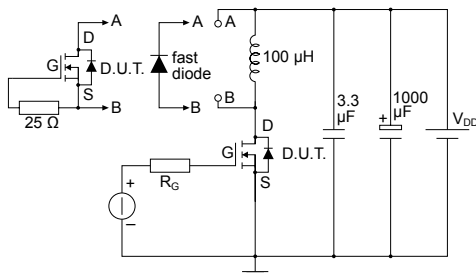
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


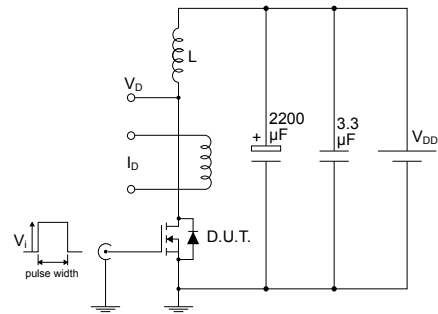
AM01468v1

**Figure 15. Test circuit for gate charge behavior**


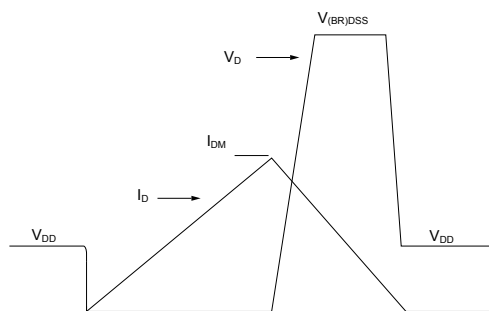
AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**


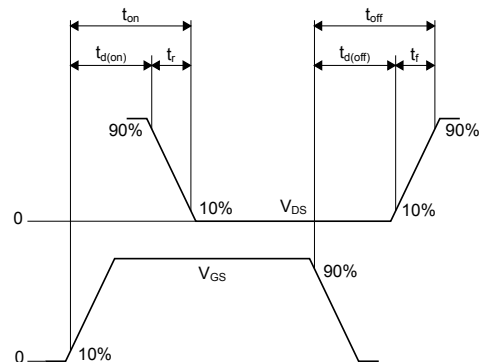
AM01470v1

**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1

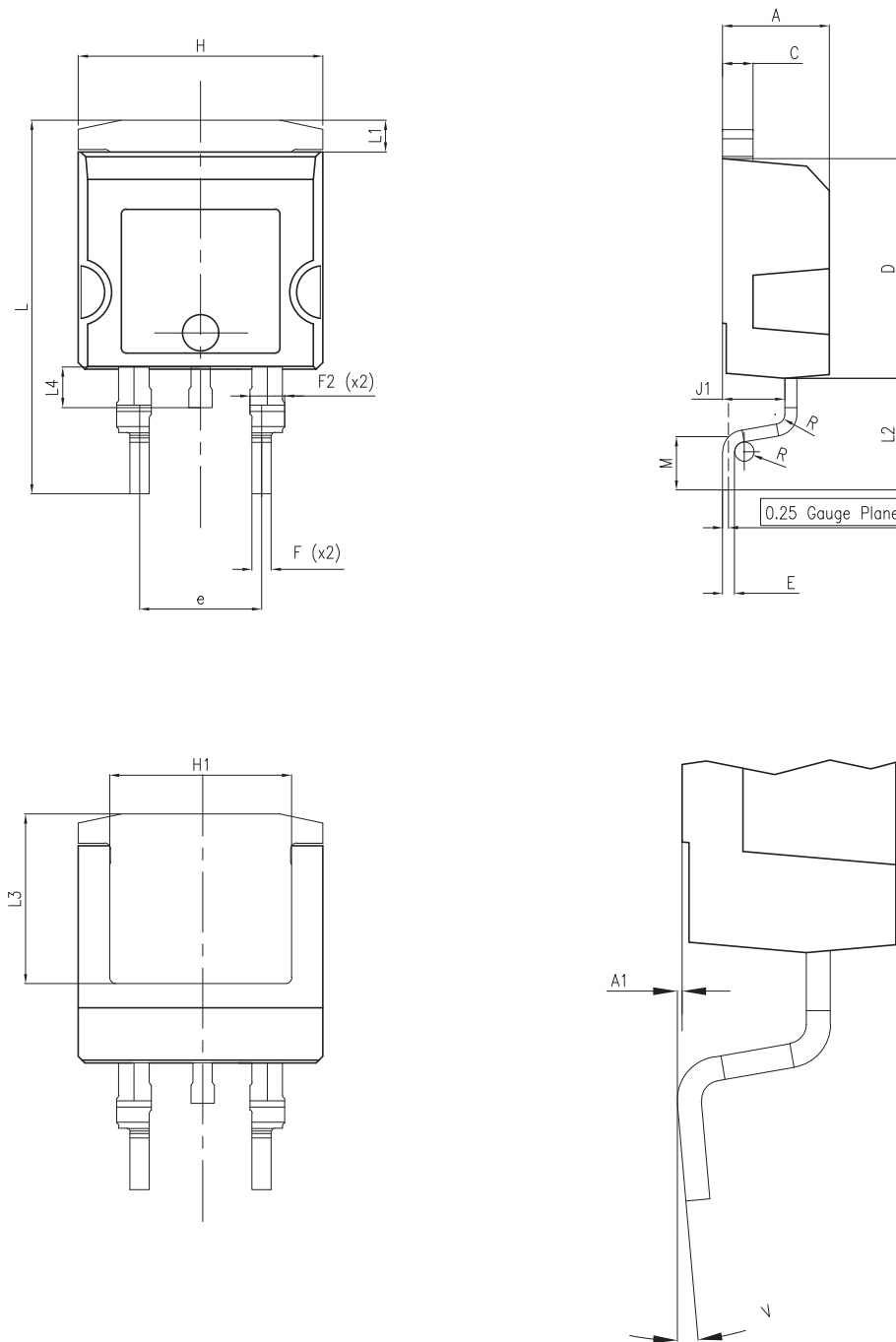


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

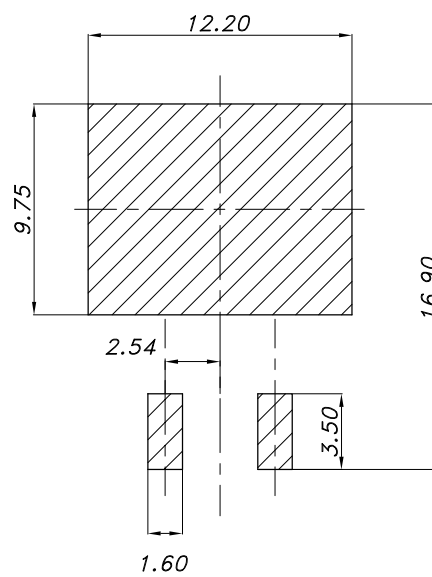
Figure 20. H<sup>2</sup>PAK-2 package outline



**Table 8. H<sup>2</sup>PAK-2 package mechanical data**

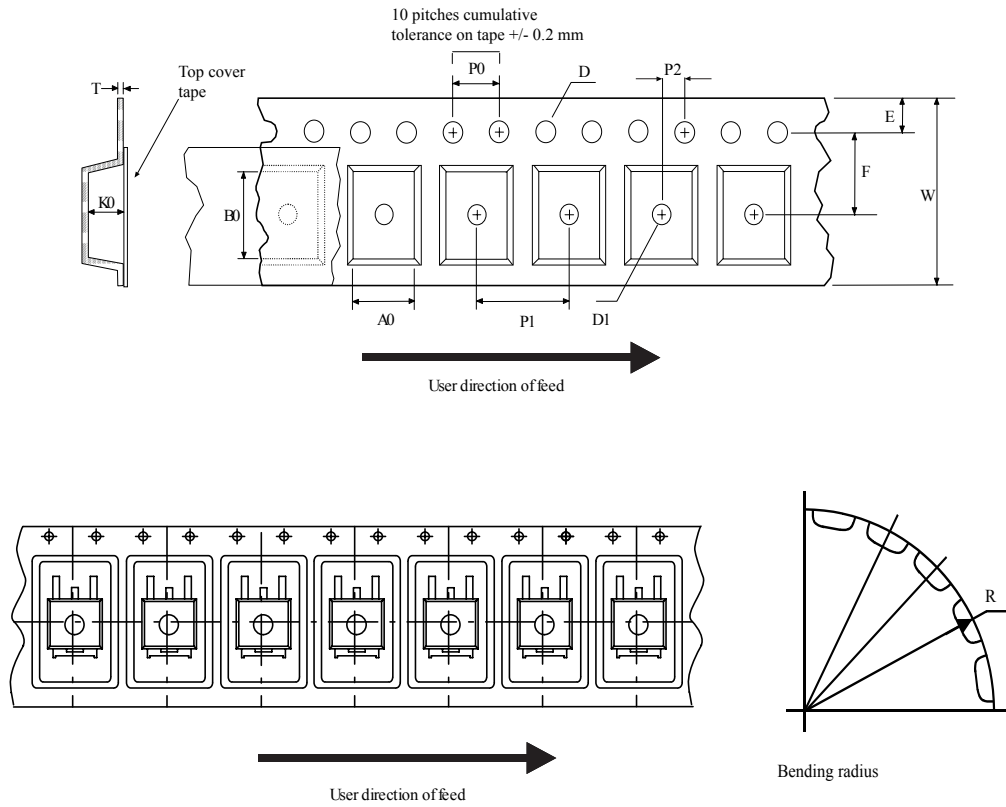
Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40		7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

**Figure 21. H<sup>2</sup>PAK-2 recommended footprint**

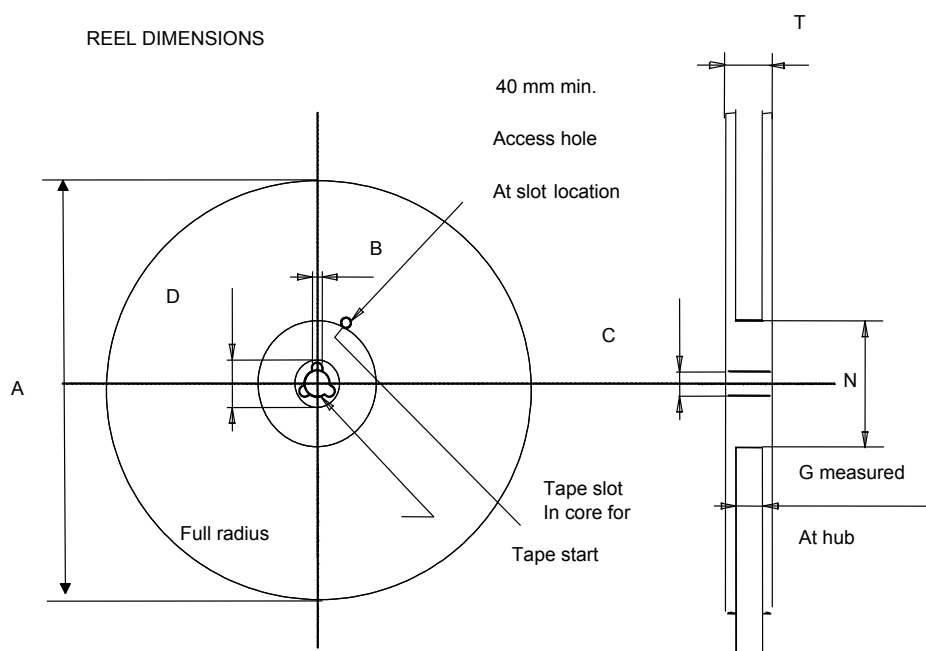


8159712\_10

*Note:* Dimensions are in mm.

**4.2 H<sup>2</sup>PAK-2 packing information**
**Figure 22. Tape outline**


AM08852v2

**Figure 23. Reel outline**


**Table 9. Tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

Table 10. Document revision history

Date	Revision	Changes
28-Oct-2022	1	First release.

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