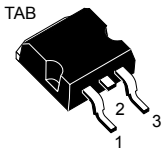
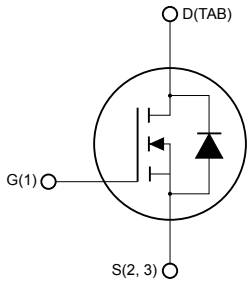
STH10N80K5-2AG

Datasheet

Automotive-grade N-channel 800 V, 0.60 Ω typ., 8 A MDmesh K5 Power MOSFET in an H²PAK-2 package



H²PAK-2



DTG1S23NZ

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH10N80K5-2AG	800 V	0.68 Ω	8 A

- AEC-Q101 qualified
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STH10N80K5-2AG

Product summary	
Order code	STH10N80K5-2AG
Marking	10N80K5
Package	H²PAK-2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	8	A
	Drain current (continuous) at T_C = 100 °C	5	A
I_{DM} (1)	Drain current (pulsed)	20	A
P_{TOT}	Total power dissipation at T_C = 25 °C	121	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 8 A, di/dt ≤ 100 A/µs; V_{DS} peak ≤ $V_{(BR)DSS}$.*
3. *V_{DS} ≤ 640 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.03	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	30	°C/W

1. *When mounted on FR-4 board of 1 inch², 2 oz Cu.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max)	2.7	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	250	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		0.60	0.68	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	426	-	pF
C_{oss}	Output capacitance		-	41	-	pF
C_{rss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{o(er)}$(1)	Equivalent capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 640 V	-	30	-	pF
$C_{o(tr)}$(2)	Equivalent capacitance time related		-	83	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz , I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 720 V, I_D = 8 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	17.3	-	nC
Q_{gs}	Gate-source charge		-	3.4	-	nC
Q_{gd}	Gate-drain charge		-	12.3	-	nC

1. *Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 400 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	14	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	34	-	ns
t_f	Fall time		-	14	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM}(1)	Source-drain current (pulsed)		-		20	A
V_{SD}(2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	436		ns
Q_{rr}	Reverse recovery charge		-	3.97		µC
I_{RRM}	Reverse recovery current		-	18		A
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	610		ns
Q_{rr}	Reverse recovery charge		-	4.85		µC
I_{RRM}	Reverse recovery current		-	16		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

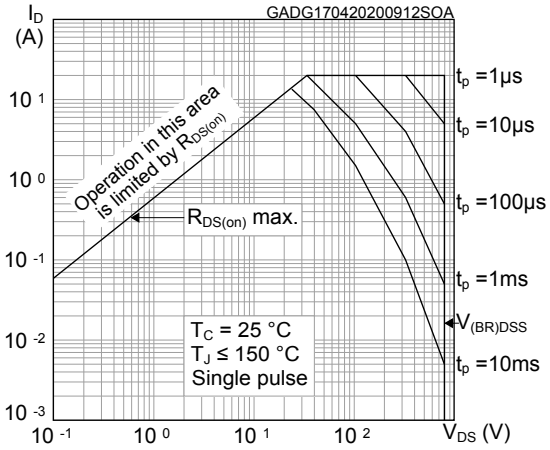


Figure 2. Maximum transient thermal impedance

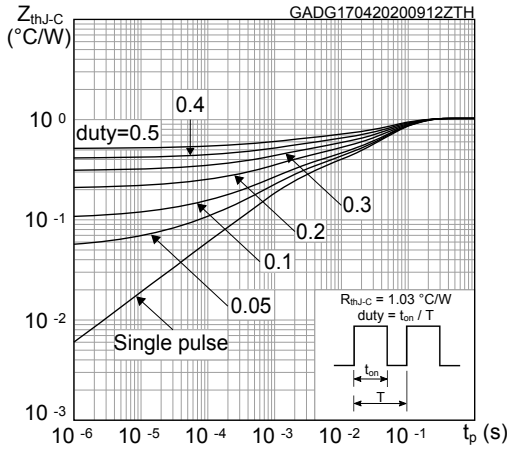


Figure 3. Typical output characteristics

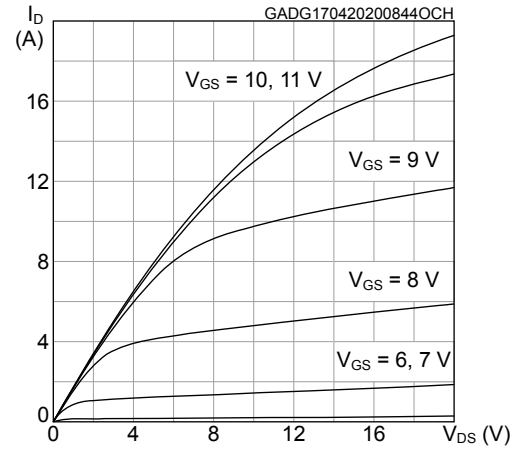


Figure 4. Typical transfer characteristics

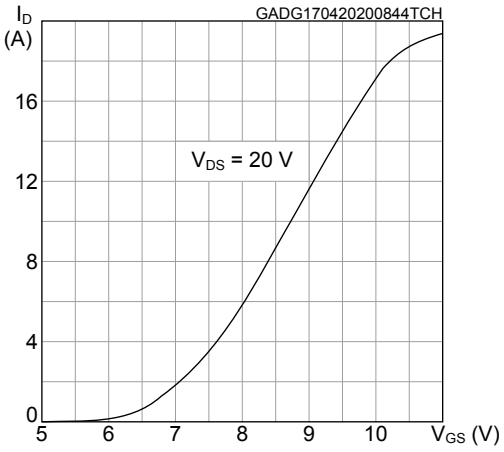


Figure 5. Typical gate charge characteristics

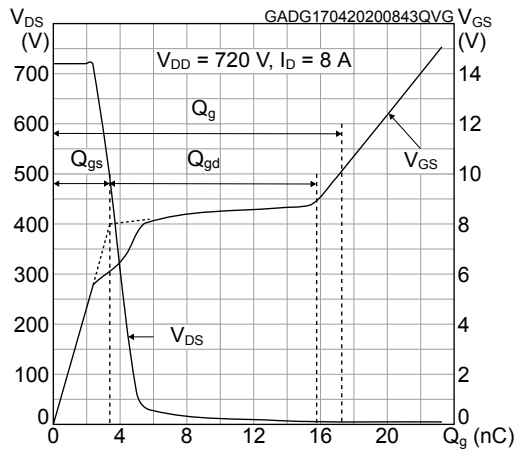


Figure 6. Typical drain-source on-resistance

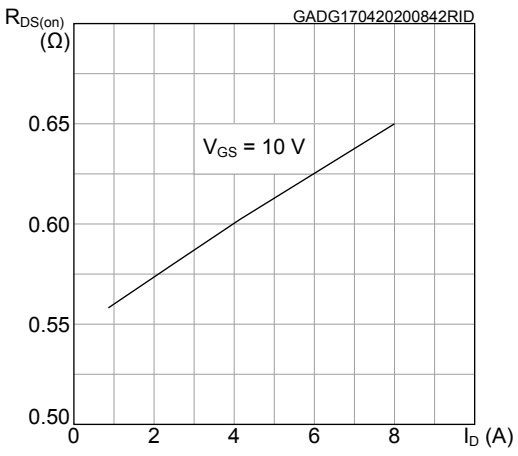


Figure 7. Typical capacitance characteristics

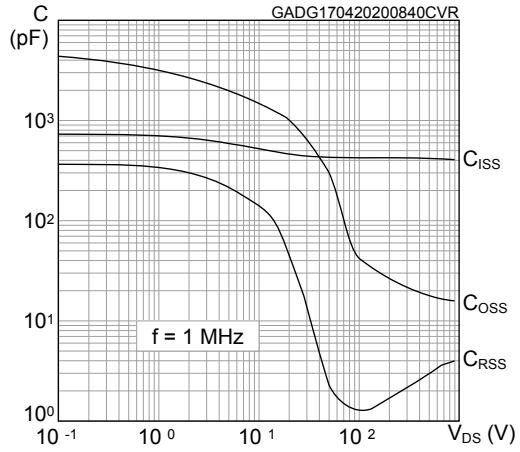


Figure 8. Normalized gate threshold vs temperature

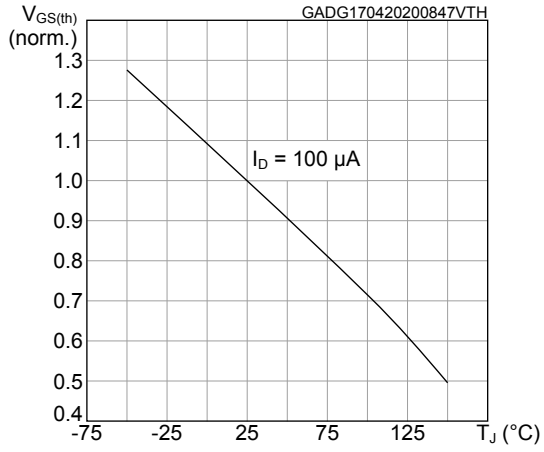


Figure 9. Normalized on-resistance vs temperature

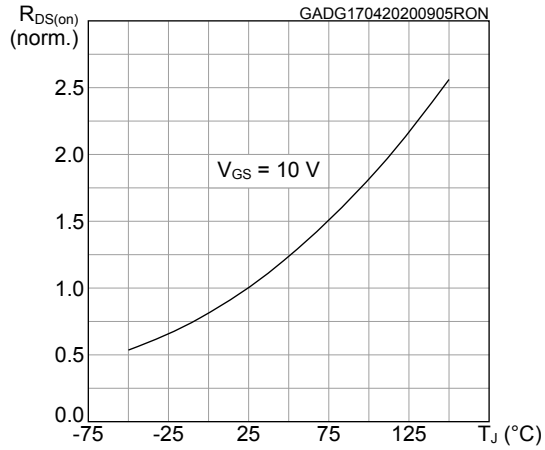


Figure 10. Normalized breakdown voltage vs temperature

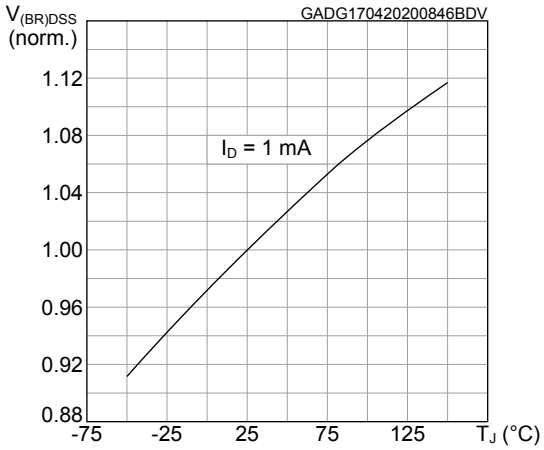


Figure 11. Maximum avalanche energy vs starting T_J

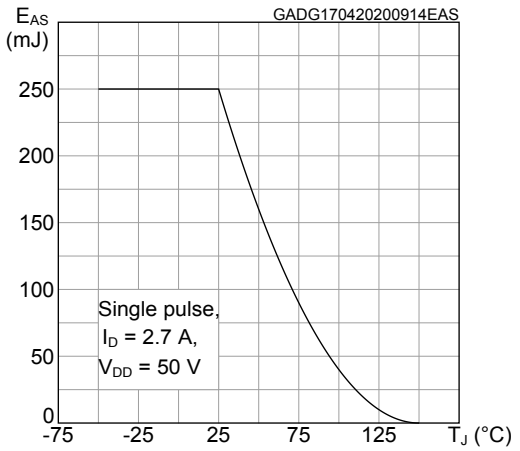
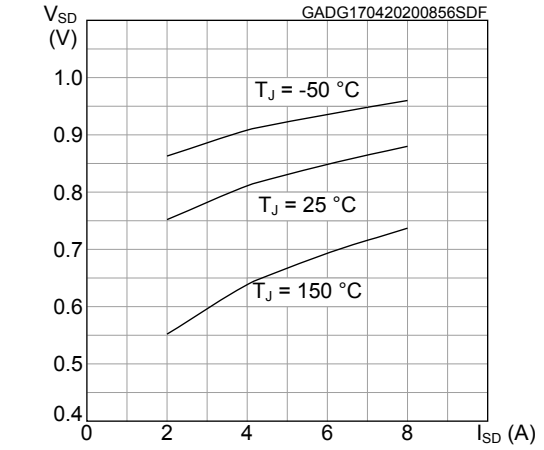


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

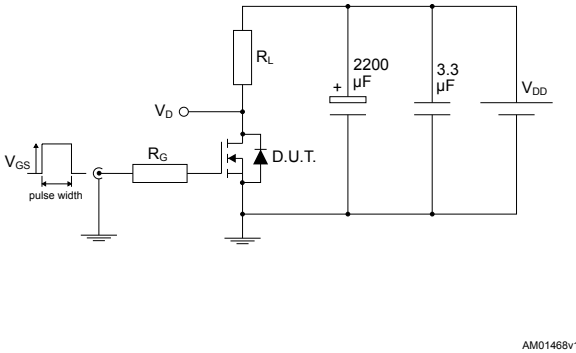


Figure 14. Test circuit for gate charge behavior

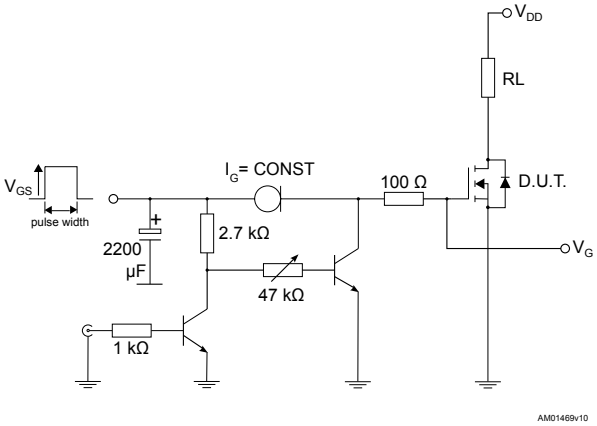


Figure 15. Test circuit for inductive load switching and diode recovery times

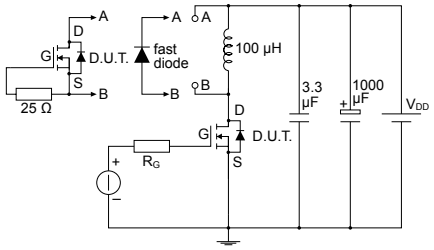


Figure 16. Unclamped inductive load test circuit

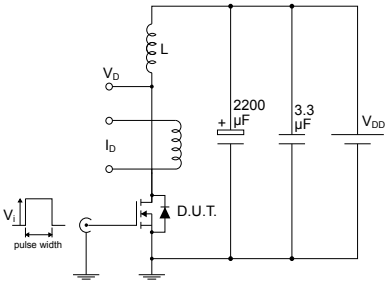


Figure 17. Unclamped inductive waveform

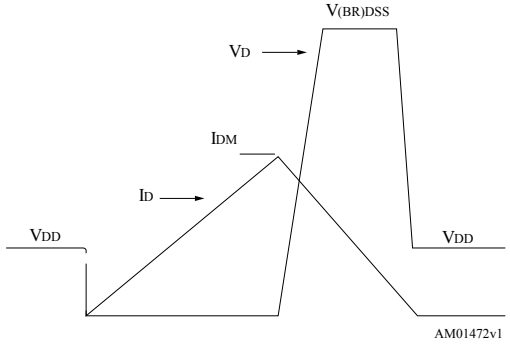
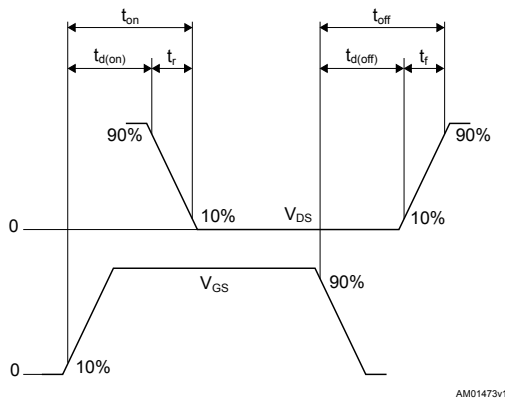


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 19. H²PAK-2 package outline

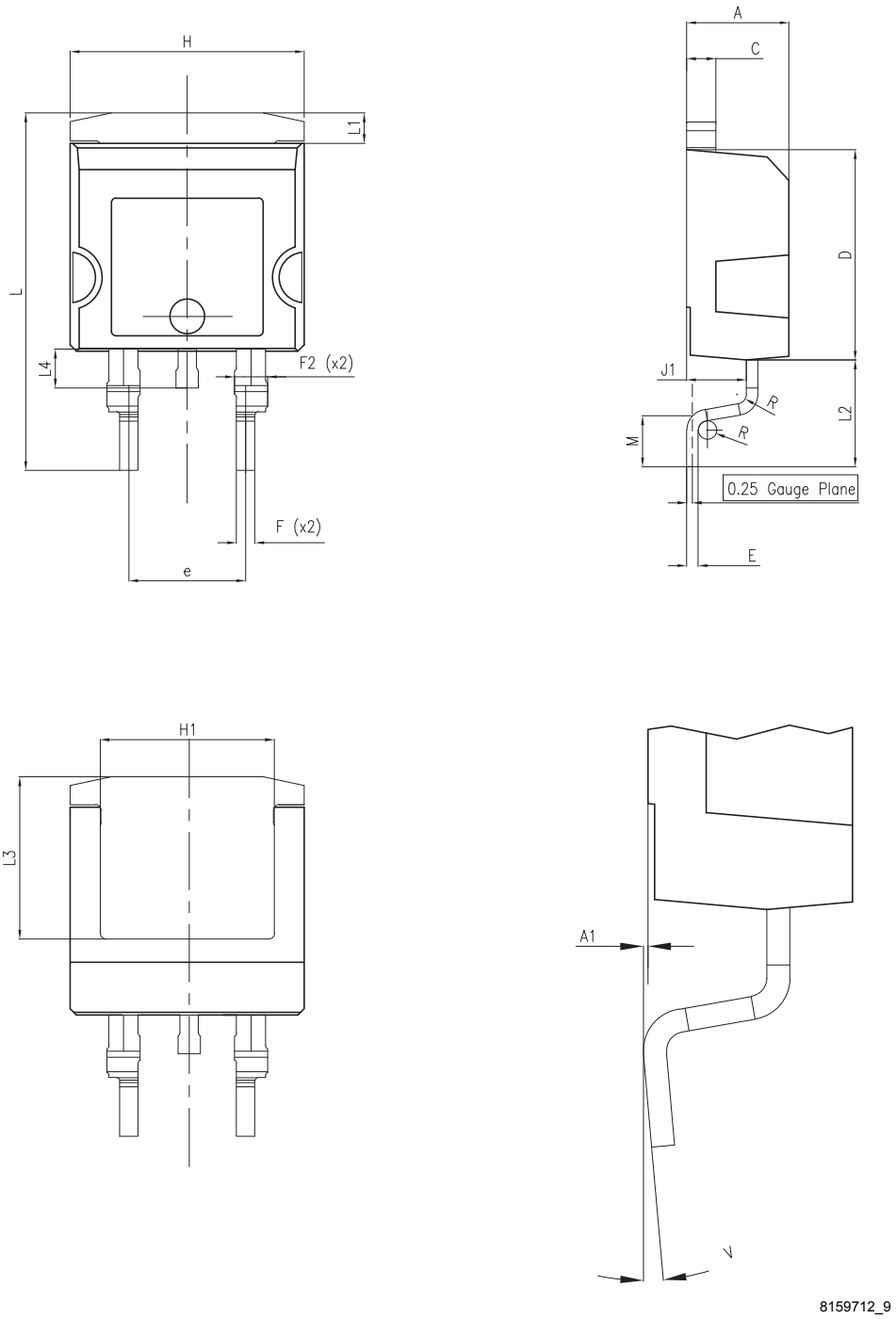
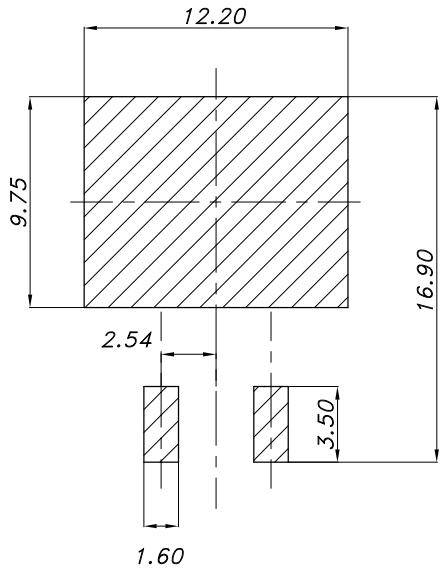


Table 8. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

Figure 20. H²PAK-2 recommended footprint



Note: Dimensions are in mm.

4.2 Packing information

Figure 21. **Tape outline**

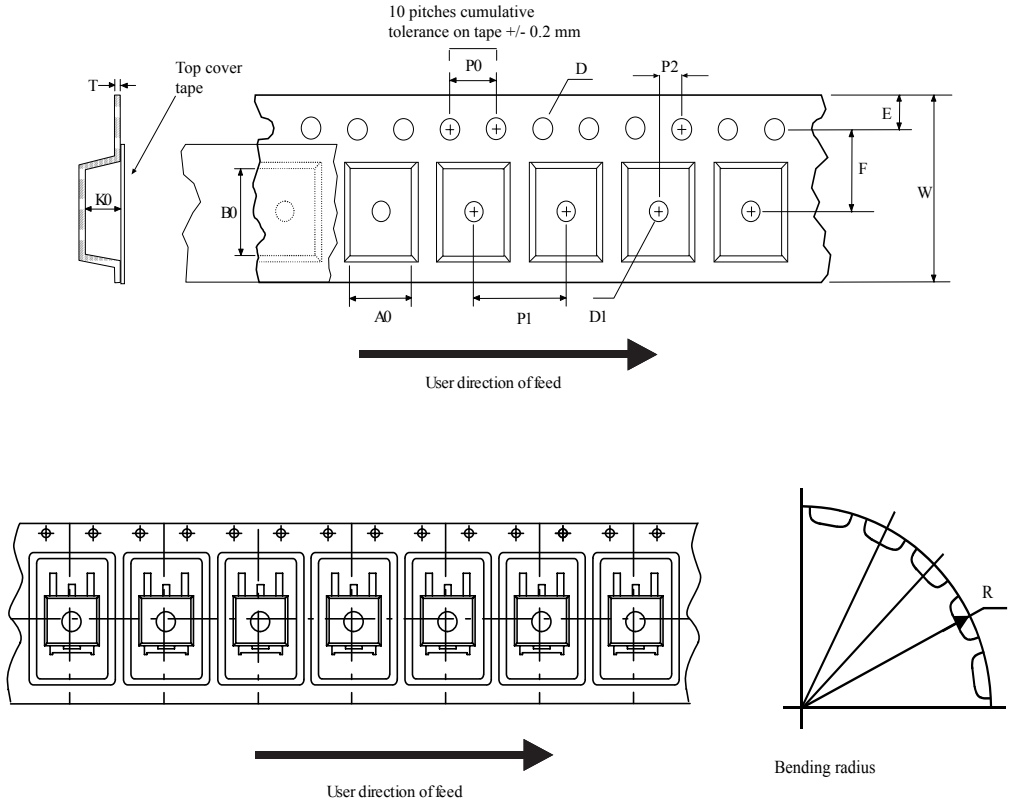


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Figure 22. **Reel outline**

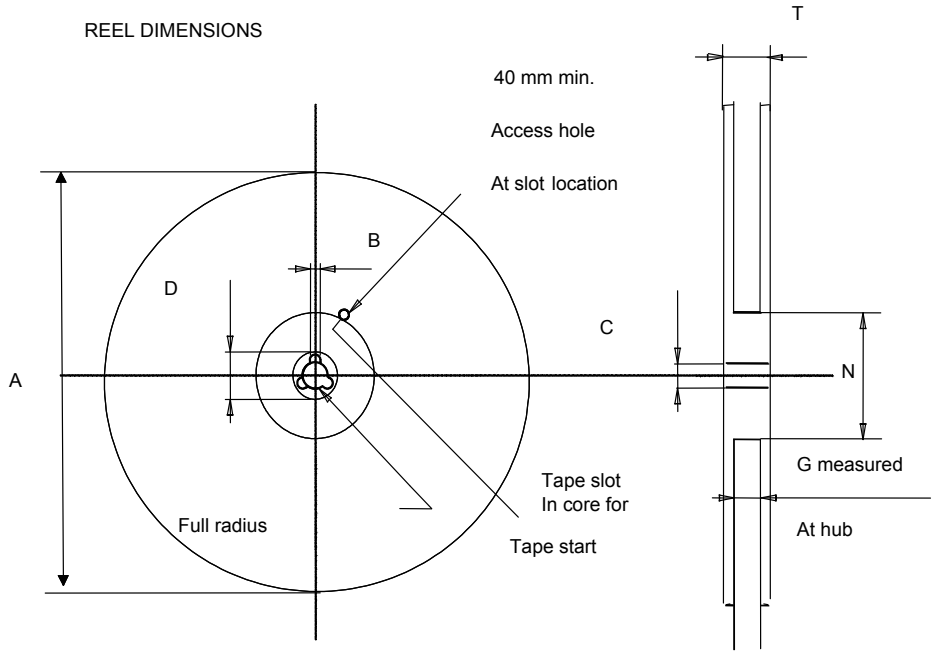

Table 9. **Tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
13-May-2020	1	First release.

Contents