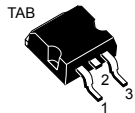
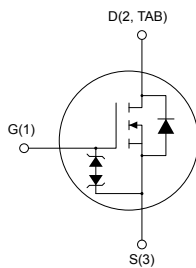



## Automotive-grade N-channel 650 V, 0.15 $\Omega$ typ., 20 A MDmesh M2 Power MOSFET in a D<sup>2</sup>PAK package


 D<sup>2</sup>PAK


AM01479V1

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB30N65M2AG	650 V	0.18 $\Omega$	20 A

- AEC-Q101 qualified 
- Extremely low gate charge
- Excellent output capacitance (C<sub>OSS</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.



#### Product status link

[STB30N65M2AG](#)

#### Product summary

<b>Order code</b>	STB30N65M2AG
<b>Marking</b>	30N65M2
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	13	A
$I_{DM}^{(1)}$	Drain current (pulsed)	55	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	190	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	2.4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	760	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 20\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS}$  peak  $< V_{(BR)DSS}$ ,  $V_{DD} = 520\text{ V}$ .
3.  $V_{DS} \leq 520\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.66	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$		0.15	0.18	$\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1440	-	pF
$C_{oss}$	Output capacitance		-	60	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.5	-	pF
$C_{oss\ eq}$ <sup>(1)</sup>	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$	-	307	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4.9	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 20\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	30.8	-	nC
$Q_{gs}$	Gate-source charge		-	6.8	-	nC
$Q_{gd}$	Gate-drain charge		-	10.2	-	nC

1.  $C_{oss\ eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$ , $I_D = 10\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	15	-	ns
$t_r$	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	58	-	ns
$t_f$	Fall time		-	10	-	ns

**Table 6. Source drain diode**

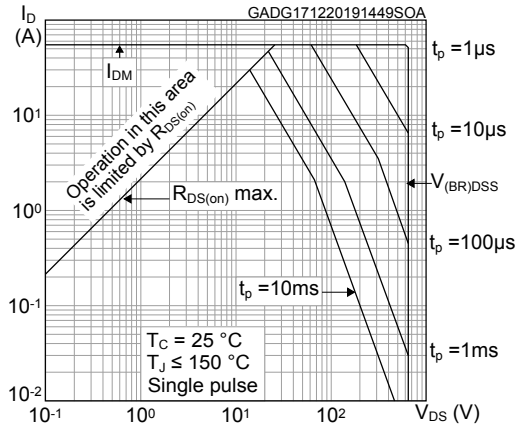
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		55	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}, V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	250		ns
$Q_{rr}$	Reverse recovery charge		-	2.0		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	16		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 60\text{ V}, T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	380		ns
$Q_{rr}$	Reverse recovery charge		-	3.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18		A

1. Pulse width limited by safe operating area.

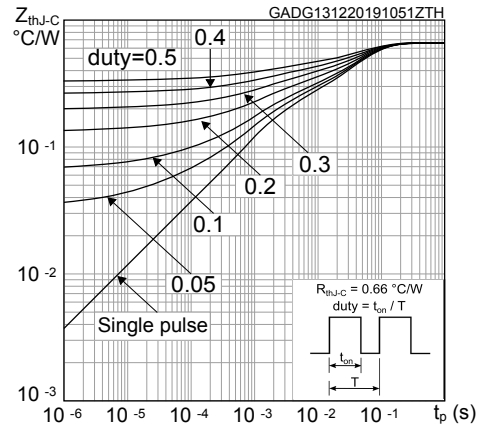
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

## 2.1 Electrical characteristics (curves)

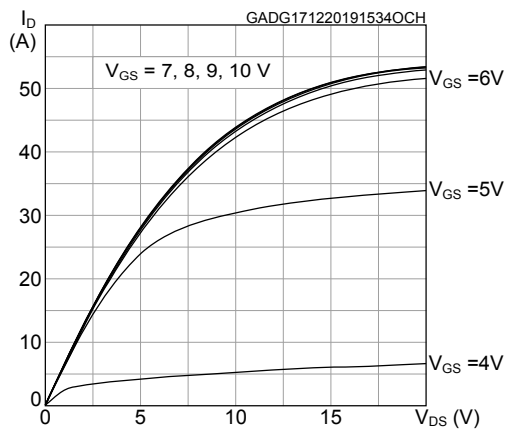
**Figure 1. Safe operating area**



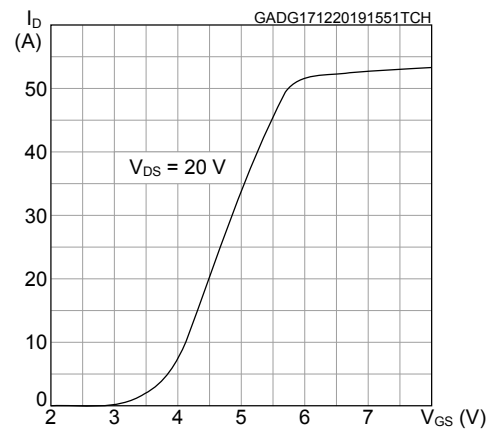
**Figure 2. Maximum transient thermal impedance**



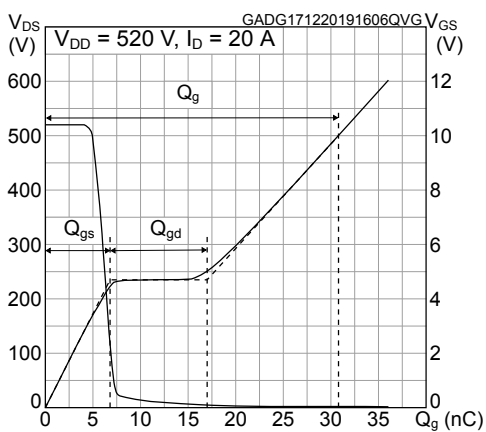
**Figure 3. Typical output characteristics**



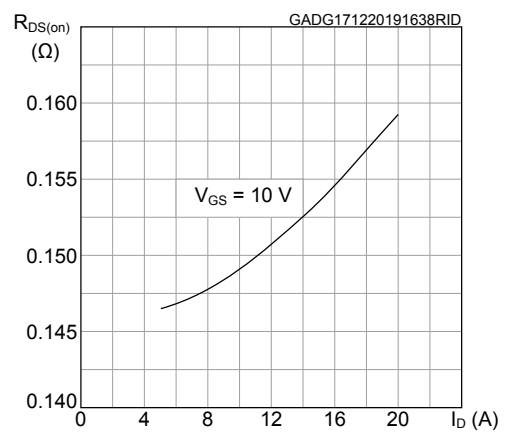
**Figure 4. Typical output characteristics**



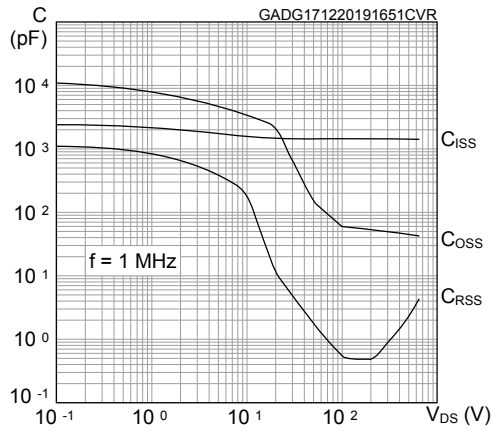
**Figure 5. Typical gate charge characteristics**



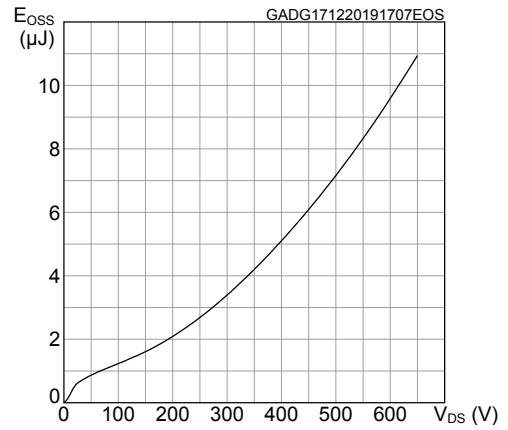
**Figure 6. Typical drain-source on-resistance**



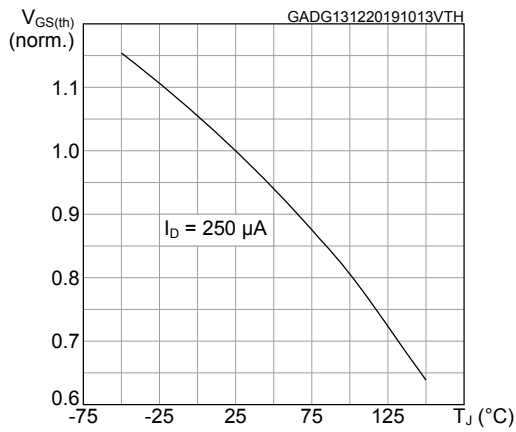
**Figure 7. Typical capacitance characteristics**



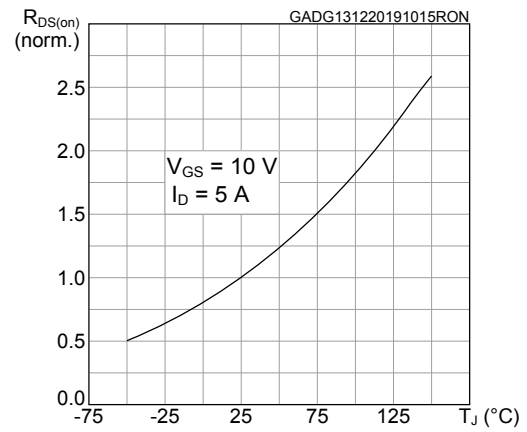
**Figure 8. Typical output capacitance stored energy**



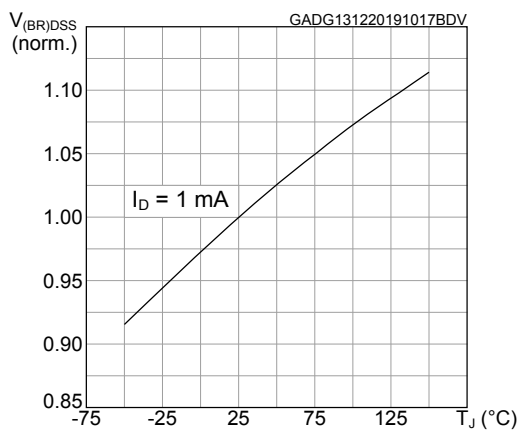
**Figure 9. Normalized gate threshold vs temperature**



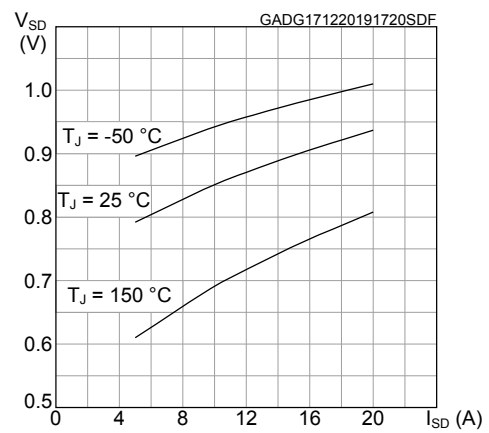
**Figure 10. Normalized on-resistance vs temperature**



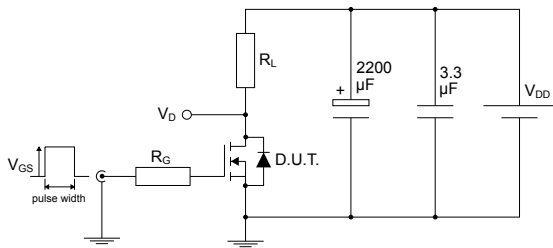
**Figure 11. Normalized breakdown voltage vs temperature**



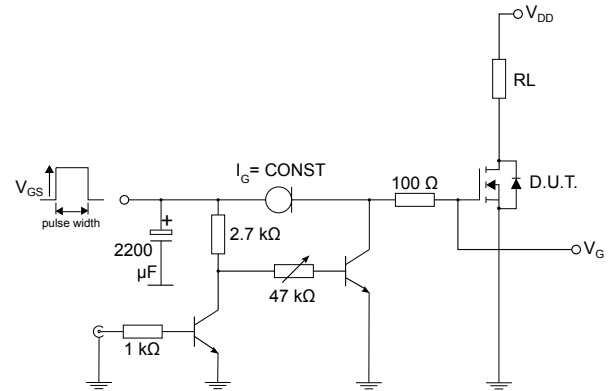
**Figure 12. Typical reverse diode forward characteristics**



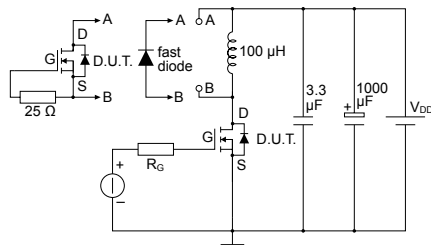
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


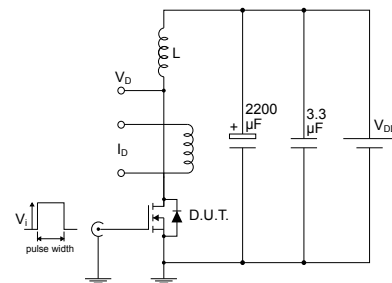
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


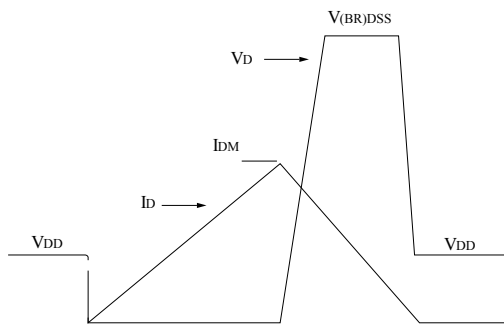
AM01469v10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


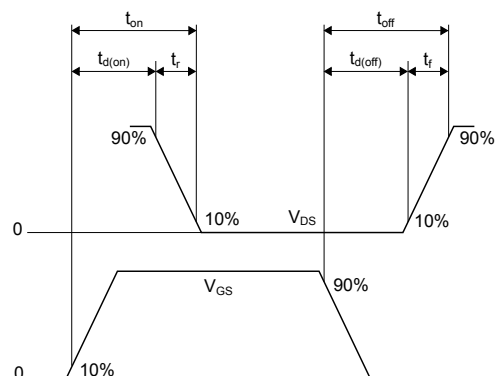
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


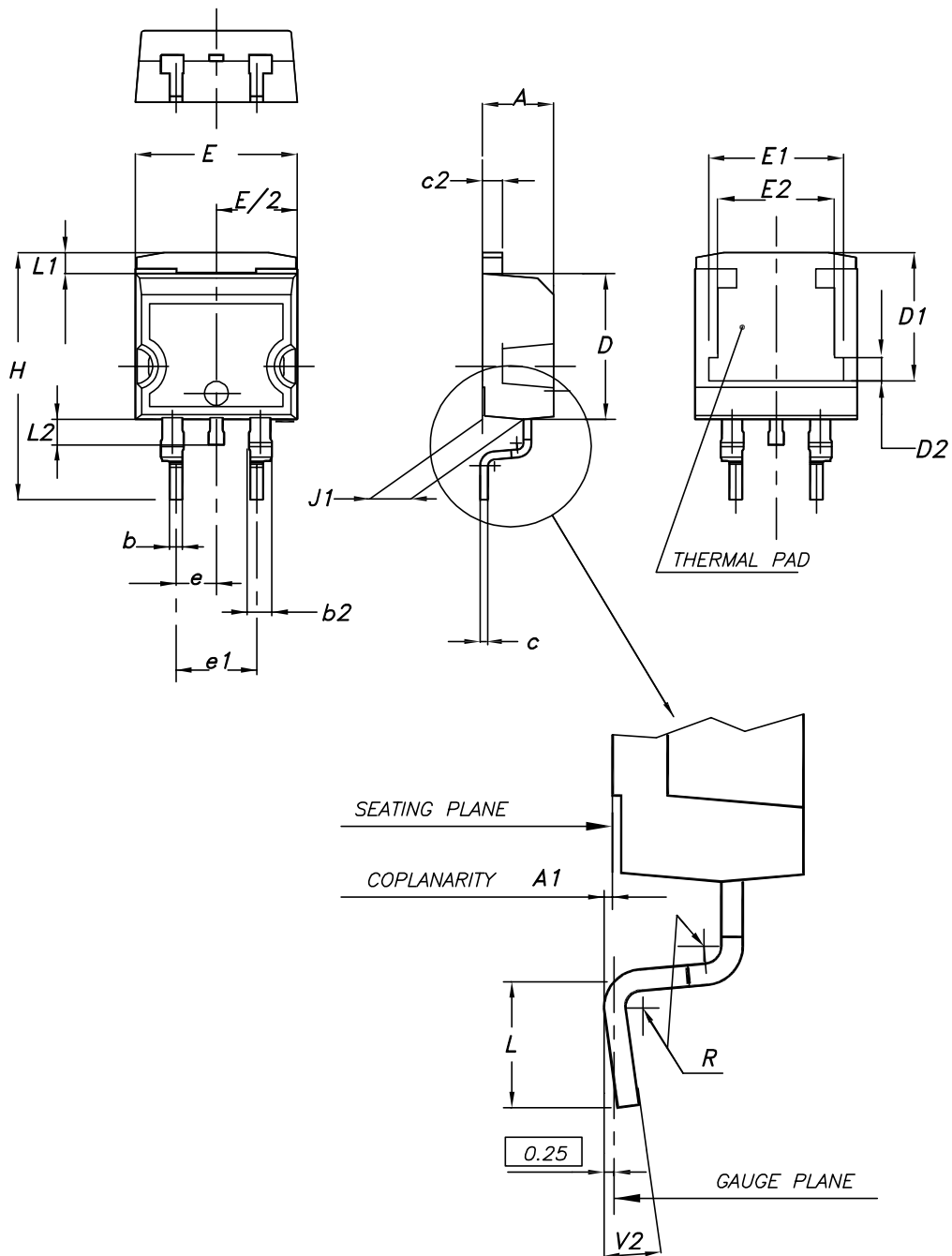
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

Figure 19. D<sup>2</sup>PAK (TO-263) type A package outline



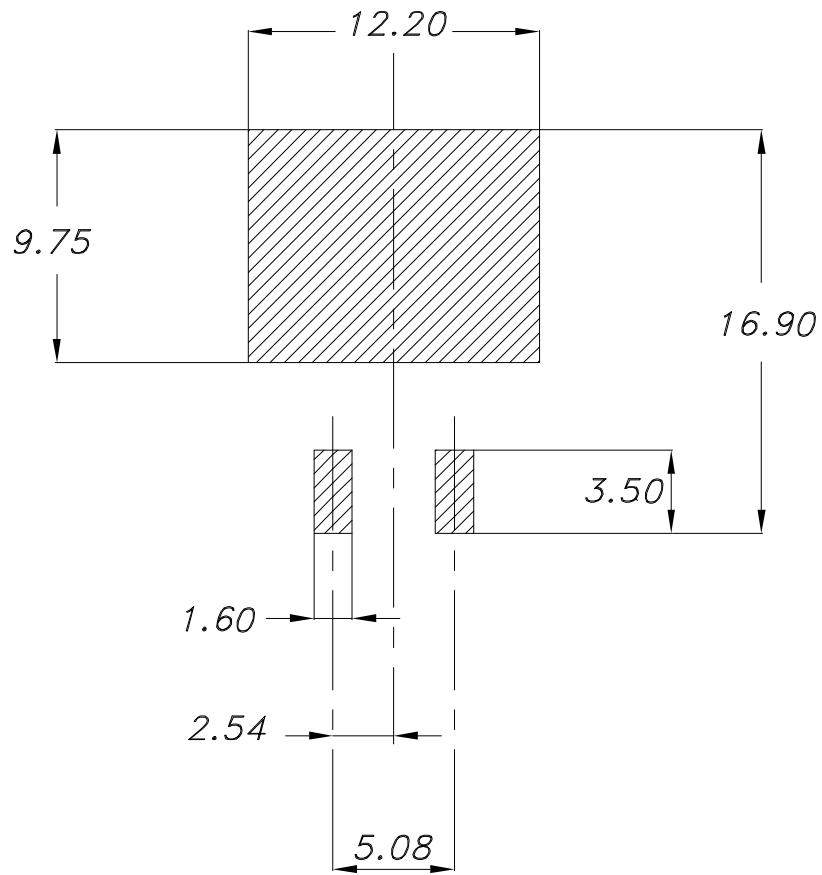
0079457\_26



**Table 7. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

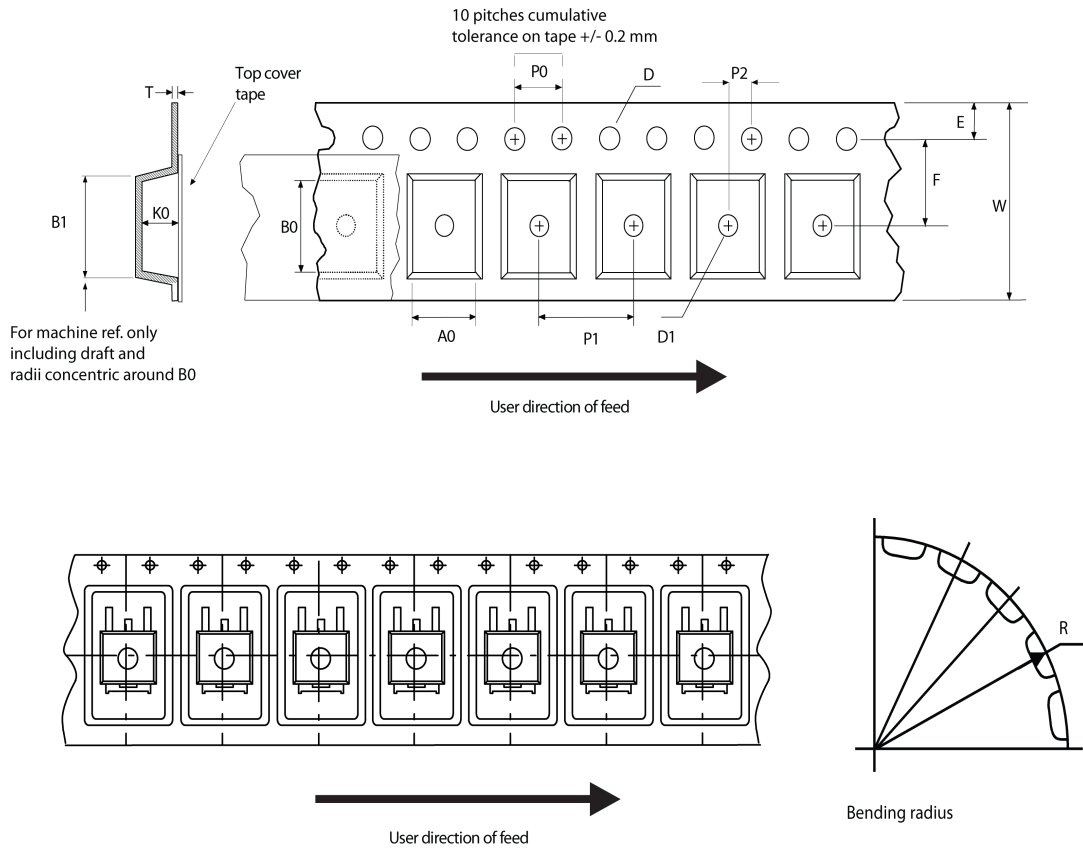
Figure 20. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



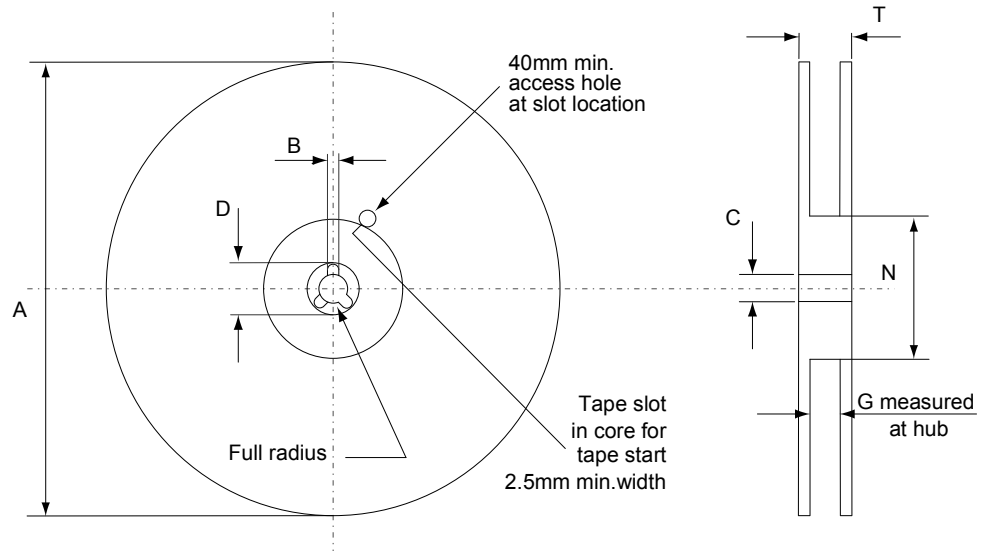
Footprint\_26

## 4.2 D<sup>2</sup>PAK packing information

**Figure 21. D<sup>2</sup>PAK tape outline**



AM08852v1

**Figure 22. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 8. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
05-Sep-2017	1	First release
18-Dec-2019	2	Updated <a href="#">Section 1</a> Electrical ratings. Updated <a href="#">Section 2</a> Electrical characteristics. Updated <a href="#">Section 2.1</a> Electrical characteristics (curves). Minor text changes.

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