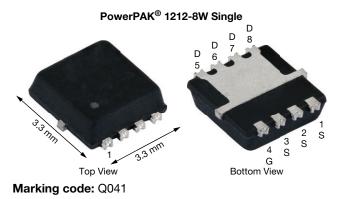
SQS840CENW

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Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET



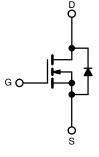
PRODUCT SUMMARY				
V _{DS} (V)	40			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.020			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.022			
I _D (A)	12			
Configuration	Single			
Package	PowerPAK 1212-8W			

FEATURES

- TrenchFET[®] power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



KOHS COMPLIANT HALOGEN FREE



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (7	Г _C = 25 °C, unles	s otherwise noted	(k		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	v	
Gate-source voltage		V _{GS}	± 20	v	
Continuous drain current ^a	T _C = 25 °C	1	12		
Continuous drain current ~	T _C = 125 °C	Ι _D	12		
Continuous source current (diode conduction) ^a		ا _S	12	А	
Pulsed drain current ^b		I _{DM}	24		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	19		
Single pulse avalanche energy	L = 0.1 IIIH	E _{AS}	18	mJ	
Maximum power dissipation ^b	T _C = 25 °C	Р	33	w	
	T _C = 125 °C	P _D	11	vv	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) e, f			260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^c	R _{thJA}	81	°C/W
Junction-to-case (drain)		R _{thJC}	4.5	C/VV

Notes

- a. Package limited
- b. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- c. When mounted on 1" square PCB (FR4 material)
- d. Parametric verification ongoing
- e. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8W is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

S19-0275-Rev. A, 25-Mar-2019 Document Number: 77821 For technical questions, contact: <u>automostechsupport@vishay.com</u>

SQS840CENW

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SPECIFICATIONS ($T_C = 25 \ ^{\circ}C$, u	nless otherv	vise noted)					
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static						•	
Drain-source breakdown voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	40	-	-	v
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	: V _{GS} , I _D = 250 μA	1.5	2.0	2.5	v
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, $V_{GS} = \pm 20 V$	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μA
		$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	20	-	-	А
		V _{GS} = 10 V	I _D = 7.5 A	-	0.014	0.020	
D · · · · · · · · · · · · · · · · · · ·	5	V _{GS} = 10 V	I _D = 7.5 A, T _J = 125 °C	-	-	0.034	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 7.5 A, T _J = 175 °C	-	-	0.042	Ω
		V _{GS} = 4.5 V	I _D = 6.5 A	-	0.015	0.022	
Forward transconductance b	9 _{fs}	V _{DS}	= 15 V, I _D = 10 A	-	62	-	S
Dynamic ^b		•				•	
Input capacitance	C _{iss}			-	825	1031	
Output capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	-	131	164	pF
Reverse transfer capacitance	C _{rss}			-	58	73	
Total gate charge ^c	Qq			-	15	22.5	
Gate-source charge ^c	Q _{qs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 4 \text{ A}$	-	2.8	-	nC
Gate-drain charge c	Q _{gd}			-	2.9	-	
Gate resistance	Rg		f = 1 MHz	1.6	3.3	5	Ω
Turn-on delay time ^c	t _{d(on)}			-	6.5	9.8	
Rise time ^c	t _r	Voo	= 20 V, $R_1 = 5 \Omega$	-	2.7	4	- ns
Turn-off delay time ^c	t _{d(off)}		$V_{\rm GEN} = 10 \rm V, R_g = 1 \Omega$	-	26	40	
Fall time ^c	t _f	-		-	4.3	6.5	
Source-Drain Diode Ratings and Charact							
Pulsed current ^a	I _{SM}			-	-	48	А
Forward voltage	V _{SD}	I _F =	4.8 A, V _{GS} = 0 V	-	0.82	1.2	V
Body diode reverse recovery time	t _{rr}	-		-	18	36	ns
Body diode reverse recovery charge	Q _{rr}	I _F = 5 A, di/dt = 100 A/μs		-	12	24	nC
Reverse recovery fall time	ta			-	11	-	1
Reverse recovery rise time	t _b	1		-	6	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			-	-1.3	-3	А

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

b. Guaranteed by design, not subject to production testing

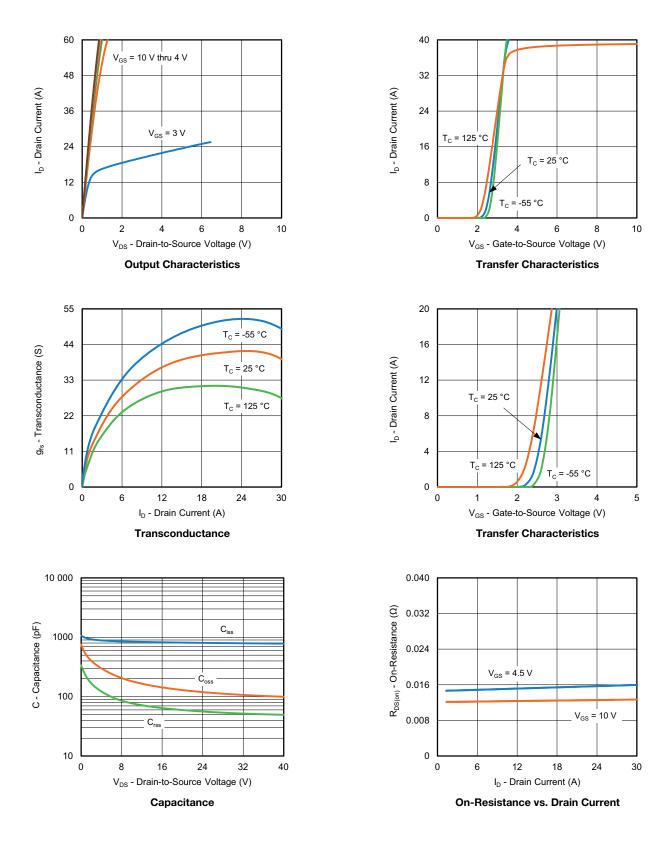
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c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



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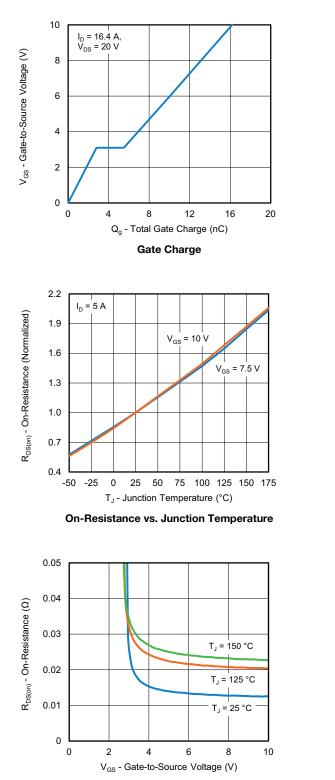
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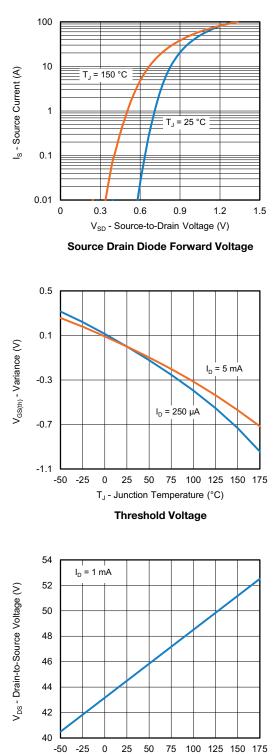
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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



On-Resistance vs. Gate-to-Source Voltage



 T_J - Junction Temperature (°C)

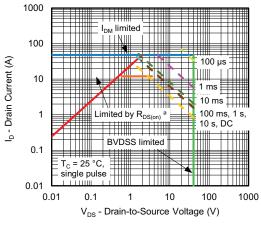
Drain Source Breakdown vs. Junction Temperature

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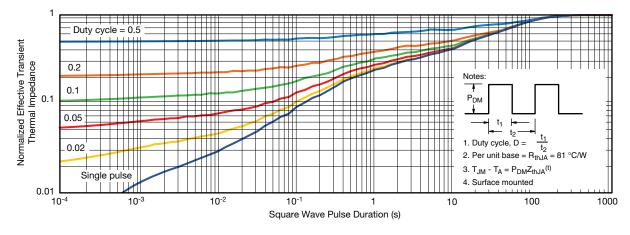
4



THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

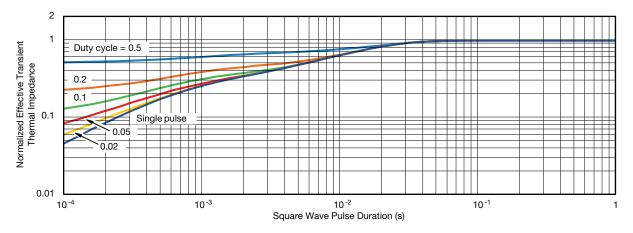
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

The characteristics shown in the two graphs

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- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

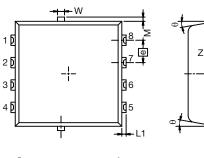
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77821.

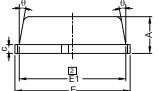


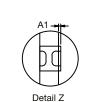
PowerPAK[®] 1212-8W Case Outline

Δ2

224



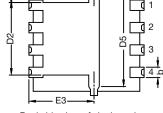




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Б



E2

E4

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Notes
1 Inch will govern

 Dimensions exclusive of mold gate burrs
 Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES				
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.			
А	0.97	1.04	1.12	0.038	0.041	0.044		
A1	0	-	0.05	0	-	0.002		
A2	0	-	0.13	0	-	0.005		
b	0.23	0.30	0.41	0.009	0.012	0.016		
С	0.23	0.28	0.33	0.009	0.011	0.013		
D	3.20	3.30	3.40	0.126	0.130	0.134		
D1	2.95	3.05	3.15	0.116	0.120	0.124		
D2	1.98	2.11	2.24	0.078	0.083	0.088		
D4	0.47 typ.			0.0185 typ.				
D5		2.3 typ.		0.090 typ.				
E	3.20	3.30	3.40	0.126	0.130	0.134		
E1	2.95	3.05	3.15	0.116	0.120	0.124		
E2	1.47	1.60	1.73	0.058	0.063	0.068		
E3	1.75	1.85	1.98	0.069	0.073	0.078		
E4		0.34 typ.			0.013 typ.			
е	0.65 BSC.			0.026 BSC				
К		0.86 typ.		0.034 typ.				
Н	0.30	0.41	0.51	0.012	0.016	0.020		
L	0.30	0.43	0.56	0.012	0.017	0.022		
L1	0.06	0.13	0.20	0.002	0.005	0.008		
θ	0°	-	12°	0°	-	12°		
W	0.15	0.25	0.36	0.006	0.010	0.014		
М	0.125 typ.			0.005 typ.				
N: C15-1530-R	ev. B, 16-Nov-15							

Backside view of single pad



RECOMMENDED MINIMUM PADS FOR PowerPAK[®] 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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