

## Automotive N-Channel 40 V (D-S) 175 °C MOSFET

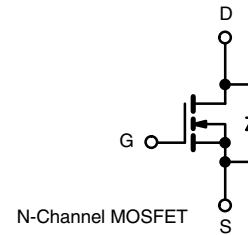
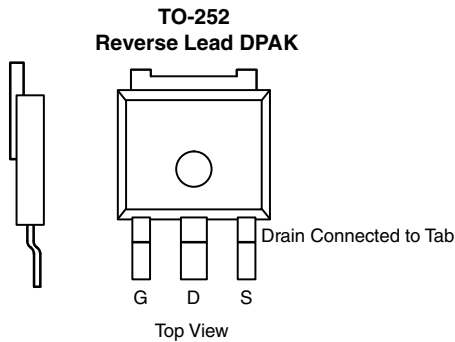


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	40
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.0038
I <sub>D</sub> (A)	50
Configuration	Single

### FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified<sup>d</sup>
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION	
Package	TO-252 Reverse Lead DPAK
Lead (Pb)-free and Halogen-free	SQR50N04-3m8-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	40	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current <sup>a</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	50
		T <sub>C</sub> = 125 °C	50
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	50	A
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	200	
Single Pulse Avalanche Current	I <sub>AS</sub>	62	
Single Pulse Avalanche Energy	E <sub>AS</sub>	192	mJ
Maximum Power Dissipation <sup>b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	
		T <sub>C</sub> = 125 °C	45
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R <sub>thJA</sub>	50	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	1.1	

### Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.



SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		40	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.5	3.0	3.5	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	50	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	-	0.0030	0.0038	$\Omega$
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0064	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0076	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		-	120	-	S
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	5360	6700	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	500	627	
Reverse Transfer Capacitance	$C_{rss}$			-	250	310	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 50\text{ A}$	-	70	105	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	16	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	13	-	
Gate Resistance	$R_g$	f = 1 MHz		0.9	1.9	2.9	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 0.4\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	11	16	ns
Rise Time <sup>c</sup>	$t_r$			-	5	8	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			-	34	51	
Fall Time <sup>c</sup>	$t_f$			-	9	14	
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>							
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	200	A
Forward Voltage	$V_{SD}$	$I_F = 30\text{ A}, V_{GS} = 0\text{ V}$		-	0.9	1.5	V

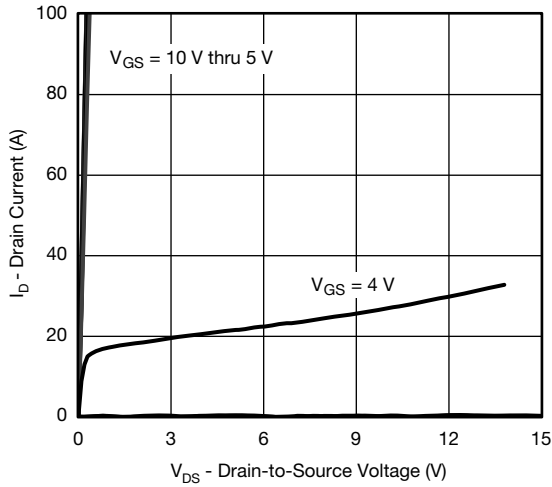
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

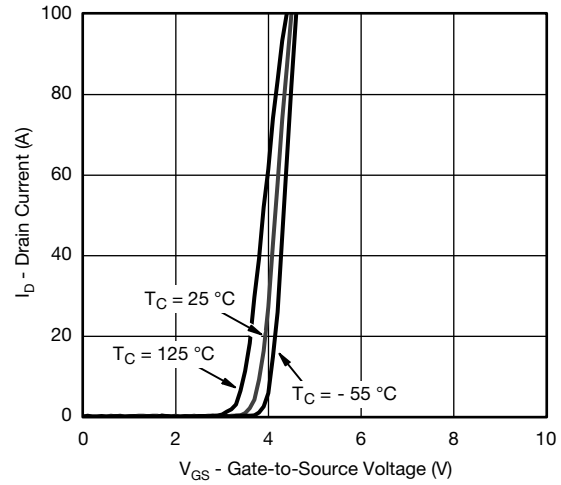
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



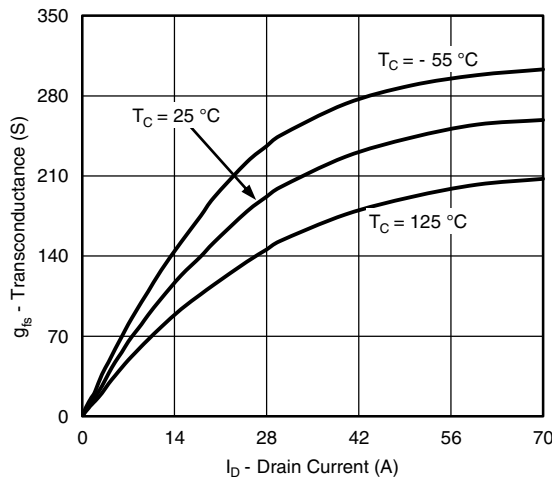
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



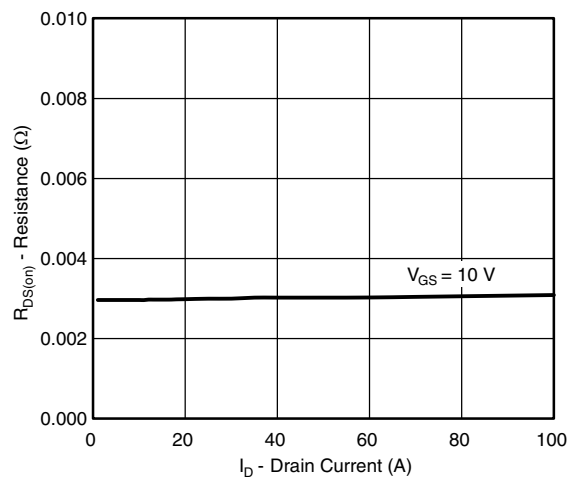
**Output Characteristics**



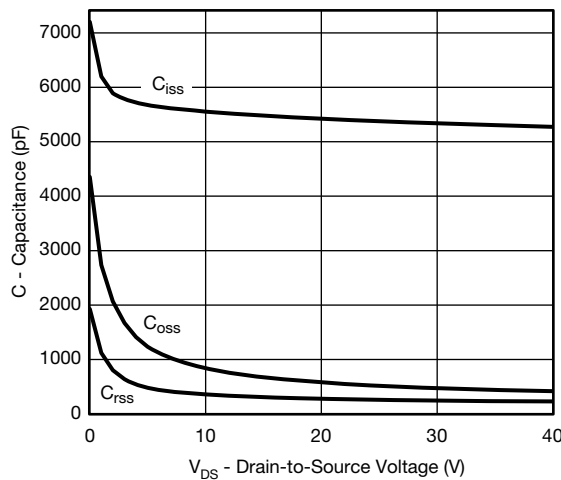
**Transfer Characteristics**



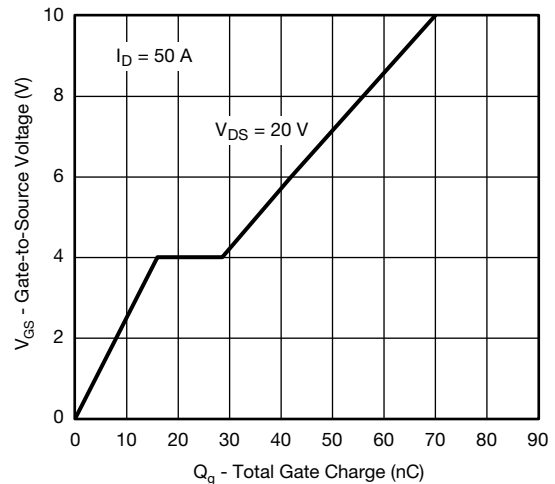
**Transconductance**



**On-Resistance vs. Drain Current**



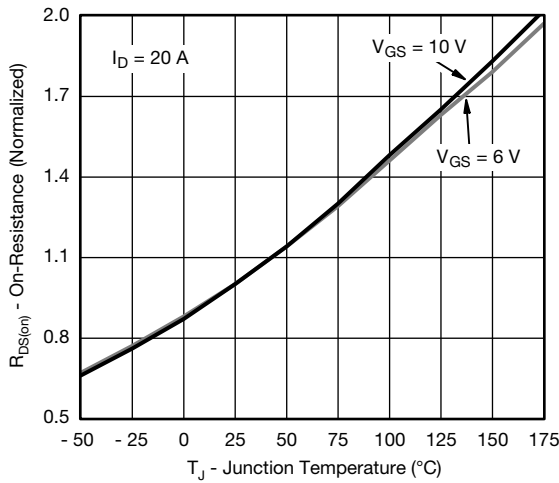
**Capacitance**



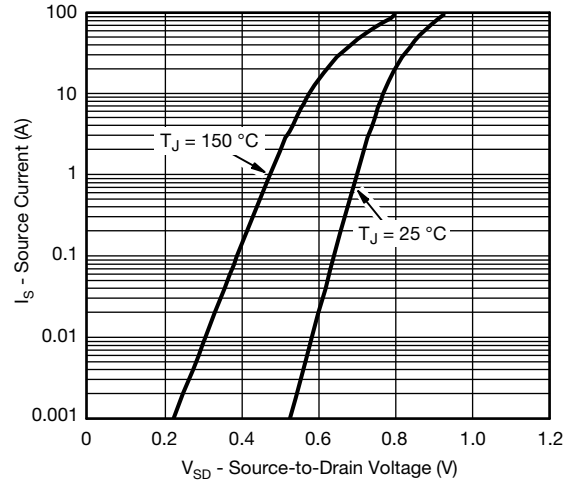
**Gate Charge**



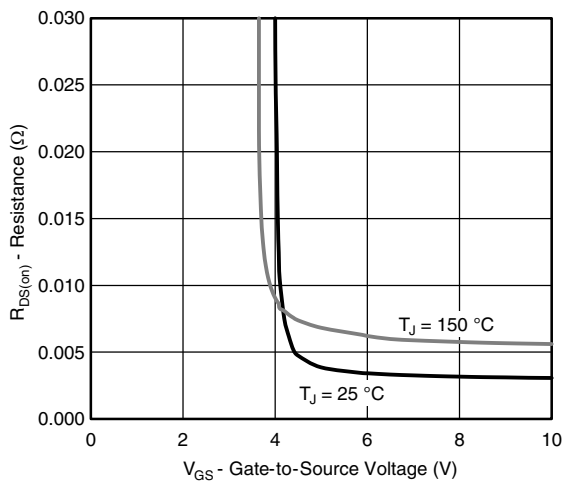
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



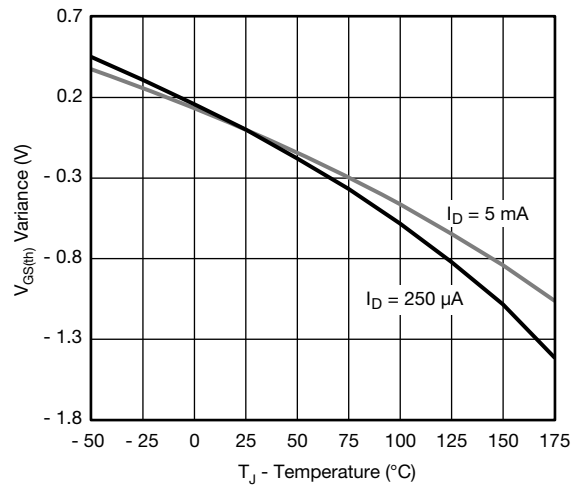
On-Resistance vs. Junction Temperature



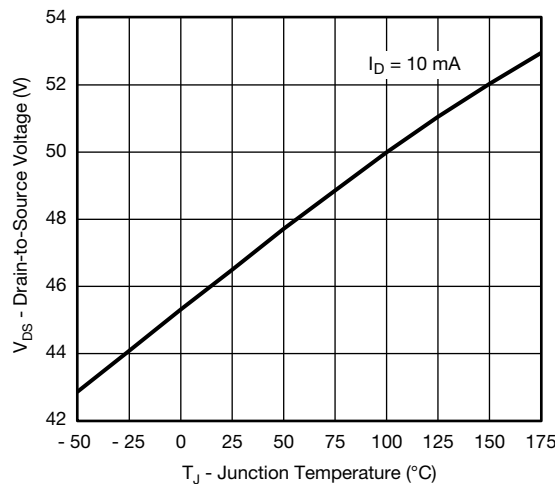
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



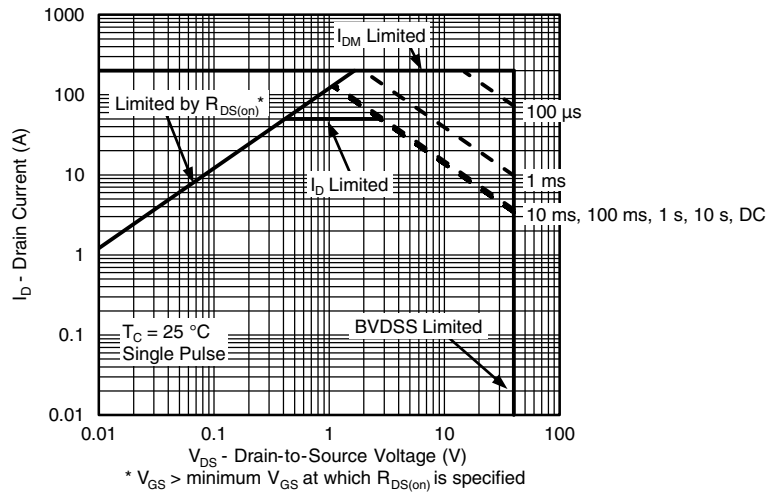
Threshold Voltage



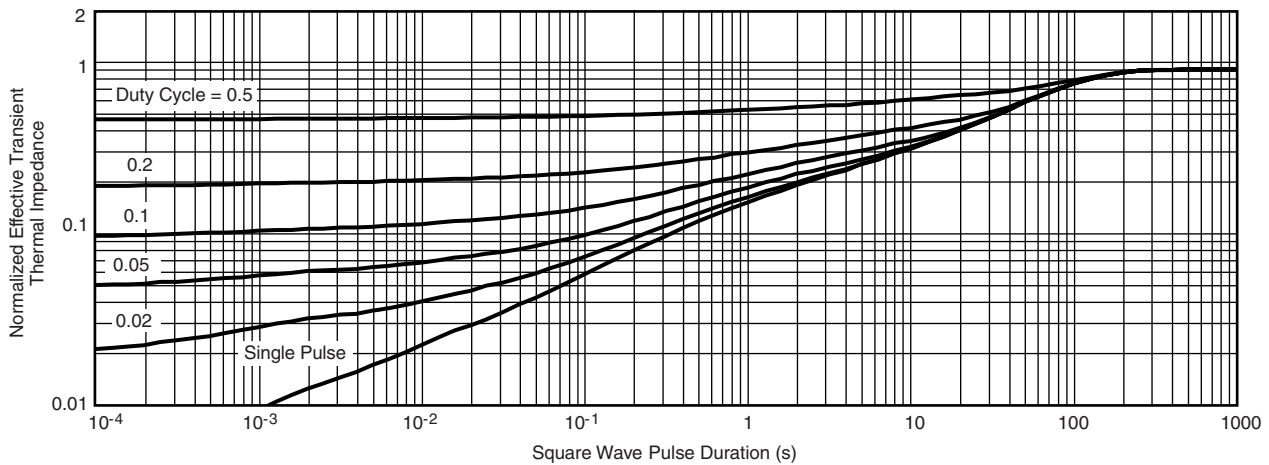
Drain Source Breakdown vs. Junction Temperature



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



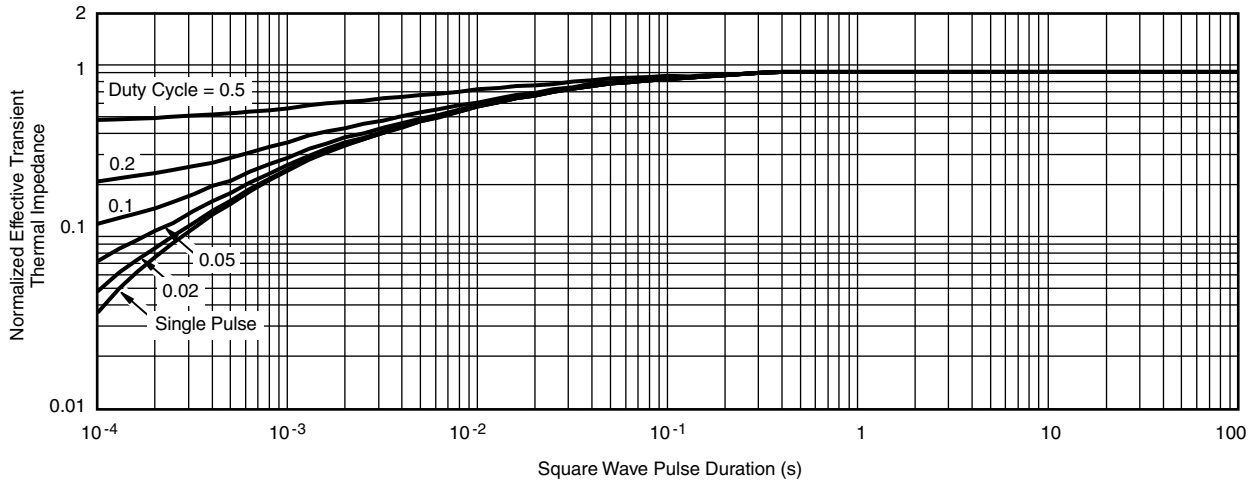
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



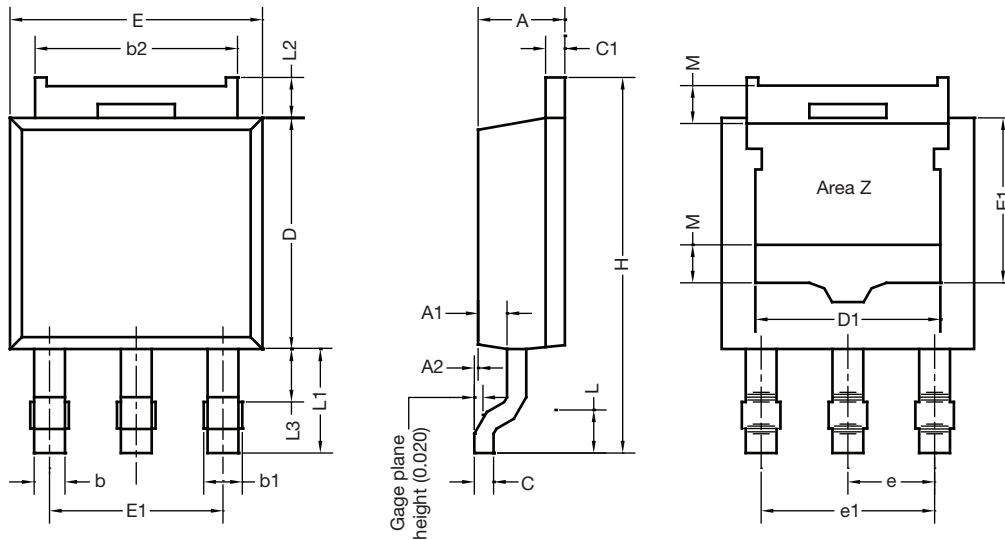
**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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## TO-252 Reverse Lead Case Outline



### Notes

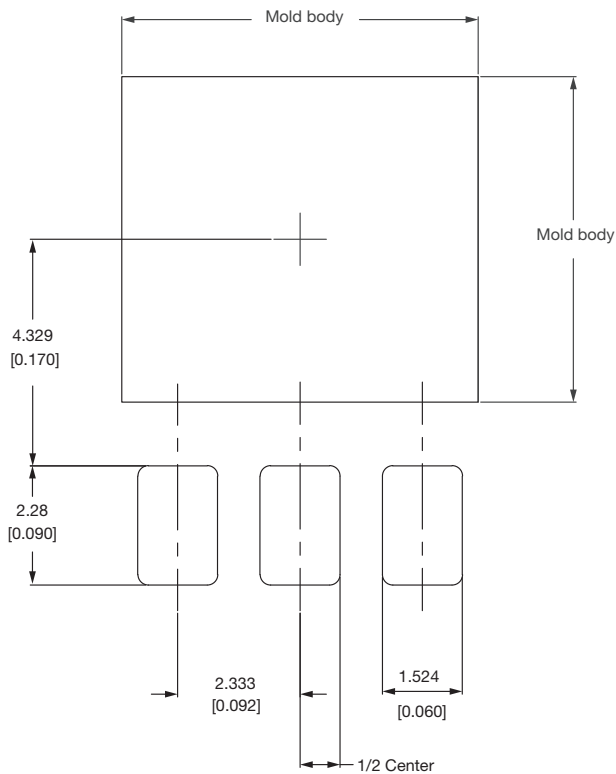
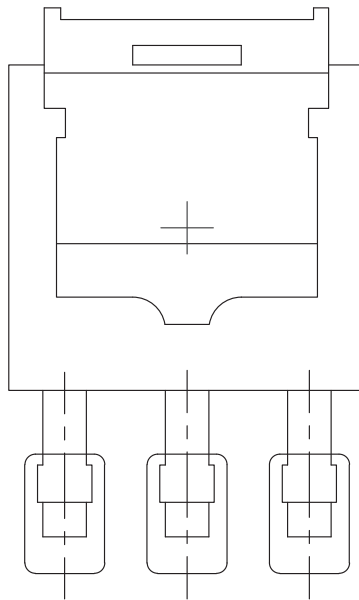
- Dimension L3 for reference only
- Area Z: unplated area more than 80 % heatsink area and for partial plating part only

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.23	2.33	0.088	0.092
A1	0.64	0.89	0.025	0.035
A2	0.03	0.18	0.001	0.007
b	0.71	0.88	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.44	0.206	0.214
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.49	5.00	0.177	0.197
E	6.48	6.73	0.255	0.265
E1	4.32	-	0.170	-
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.65	10.41	0.380	0.410
L	1.40	1.78	0.055	0.070
L1	2.74 BSC		0.108 BSC	
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.040	0.060
M	-	1.00 (reference only)	-	0.039 (reference only)

ECN: T16-0952-Rev. D, 16-Jan-17  
DWG: 5894



## Recommended Land Pattern DPAK (TO-252) 3LR



**Note**

- Dimensions in mm (inches)

ECN: T22-0575-Rev. A, 12-Dec-2022  
DWG: 3015





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