

Automotive P-Channel 40 V (D-S) 175 °C MOSFET

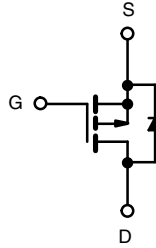
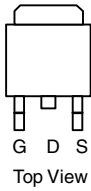


RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	- 40
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.0094
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.0170
I_D (A)	- 50
Configuration	Single

FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R_g and UIS Tested
- AEC-Q101 Qualified^d
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912

TO-263


P-Channel MOSFET

ORDERING INFORMATION

Package	TO-263
Lead (Pb)-free and Halogen-free	SQM50P04-09L-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	- 40	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ^a	I_D	$T_C = 25$ °C	- 50	
		$T_C = 125$ °C	- 50	
Continuous Source Current (Diode Conduction) ^a	I_S	- 50	A	
Pulsed Drain Current ^b	I_{DM}	- 200		
Single Pulse Avalanche Current	I_{AS}	- 50		
Single Pulse Avalanche Energy	E_{AS}	L = 0.1 mH	125	mJ
Maximum Power Dissipation ^b			P_D	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	$T_C = 25$ °C	50	W
		$T_C = 125$ °C	- 55 to + 175	
			- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)			

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.



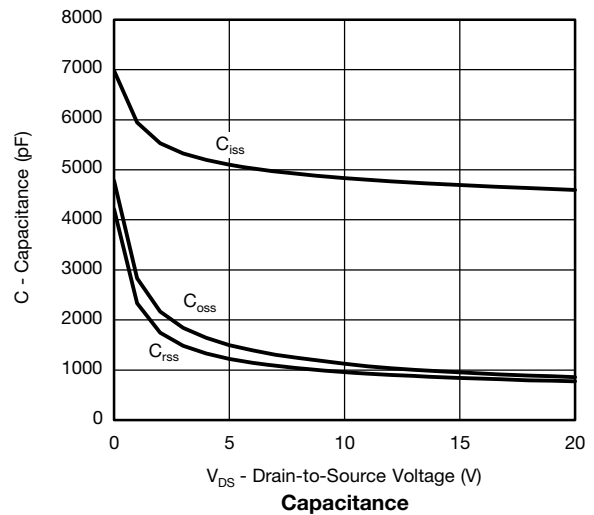
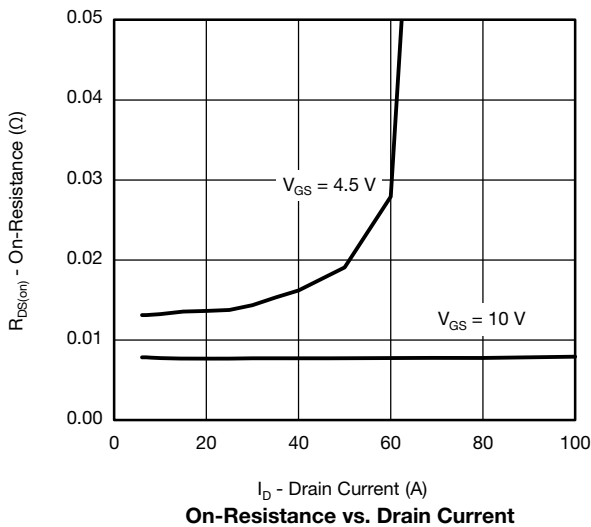
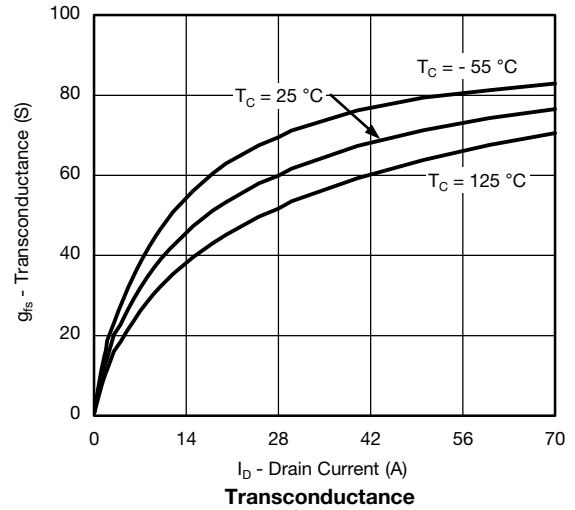
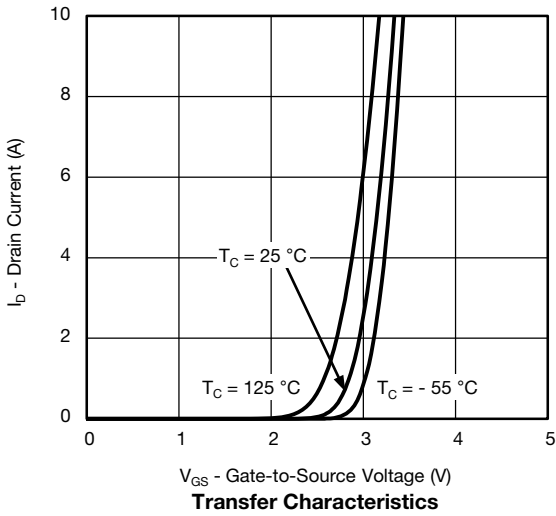
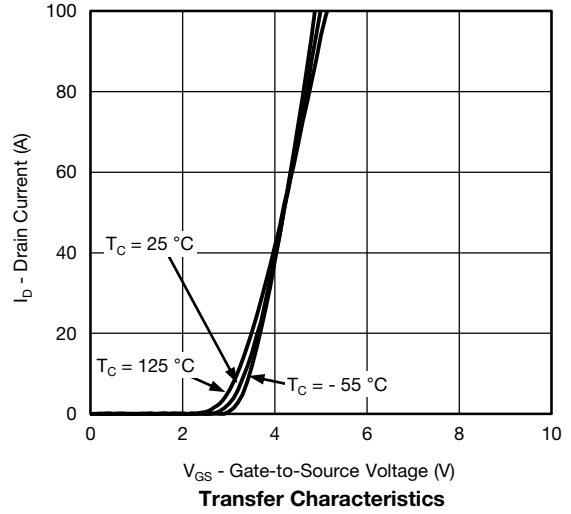
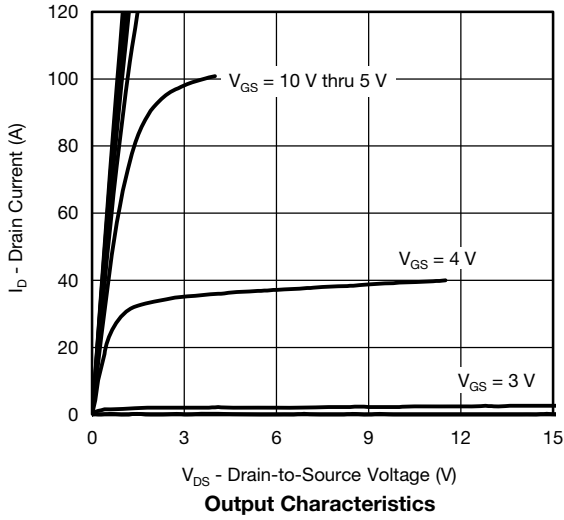
SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-40	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1.5	-2.0	-2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = -40\text{ V}$	-	-	-1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = -40\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	-50	
		$V_{GS} = 0\text{ V}$, $V_{DS} = -40\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	-250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = -10\text{ V}$, $V_{DS} \leq -5\text{ V}$	-100	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -50\text{ A}$	-	0.0078	0.0094	Ω
		$V_{GS} = -10\text{ V}$, $I_D = -50\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	0.0139	
		$V_{GS} = -10\text{ V}$, $I_D = -50\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	0.0162	
		$V_{GS} = -4.5\text{ V}$, $I_D = -25\text{ A}$	-	0.0138	0.0170	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -50\text{ A}$	-	70	-	S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = -10\text{ V}$, $f = 1\text{ MHz}$	-	4836	6045	μF
Output Capacitance	C_{oss}		-	1129	1415	
Reverse Transfer Capacitance	C_{rss}		-	959	1200	
Total Gate Charge ^c	Q_g	$V_{GS} = -10\text{ V}$, $V_{DS} = -20\text{ V}$, $I_D = -50\text{ A}$	-	96.5	145	nC
Gate-Source Charge ^c	Q_{gs}		-	21.4	-	
Gate-Drain Charge ^c	Q_{gd}		-	16.6	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.2	2.56	3.9	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -20\text{ V}$, $R_L = 0.4\text{ }\Omega$ $I_D \cong -50\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	-	12	18	ns
Rise Time ^c	t_r		-	13	20	
Turn-Off Delay Time ^c	$t_{d(off)}$		-	61	91	
Fall Time ^c	t_f		-	18	27	
Source-Drain Diode Ratings and Characteristics^b						
Pulsed Current ^a	I_{SM}		-	-	-200	A
Forward Voltage	V_{SD}	$I_F = -40\text{ A}$, $V_{GS} = 0\text{ V}$	-	-0.95	-1.5	V

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

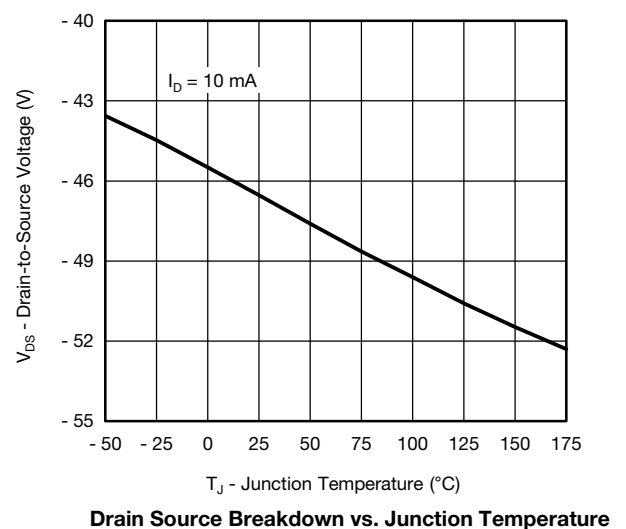
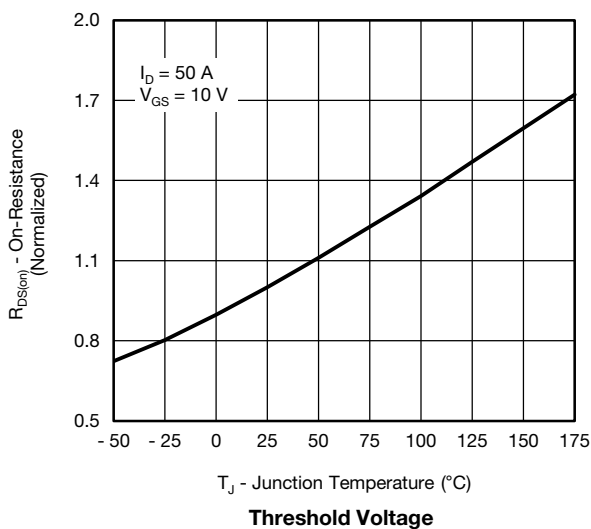
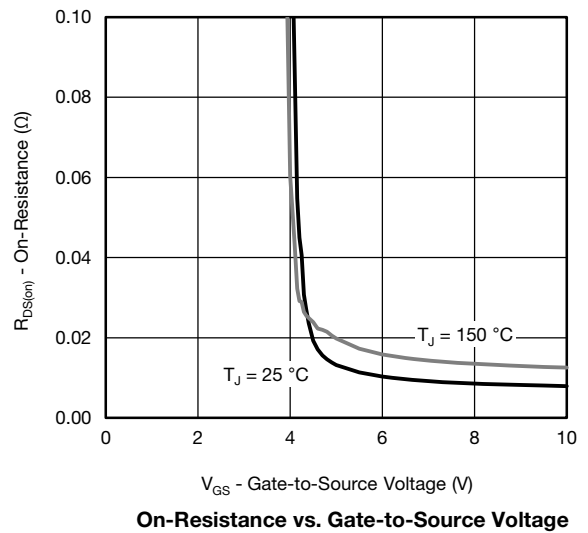
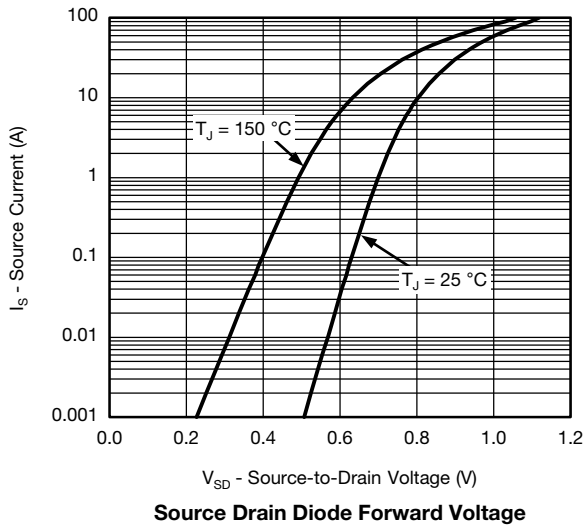
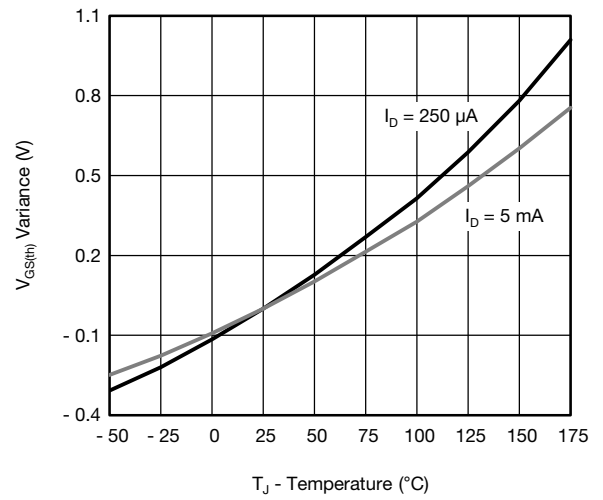
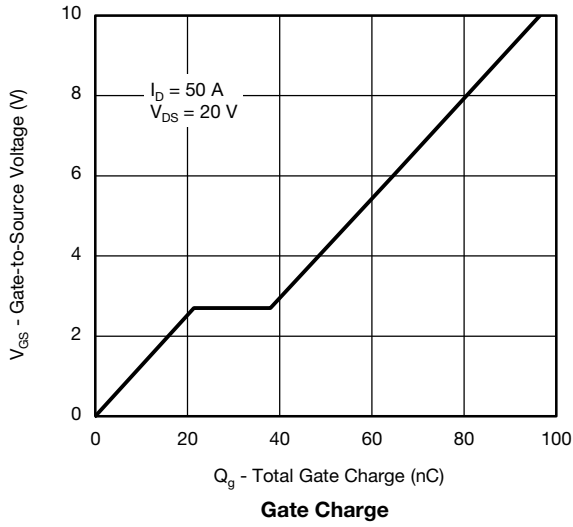
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



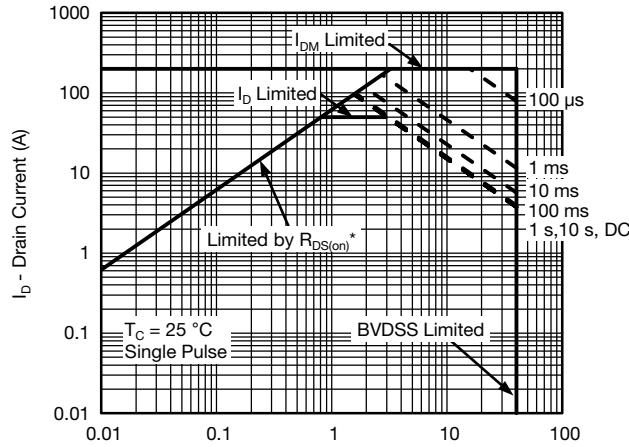


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



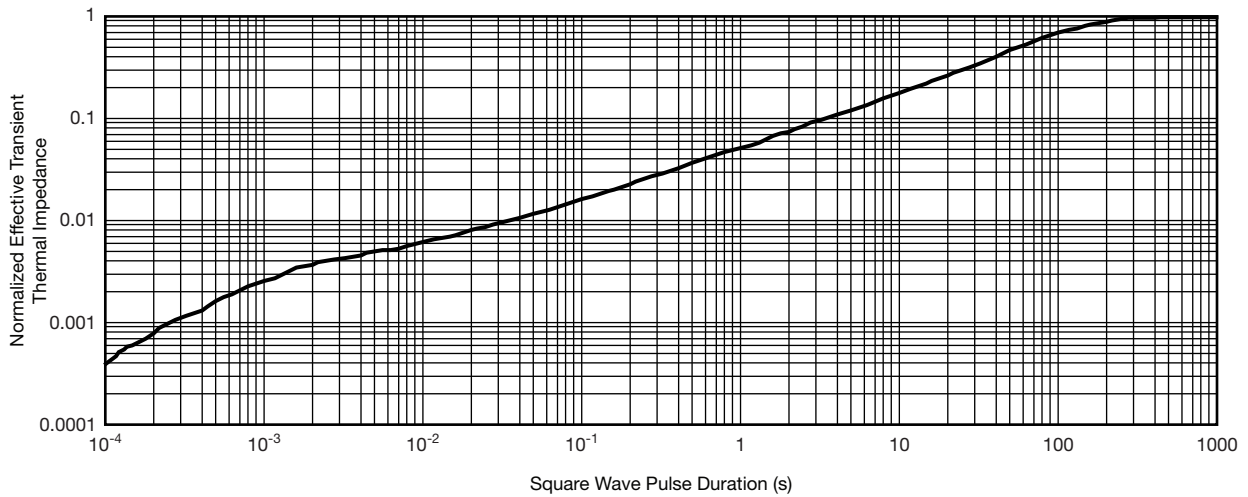


THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

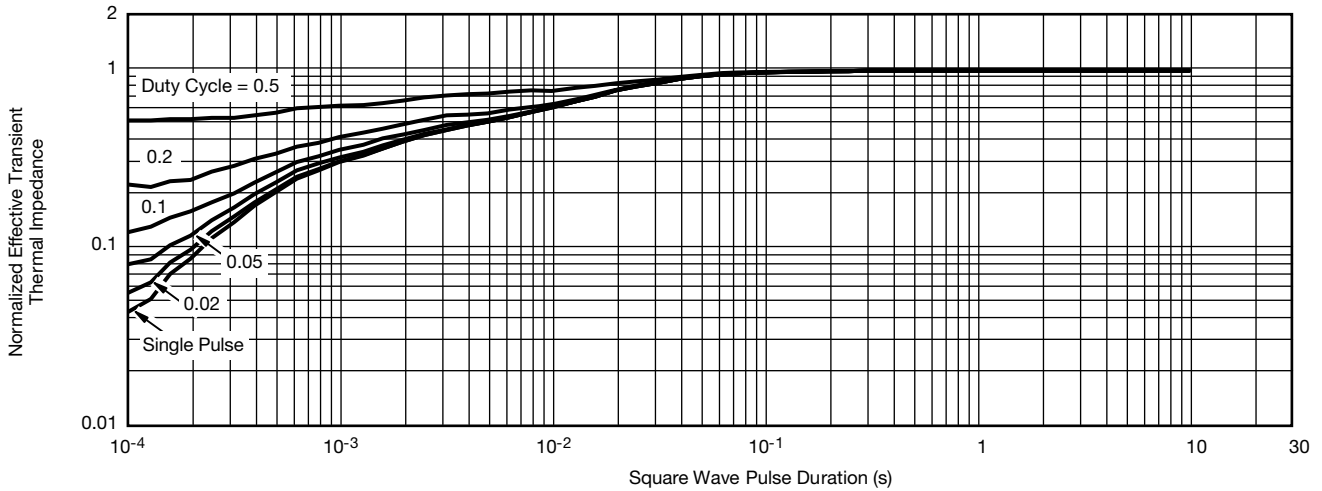
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



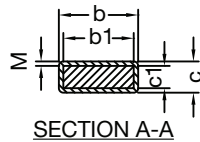
Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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TO-263 (D²PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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