

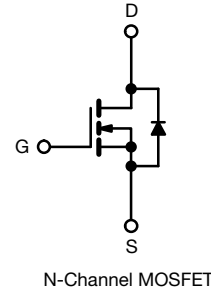
Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE


RoHS
 COMPLIANT
 HALOGEN
FREE


N-Channel MOSFET

PRODUCT SUMMARY

V _{DS} (V)	60
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0020
I _D (A)	362
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ160EP (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	60	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	I _D	T _C = 25 °C	362
		T _C = 125 °C	209
Continuous source current (diode conduction)	I _S	400	A
Pulsed drain current ^a	I _{DM}	426	
Single pulse avalanche current	I _{AS}	50	
Single pulse avalanche energy	E _{AS}	125	mJ
Maximum power dissipation	P _D	T _C = 25 °C	500
		T _C = 125 °C	166
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R _{thJA}	42	°C/W
Junction-to-case (drain)	R _{thJC}	0.3	

Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.2	2.8	3.5	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	250	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$ $V_{DS} \geq 5\text{ V}$	30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}$	-	0.0014	0.0020	Ω
		$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0032	
		$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0040	
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	-	150	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	4873	6697	μF
Output capacitance	C_{oss}		-	1955	2727	
Reverse transfer capacitance	C_{rss}		-	140	196	
Total gate charge ^c	Q_g	$V_{GS} = 10\text{ V}$ $V_{DS} = 30\text{ V}, I_D = 10\text{ A}$	-	79	119	nC
Gate-source charge ^c	Q_{gs}		-	24	-	
Gate-drain charge ^c	Q_{gd}		-	18	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.4	0.9	1.4	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 3.0\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	19	29	ns
Rise time ^c	t_r		-	12	18	
Turn-off delay time ^c	$t_{d(off)}$		-	33	50	
Fall time ^c	t_f		-	10	15	
Source-Drain Diode Ratings and Characteristics ^b						
Pulsed current ^a	I_{SM}		-	-	426	A
Forward voltage	V_{SD}	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	56	112	ns
Body diode reverse recovery charge	Q_{rr}		-	56	112	nC
Reverse recovery fall time	t_a		-	25	-	ns
Reverse recovery rise time	t_b		-	33	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	1.7	-

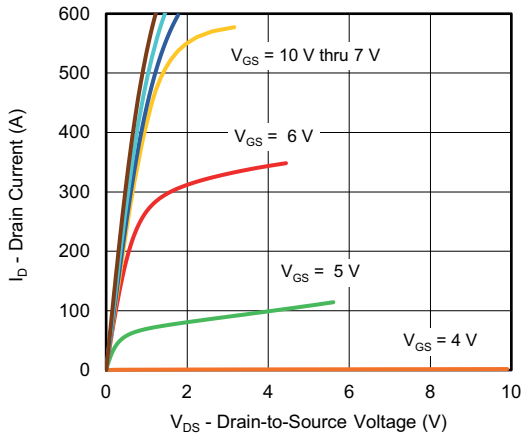
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

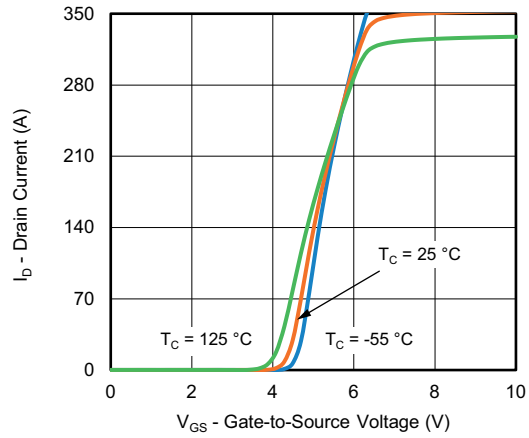
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



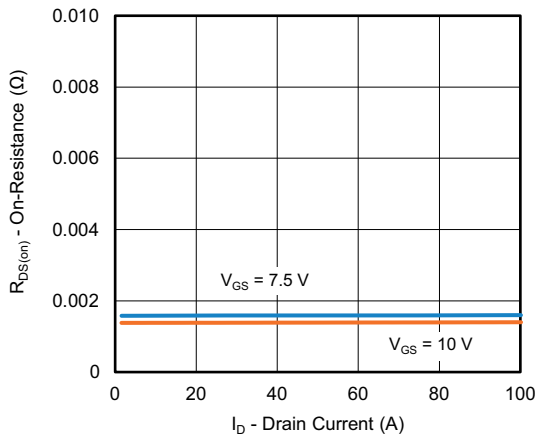
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



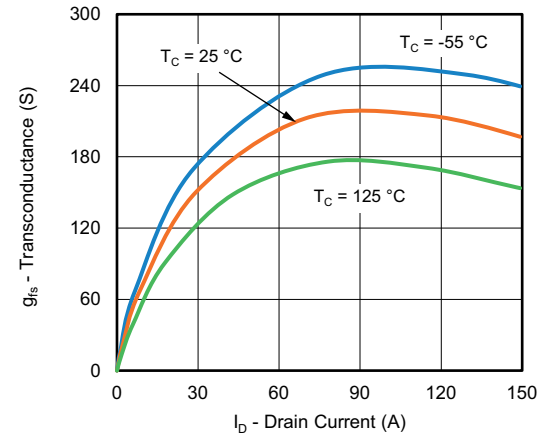
Output Characteristics



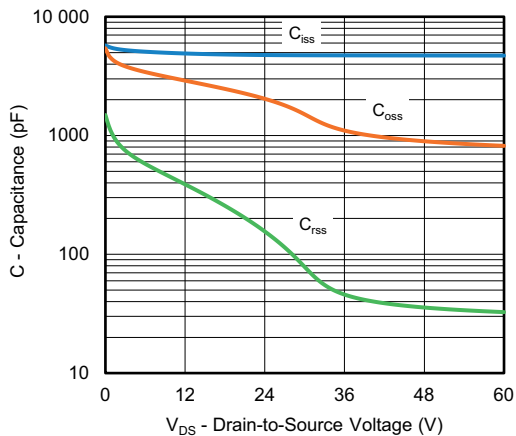
Transfer Characteristics



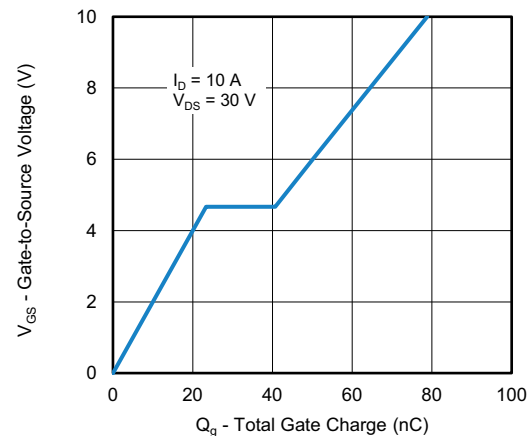
On-Resistance vs. Drain Current



Transconductance



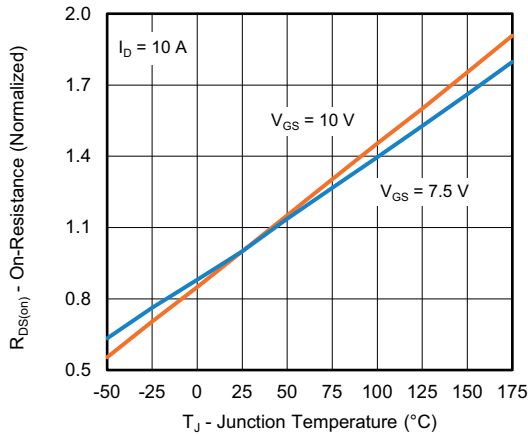
Capacitance



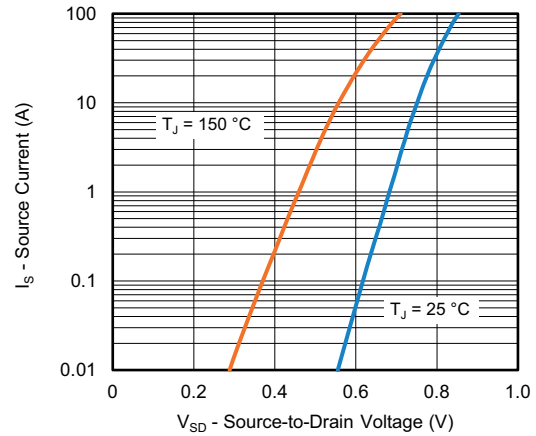
Gate Charge



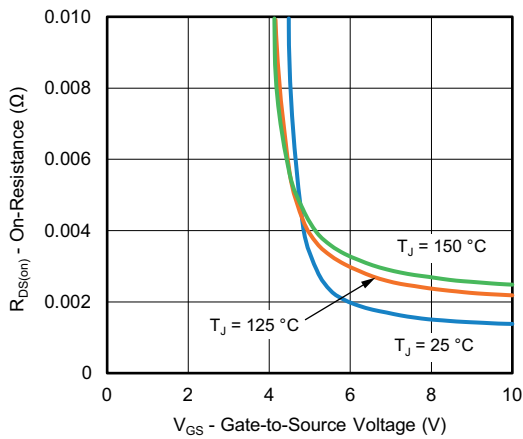
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



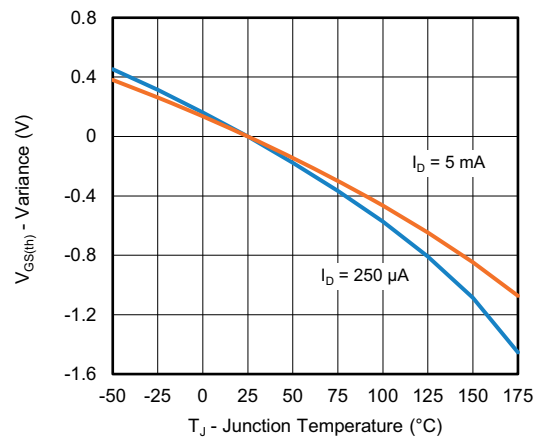
On-Resistance vs. Junction Temperature



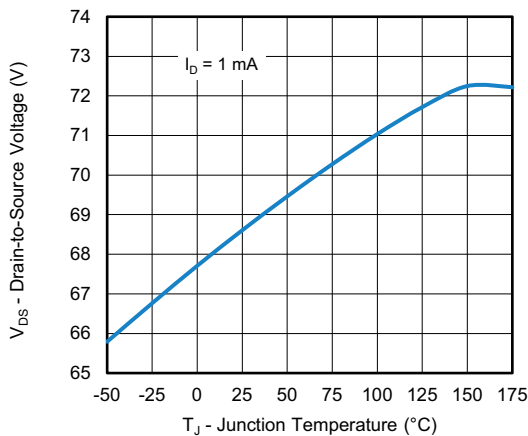
Source Drain Diode Forward Voltage



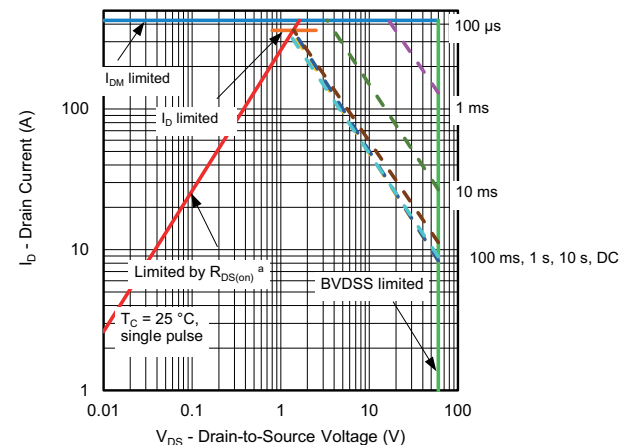
On-Resistance vs. Gate-to Source Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



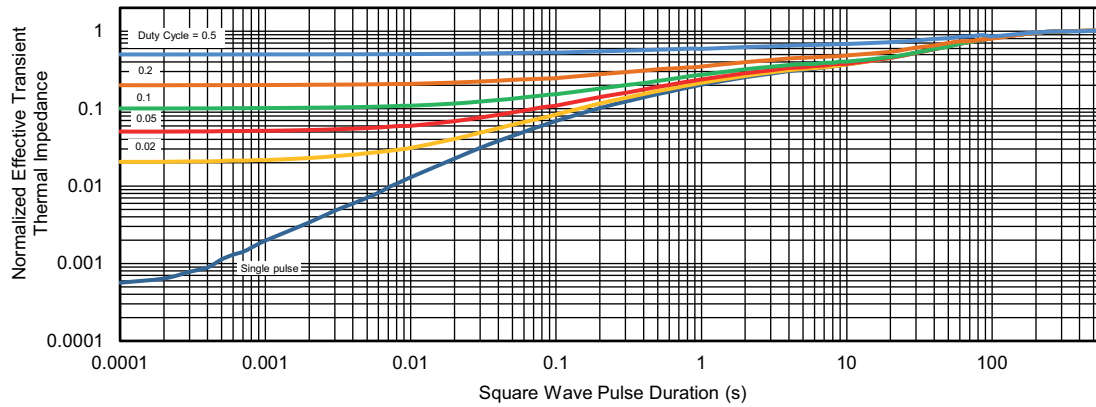
Safe Operating Area

Note

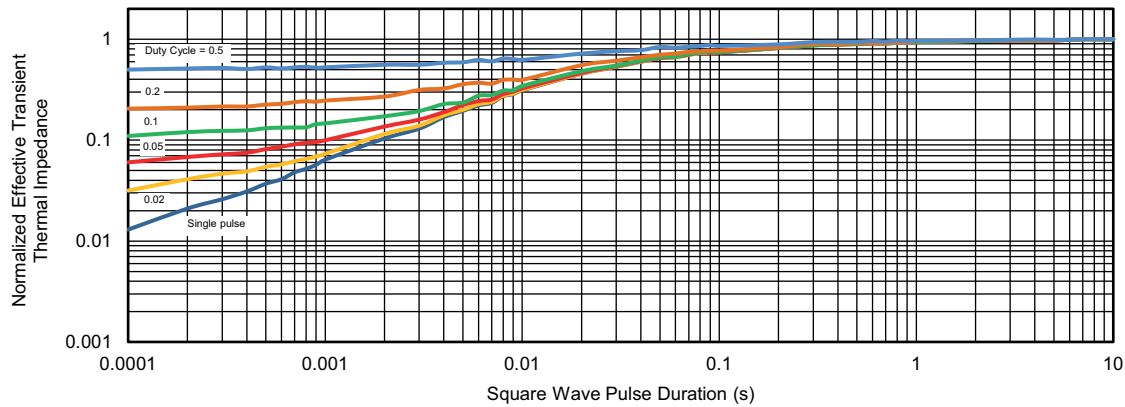
- a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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PowerPAK® SO-8L (PPKS08LWLA) Case Outline 3



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.05	1.10	0.039	0.041	0.043
A1	0.00	---	0.127	0.000	---	0.005
b	0.33	0.41	0.49	0.013	0.016	0.019
b1	0.43	0.51	0.59	0.017	0.020	0.023
b2	4.00	4.10	4.20	0.157	0.161	0.165
c	0.15	0.20	0.25	0.006	0.008	0.010
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D5	0.51	0.61	0.71	0.020	0.024	0.028
D6	2.64	2.74	2.84	0.104	0.108	0.112
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
E3	3.48	3.58	3.68	0.137	0.141	0.145
E4	2.72	2.82	2.92	0.107	0.111	0.115
E5	0.71	0.81	0.91	0.028	0.032	0.036
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
W1	0.31	0.41	0.51	0.012	0.016	0.020
W4	0.31	0.36	0.41	0.012	0.014	0.016
z1	0.37	0.47	0.57	0.015	0.019	0.022
z2	0.99	1.09	1.19	0.039	0.043	0.047
θ	0°	---	5°	0°	---	5°

ECN: C23-1016-Rev. D, 18-Sep-2023
DWG: 6067

Note

- Millimeter will govern



Recommended Land Pattern PowerPAK® SO-8L Single Short Ear



Dimensions in Millimeters (Inches)



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