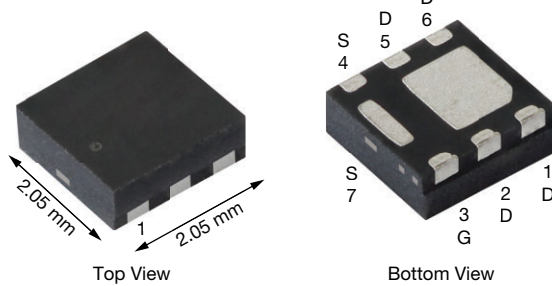


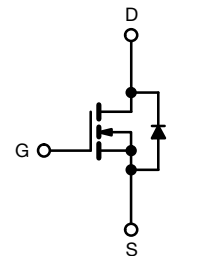
Automotive N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® SC-70W-6L Single

Marking Code: Q4XXXX

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


N-Channel MOSFET

PRODUCT SUMMARY

V _{DS} (V)	80
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0800
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.0950
I _D (A)	5.63
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA604CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	80	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	I _D	T _C = 25 °C ^a	5.63
		T _C = 125 °C	5.13
Continuous source current (diode conduction) ^a	I _S	5.63	A
Pulsed drain current ^a	I _{DM}	21	
Single pulse avalanche current	I _{AS}	9	
Single pulse avalanche energy	E _{AS}	4.05	mJ
Maximum power dissipation	P _D	T _C = 25 °C	13.6
		T _C = 125 °C	4.5
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R _{thJA}	90	°C/W
Junction-to-case (drain)	R _{thJC}	11	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		80	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.5	2	2.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 80 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	5	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 3 A	-	0.0593	0.0800	Ω
		V _{GS} = 10 V	I _D = 3 A, T _J = 125 °C	-	-	0.1405	
		V _{GS} = 10 V	I _D = 3 A, T _J = 175 °C	-	-	0.1724	
		V _{GS} = 4.5 V	I _D = 2.5 A	-	0.0690	0.0950	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3 A		-	10.2	-	S
Dynamic ^b							
Input capacitance	C _{ISS}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	315	445	pF
Output capacitance	C _{OSS}			-	63	90	
Reverse transfer capacitance	C _{RSS}			-	9	13	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 40 V, I _D = 5 A	-	6.5	9.8	nC
Gate-source charge ^c	Q _{gs}			-	1.3	-	
Gate-drain charge ^c	Q _{gd}			-	1.2	-	
Gate resistance	R _g	f = 1 MHz		0.62	1.24	1.86	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 40 V, R _L = 40 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 1 Ω		-	5	10	ns
Rise time ^c	t _r			-	3	6	
Turn-off delay time ^c	t _{d(off)}			-	14	22	
Fall time ^c	t _f			-	5	10	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	21	A
Forward voltage	V _{SD}	I _F = 3 A, V _{GS} = 0 V		-	0.85	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 1 A, di/dt = 100 A/μs		-	17	34	ns
Body diode reverse recovery charge	Q _{rr}			-	10.2	20.5	nC
Reverse recovery fall time	t _a			-	12	-	ns
Reverse recovery rise time	t _b			-	5	-	
Body diode peak reverse recovery current	I _{RM(REC)}					-	-1.03

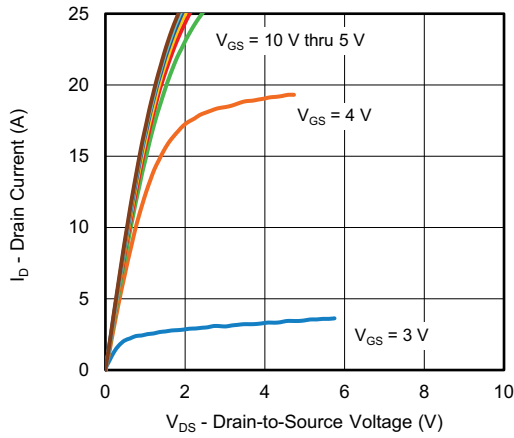
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

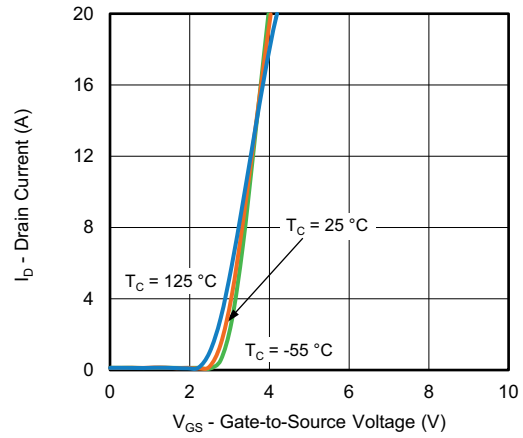
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



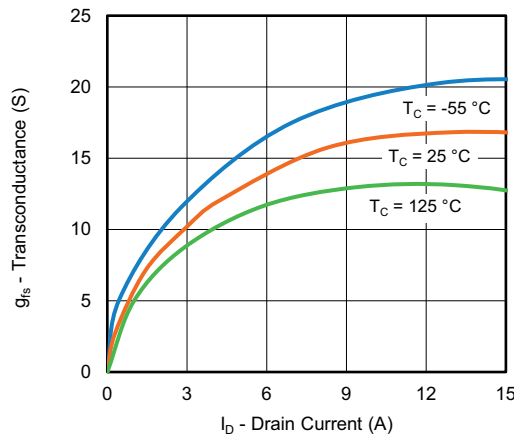
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



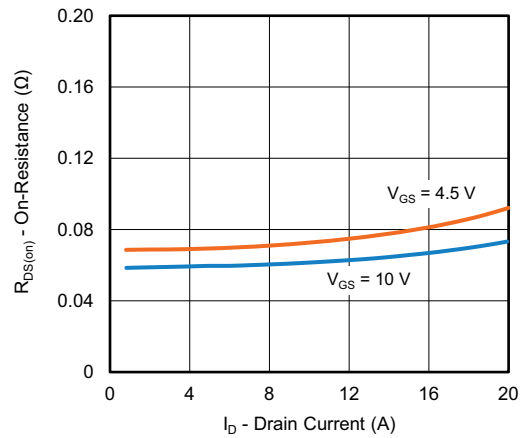
Output Characteristics



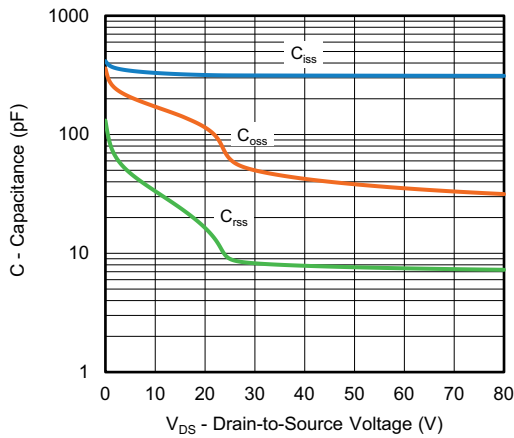
Transfer Characteristics



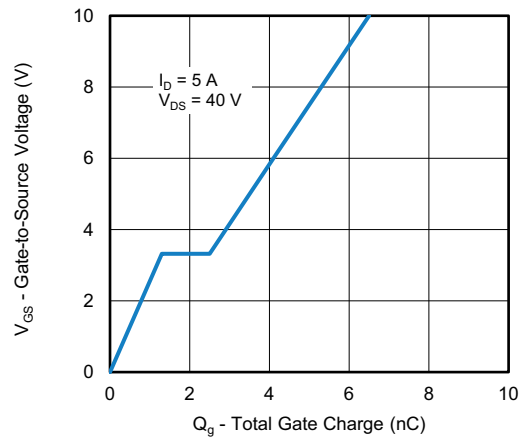
Transconductance



On-Resistance vs. Drain Current



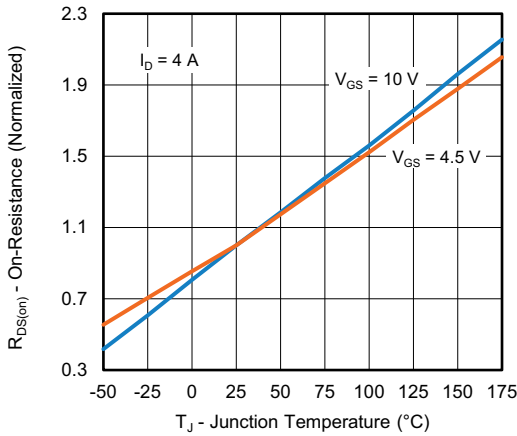
Capacitance



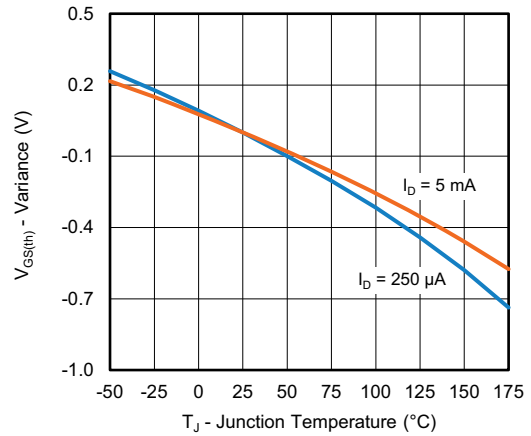
Gate Charge



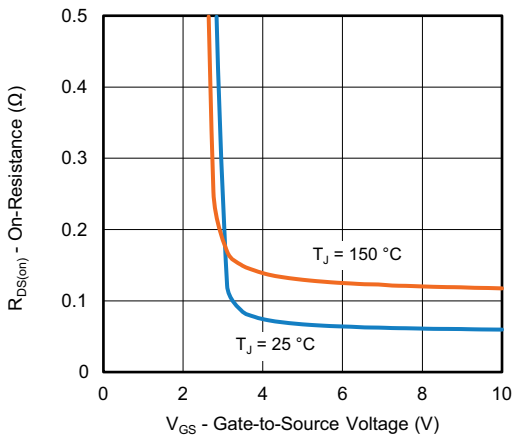
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



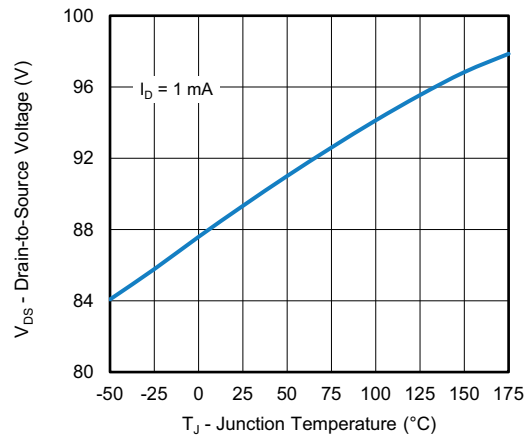
On-Resistance vs. Junction Temperature



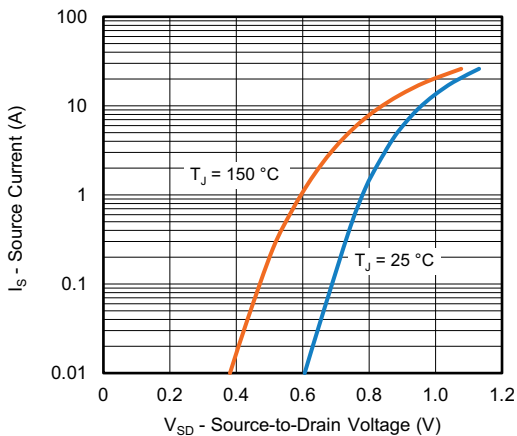
Threshold Voltage



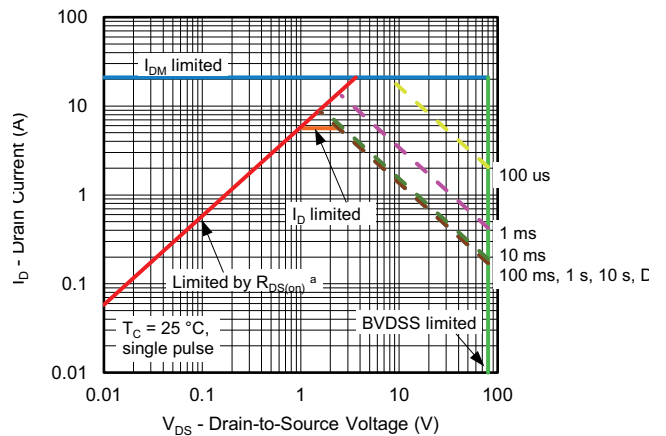
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage



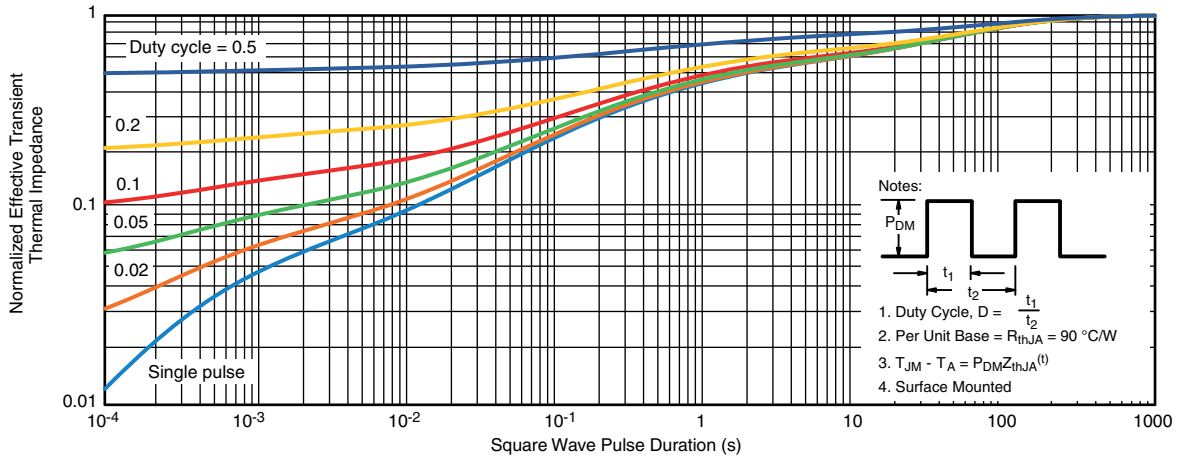
Safe Operating Area

Note

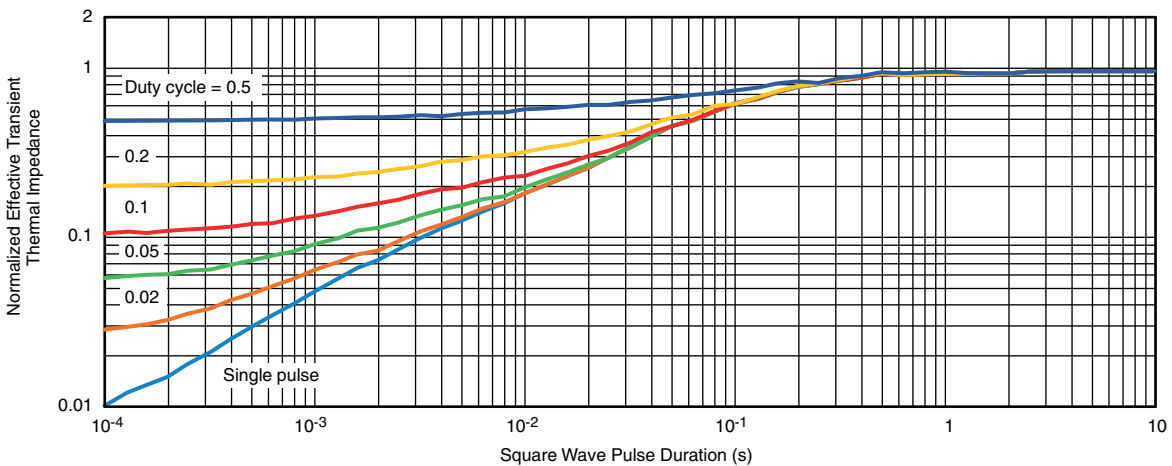
- a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



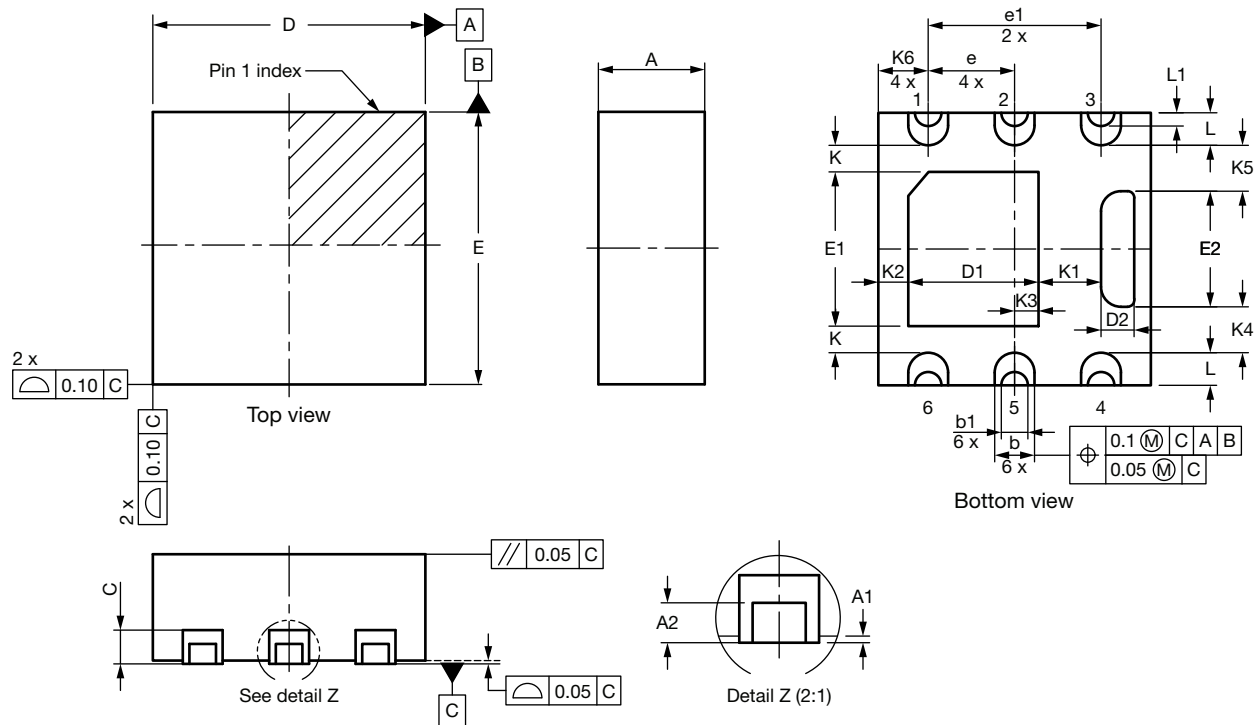
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62007.

PowerPAK® SC70W-6L SIDEWETTABLE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.10	-	-	0.004	-	-
b	0.25	0.30	0.35	0.010	0.012	0.014
b1	0.15	0.20	0.23	0.006	0.008	0.009
C	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.05	2.15	0.077	0.081	0.085
D1	0.88	0.98	1.08	0.035	0.039	0.043
D2	0.20	0.25	0.30	0.008	0.010	0.012
E	1.95	2.05	2.15	0.077	0.081	0.085
E1	1.06	1.16	1.26	0.042	0.046	0.050
E2	0.82	0.87	0.92	0.032	0.034	0.036
e	0.65 BSC			0.026 BSC		
e1	1.30 BSC			0.051 BSC		
K	0.20 typ.			0.008 typ.		
K1	0.47 typ.			0.019 typ.		
K2	0.23 typ.			0.009 typ.		
K3	0.18 typ.			0.007 typ.		
K4	0.35 typ.			0.014 typ.		
K5	0.35 typ.			0.014 typ.		
K6	0.38 typ.			0.015 typ.		
L	0.15	0.25	0.35	0.006	0.010	0.014
L1	-	0.10	-	-	0.004	-

ECN: C19-1644-Rev. A, 10-Jan-2020
DWG: 6076

Notes

- Package outline exclusive of mold flash and metal burr
- Package outline inclusive of plating



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