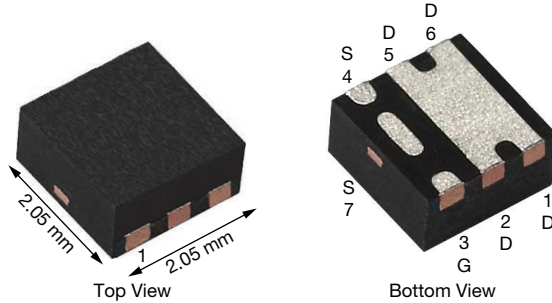


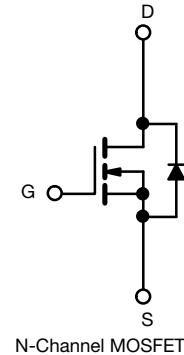
Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® SC-70-6L Single

Marking Code: QDXXXX

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified ^d
- 100 % R_G and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE


RoHS
 COMPLIANT
 HALOGEN
FREE


PRODUCT SUMMARY	
V _{DS} (V)	60
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.032
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.048
I _D (A)	9
Configuration	Single
Package	PowerPAK SC-70

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	60	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current ^a	I _D	T _C = 25 °C	9
		T _C = 125 °C	8.3
Continuous source current (diode conduction) ^a	I _S	9	A
Pulsed drain current ^a	I _{DM}	24.5	
Single pulse avalanche current	I _{AS}	13	
Single pulse avalanche energy	E _{AS}	8.4	mJ
Maximum power dissipation ^b	P _D	T _C = 25 °C	13.6
		T _C = 125 °C	4.5
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R _{thJA}	90	°C/W
Junction-to-case (drain)	R _{thJC}	11	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- Parametric verification ongoing
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		60	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		1.5	2	2.5	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	250	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = 4.5\text{ V}$	$V_{DS} \geq 5\text{ V}$	10	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$	-	0.026	0.032	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	0.058	
		$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	0.065	
		$V_{GS} = 4.5\text{ V}$	$I_D = 3\text{ A}$	-	0.045	0.048	
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 6\text{ A}$		-	21	-	S
Dynamic ^b							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$	-	509	636	pF
Output capacitance	C_{oss}			-	242	302	
Reverse transfer capacitance	C_{rss}			-	14.6	18.3	
Total gate charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 30\text{ V}$, $I_D = 5\text{ A}$	-	7.75	9.7	nC
Gate-source charge ^c	Q_{gs}			-	1.53	-	
Gate-drain charge ^c	Q_{gd}			-	1.2	-	
Gate resistance	R_g	$f = 1\text{ MHz}$		0.24	0.41	0.65	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $R_L = 6\text{ }\Omega$ $I_D \cong 5\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ k}\Omega$		-	7.3	9.1	ns
Rise time ^c	t_r			-	2	2.5	
Turn-off delay time ^c	$t_{d(off)}$			-	12	15.5	
Fall time ^c	t_f			-	1.4	1.8	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I_{SM}			-	-	24	A
Forward voltage	V_{SD}	$I_F = 4.5\text{ A}$, $V_{GS} = 0\text{ V}$		-	0.75	1.2	V

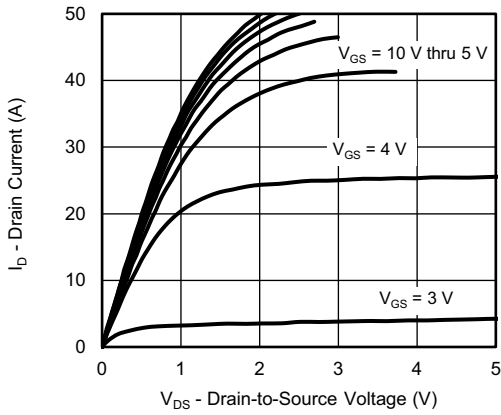
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

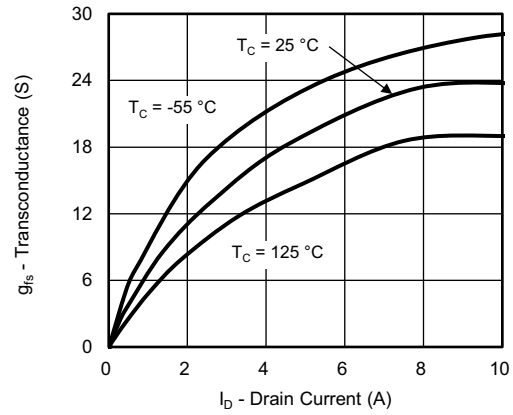
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



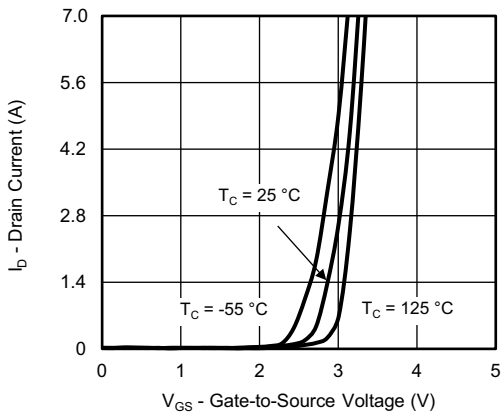
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



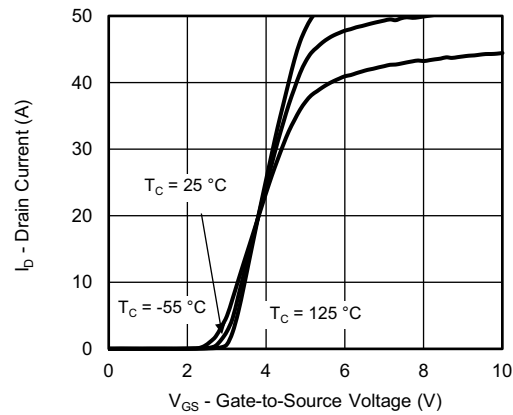
Output Characteristics



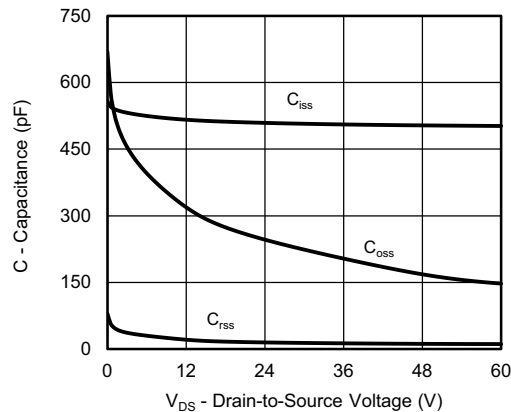
Transconductance



Transfer Characteristics

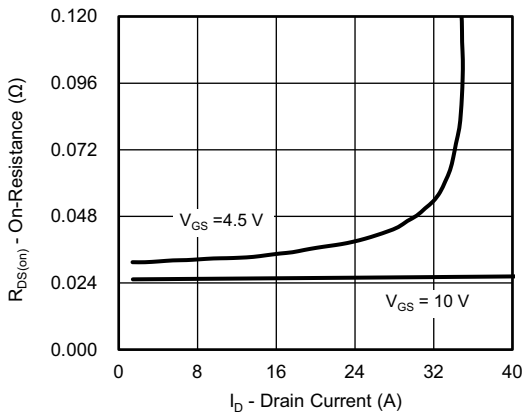


Transfer Characteristics

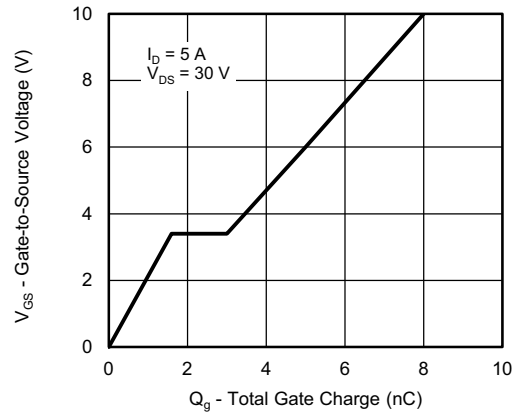


Capacitance

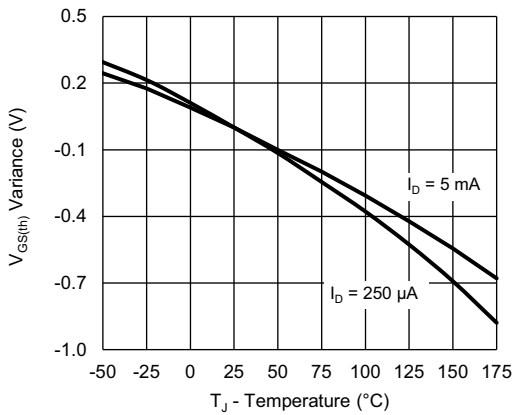
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



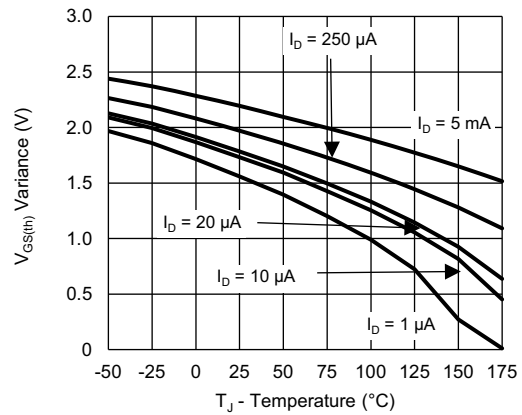
On-Resistance vs. Drain Current



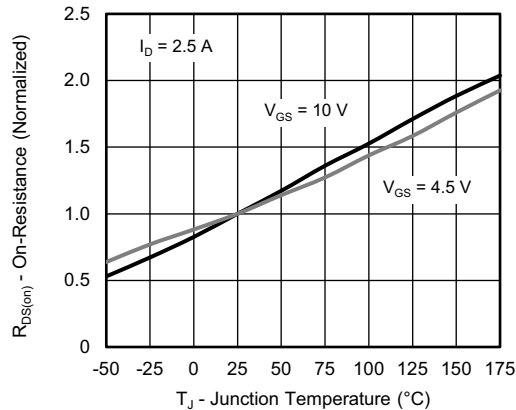
Gate Charge



Threshold Voltage

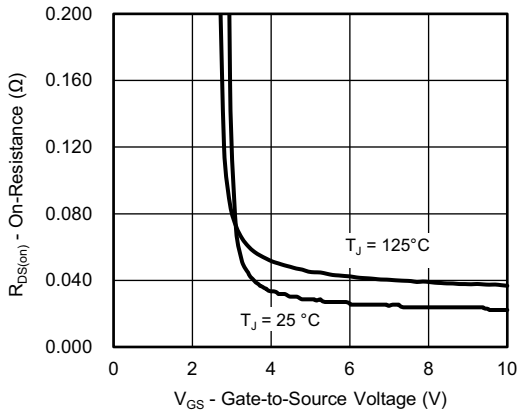


Threshold Voltage

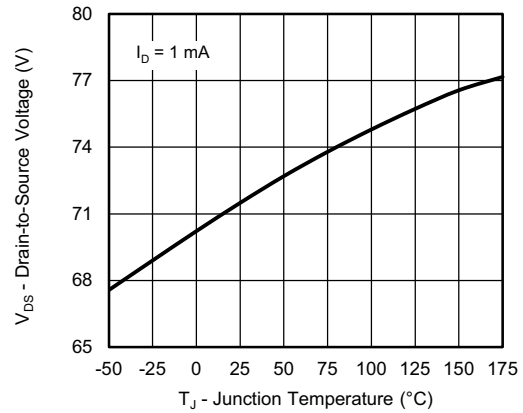


On-Resistance vs. Junction Temperature

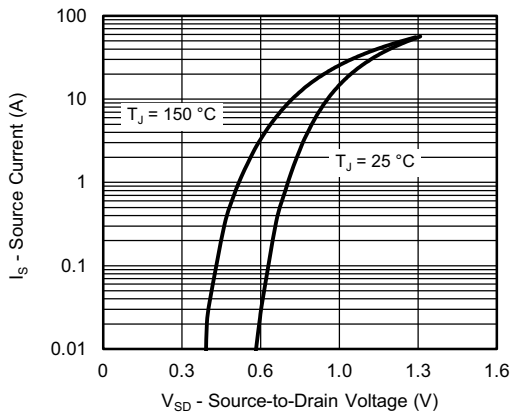
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



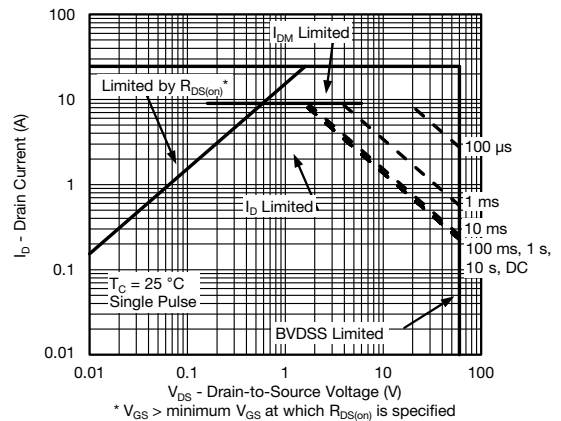
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature

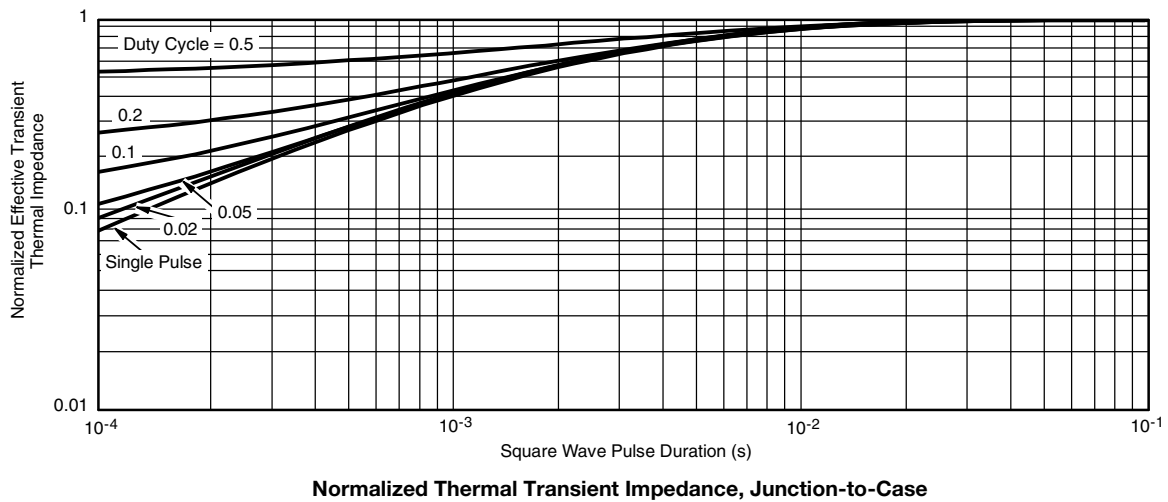
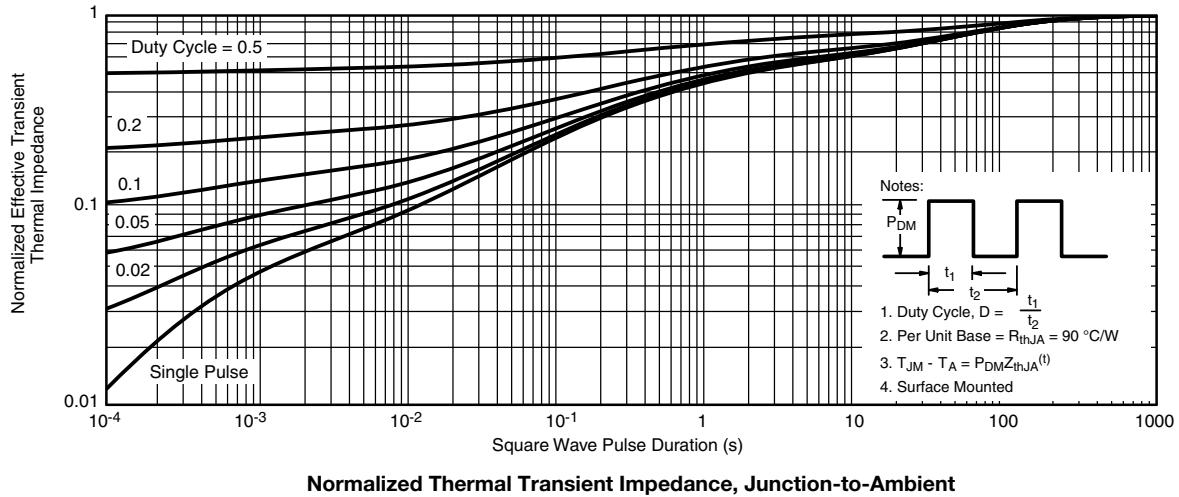


Source Drain Diode Forward Voltage



Safe Operating Area

THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

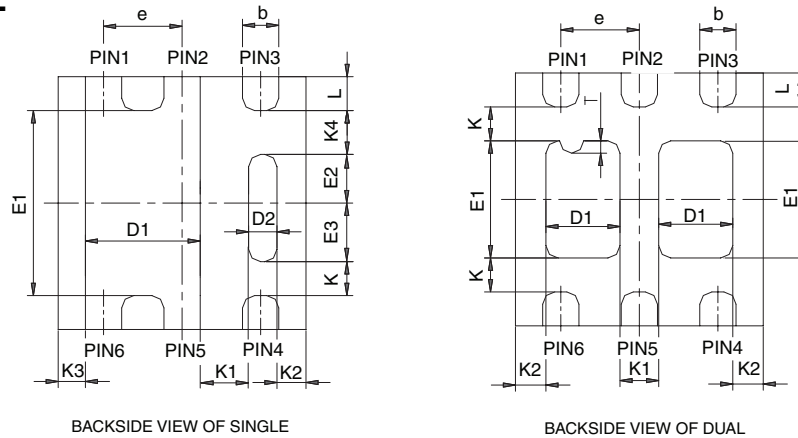


Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

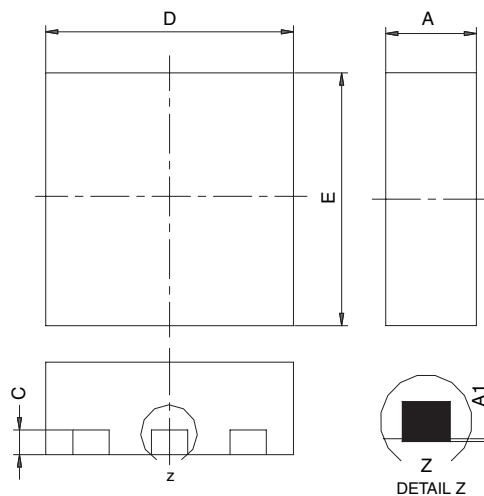
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PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07
 DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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