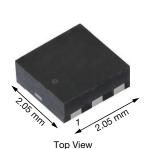
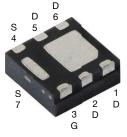
www.vishay.com

Vishay Siliconix

Automotive P-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® SC-70W-6L Single





Single

Bottom View

Marking Code: Q8XXXX

Configuration

PRODUCT SUMMARY V_{DS} (V) -60 $R_{DS(on)}$ (Ω) at V_{GS} = -10 V 0.1550 $R_{DS(on)}$ (Ω) at V_{GS} = -4.5 V 0.2130 I_D (A) -6.46

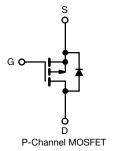
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_a and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





ROHS COMPLIANT HALOGEN FREE



ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA411CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATING	GS (T _C = 25 °C, unless	s otherwise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	-60	V	
Gate-source voltage		V _{GS}	V _{GS} ± 20		
Continuous drain current	T _C = 25 °C	1	-6.46		
	T _C = 125 °C	I _D	-3.73		
Continuous source current (diode conduction) ^a		Is	-9	А	
Pulsed drain current ^b		I _{DM}	-20		
Single pulse avalanche current	e avalanche current		-14		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	9.8	mJ	
Maximum power dissipation	T _C = 25 °C	D	13.6	W	
	T _C = 125 °C	P_{D}	4.5		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e		-	260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient P	CB mount c	R_{thJA}	90	°C/W
Junction-to-case (drain)		R _{th.IC}	11	C/VV

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V _{DS}	V _{GS} =	0 V, I _D = -250 μA	-60	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = -250 μA	-1.5	-2.0	-2.5	V	
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = -60 V	-	-	-1	μΑ	
Zero gate voltage drain current	I_{DSS}	V _{GS} = 0 V	V _{DS} = -60 V, T _J = 125 °C	-	-	-50		
		V _{GS} = 0 V	V _{DS} = -60 V, T _J = 175 °C	-	-	-250		
On-state drain current ^a	I _{D(on)}	V _{GS} = -10 V	V _{DS} ≥ -5 V	-6	-	-	Α	
	, ,	V _{GS} = -10 V	I _D = -3.5 A	-	0.1255	0.1550		
Drain acurae an etate	В	V _{GS} = -10 V	I _D = -3.5 A, T _J = 125 °C	-	-	0.2639	Ω	
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = -10 V	I _D = -3.5 A, T _J = 175 °C	-	-	0.3261		
_		V _{GS} = -4.5 V	I _D = -3 A	-	0.1645	0.2130	1	
Forward transconductance b	9 _{fs}	V _{DS} =	-15 V, I _D = -3.5 A	-	6	-	S	
Dynamic ^b								
Input capacitance	C _{iss}			-	421	590		
Output capacitance	Coss	$V_{GS} = 0 V$	V _{DS} = -25 V, f = 1 MHz	-	64	90	pF	
Reverse transfer capacitance	C _{rss}			-	35	50		
Total gate charge ^c	Qg			-	10.2	15.5		
Gate-source charge ^c	Q _{gs}	V _{GS} = -10 V	$V_{DS} = -30 \text{ V}, I_{D} = -6.5 \text{ A}$	-	2.2	-	nC	
Gate-drain charge ^c	Q _{gd}			-	2.6	-		
Gate resistance	R_g		f = 1 MHz	2.50	5.18	7.80	Ω	
Turn-on delay time ^c	t _{d(on)}			-	7	12		
Rise time ^c	t _r	$V_{DD} = -30 \text{ V}, \text{ R}_{L} = 12 \Omega$ $I_{D} \cong -2.5 \text{ A}, \text{ V}_{GEN} = -10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	4	7	ns	
Turn-off delay time ^c	t _{d(off)}			-	17	29		
Fall time ^c	t _f			-	4	7	1	
Source-Drain Diode Ratings and Charact	eristics ^b				•			
Pulsed current a	I _{SM}			-	-	-20	Α	
Forward voltage	V_{SD}	I _F = -3.5 A, V _{GS} = 0 V		-	-0.88	-1.2	V	
Body diode reverse recovery time	t _{rr}			-	24	48	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = -2 A, di/dt = 100 A/μs		-	28	56	nC	
Reverse recovery fall time	ta			-	21	-		
Reverse recovery rise time	t _b			-	3	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-3.4	-	Α	

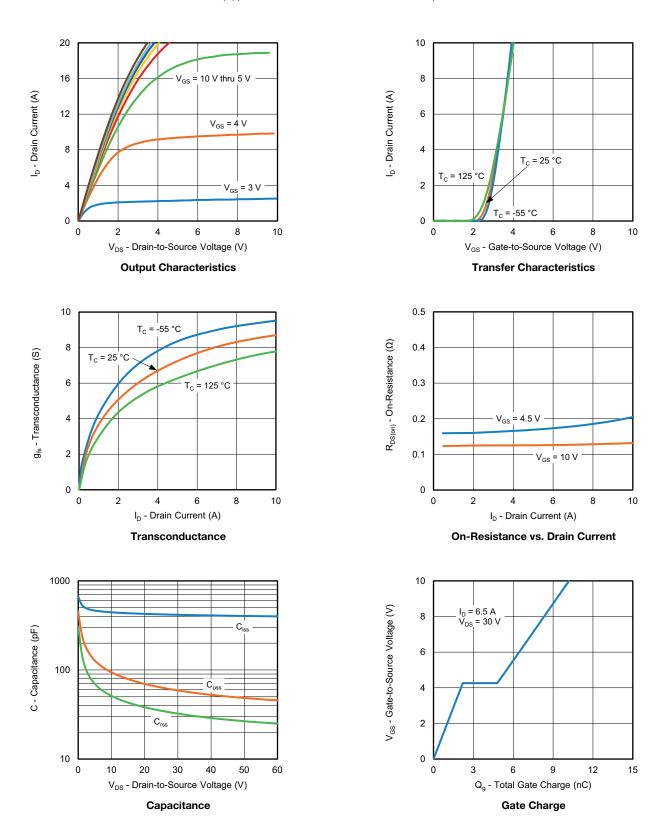
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

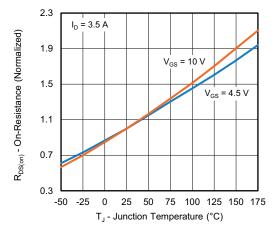


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

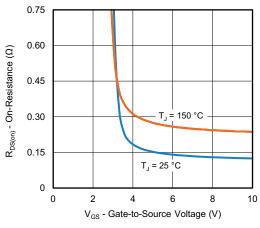




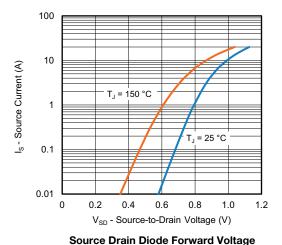
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature

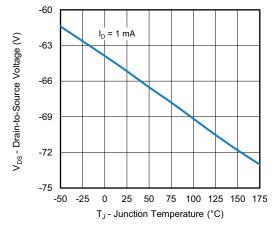


On-Resistance vs. Gate-to-Source Voltage

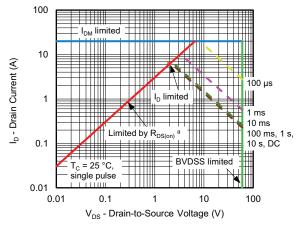


1.0 0.7 I_D = -250 μA V_{GS(th)} - Variance (V) 0.4 $I_D = -5 \text{ mA}$ 0.1 -0.2 -0.5 -50 -25 25 50 75 100 125 150 175 T_J - Junction Temperature (°C)

Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



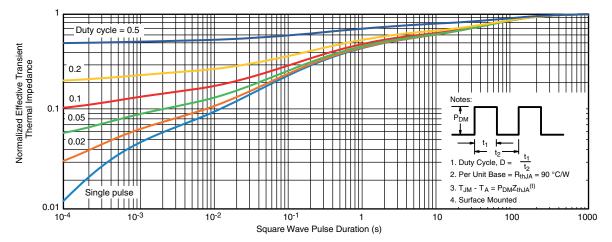
Safe Operating Area

Note

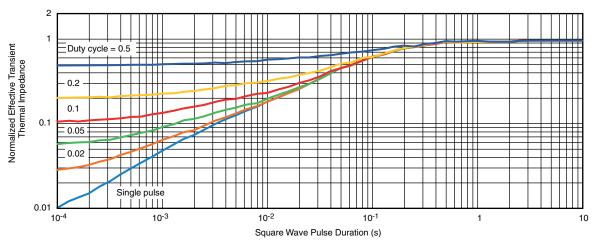
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

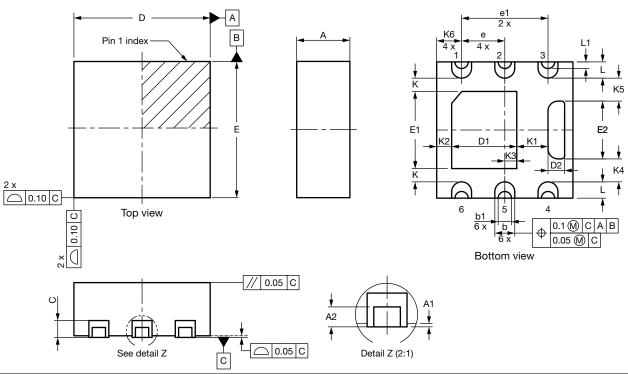


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63171.



PowerPAK® SC70W-6L SIDEWETTABLE



DIM.		MILLIMETERS			INCHES			
DIWI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	0.70	0.80	0.90	0.027	0.031	0.035		
A1	0.00	0.02	0.05	0.000	0.001	0.002		
A2	0.10	-	-	0.004	-	-		
b	0.25	0.30	0.35	0.010	0.012	0.014		
b1	0.15	0.20	0.23	0.006	0.008	0.009		
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	1.95	2.05	2.15	0.077	0.081	0.085		
D1	0.88	0.98	1.08	0.035	0.039	0.043		
D2	0.20	0.25	0.30	0.008	0.010	0.012		
E	1.95	2.05	2.15	0.077	0.081	0.085		
E1	1.06	1.16	1.26	0.042	0.046	0.050		
E2	0.82	0.87	0.92	0.032	0.034	0.036		
е		0.65 BSC			0.026 BSC			
e1		1.30 BSC		0.026 BSC 0.051 BSC				
K		0.20 typ.			0.008 typ.			
K1		0.47 typ.			0.019 typ.			
K2		0.23 typ.		0.009 typ.				
K3		0.18 typ.		0.007 typ.				
K4		0.35 typ.		0.014 typ.				
K5		0.35 typ.		0.014 typ.				
K6		0.38 typ.			0.015 typ.			
L	0.15	0.25	0.35	0.006	0.010	0.014		
L1	-	0.10	-	-	0.004	-		

DWG: 6076

Notes

- Package outline exclusive of mold flash and metal burr
- Package outline inclusive of plating

Revison: 10-Jan-2020 1 Document Number: 77413



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