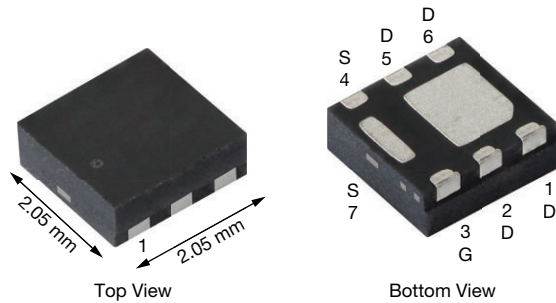


Automotive P-Channel 12 V (D-S) 175 °C MOSFET

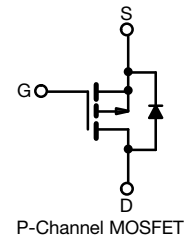
PowerPAK® SC-70W-6L Single

Marking Code: QAAXXXX

PRODUCT SUMMARY	
V_{DS} (V)	-12
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.019
$R_{DS(on)}$ (Ω) at $V_{GS} = -2.5$ V	0.026
$R_{DS(on)}$ (Ω) at $V_{GS} = -1.8$ V	0.040
I_D (A)	-9
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA409CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-12	V
Gate-source voltage		V_{GS}	± 8	
Continuous drain current ^a	$T_C = 25$ °C	I_D	-9	A
	$T_C = 125$ °C		-9	
Continuous source current (diode conduction) ^a		I_S	-9	
Pulsed drain current ^b		I_{DM}	-36	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	-15	mJ
Single pulse avalanche energy		E_{AS}	11.25	
Maximum power dissipation	$T_C = 25$ °C	P_D	13.6	W
	$T_C = 125$ °C		4.5	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^c	R_{thJA}	90	°C/W
Junction-to-case (drain)		R_{thJF}	11	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Not intended for continuous use with positive gate voltage > 3.0 V



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = -250\text{ }\mu\text{A}$		-12	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-0.45	-0.7	-1.0	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = -12\text{ V}$	-	-	-1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = -12\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -12\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	-150	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = -4.5\text{ V}$	$V_{DS} \geq 5\text{ V}$	-8	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$	$I_D = -4.5\text{ A}$	-	0.0142	0.019	Ω
		$V_{GS} = -4.5\text{ V}$	$I_D = -4.5\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0253	
		$V_{GS} = -4.5\text{ V}$	$I_D = -4.5\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0288	
		$V_{GS} = -2.5\text{ V}$	$I_D = -3\text{ A}$	-	0.0198	0.026	
		$V_{GS} = -1.8\text{ V}$	$I_D = -2\text{ A}$	-	0.0303	0.040	
Forward transconductance ^b	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -4\text{ A}$		-	20	-	S
Dynamic ^b							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = -6\text{ V}, f = 1\text{ MHz}$	-	2191	3070	μF
Output capacitance	C_{oss}			-	374	525	
Reverse transfer capacitance	C_{rss}			-	361	510	
Total gate charge ^c	Q_g	$V_{GS} = -4.5\text{ V}$	$V_{DS} = -6\text{ V}, I_D = -8\text{ A}$	-	22	33	nC
Gate-source charge ^c	Q_{gs}			-	5	-	
Gate-drain charge ^c	Q_{gd}			-	6	-	
Gate resistance	R_g	f = 1 MHz		3.2	6.45	9.7	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong -2.5\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		-	15	25	ns
Rise time ^c	t_r			-	33	50	
Turn-off delay time ^c	$t_{d(off)}$			-	61	95	
Fall time ^c	t_f			-	44	70	
Source-Drain Diode Ratings and Characteristics							
Pulsed current ^a	I_{SM}			-	-	-36	A
Forward voltage	V_{SD}	$I_F = -4.5\text{ A}, V_{GS} = 0$		-	-0.72	-1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = -2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		-	14	28	ns
Body diode reverse recovery charge	Q_{rr}			-	6	12	nC
Reverse recovery fall time	t_a			-	7	-	ns
Reverse recovery rise time	t_b			-	7	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-0.8	-	A

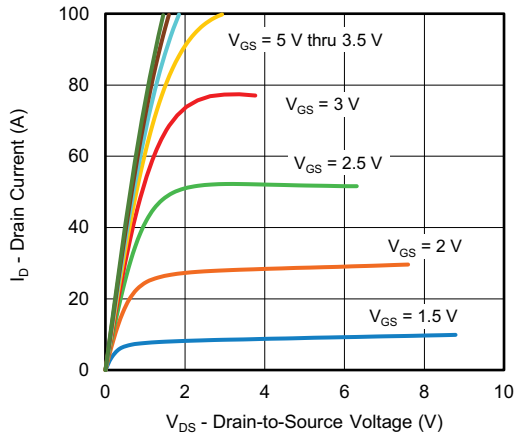
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

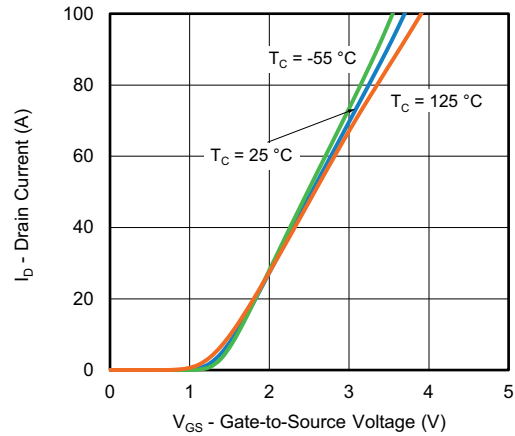
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



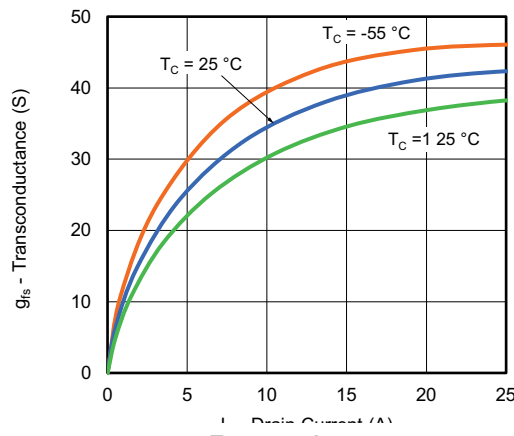
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



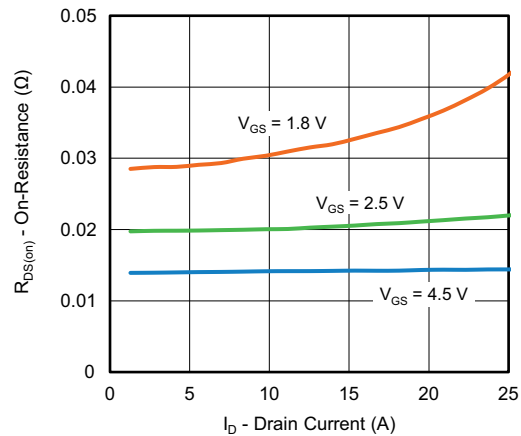
Output Characteristics



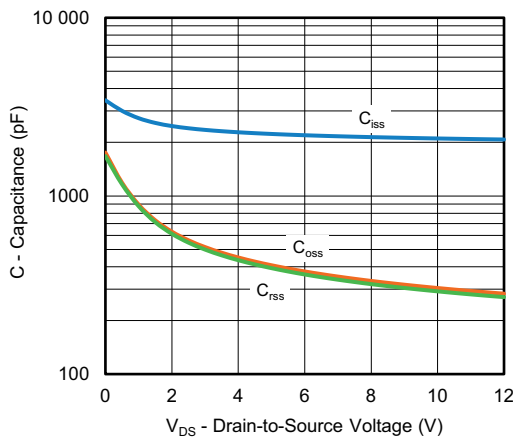
Transfer Characteristics



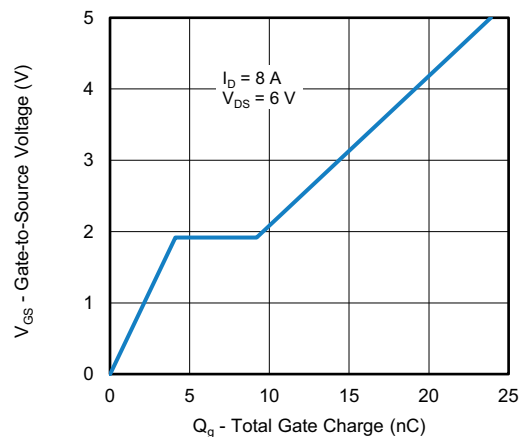
Transconductance



On-Resistance vs. Drain Current



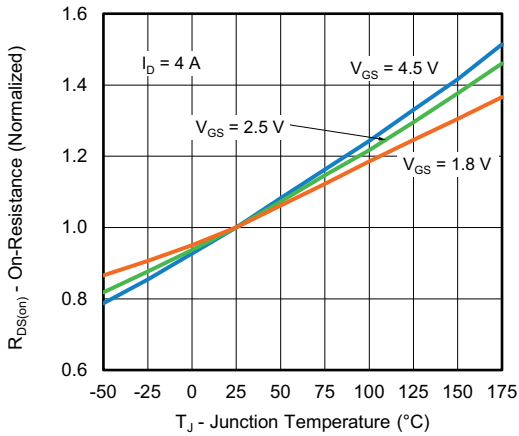
Capacitance



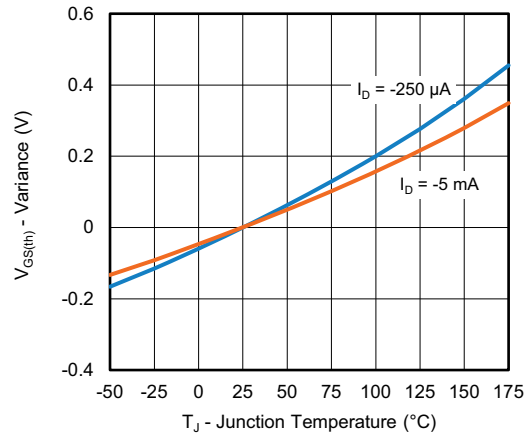
Gate Charge



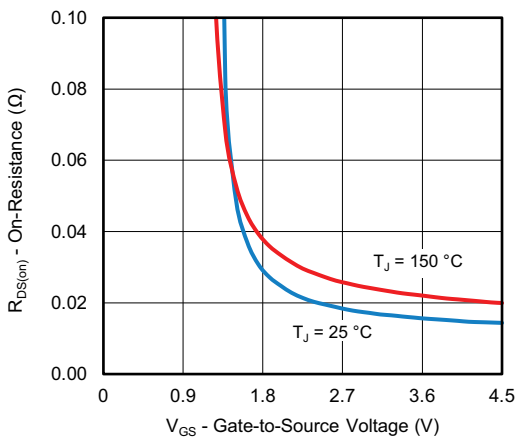
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



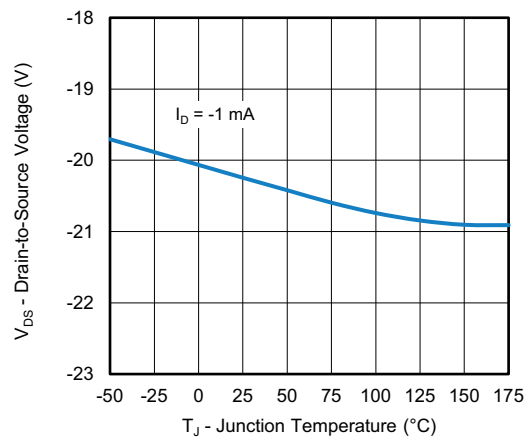
On-Resistance vs. Junction Temperature



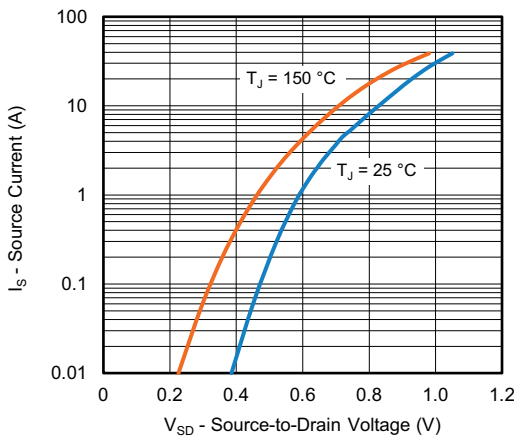
Threshold Voltage



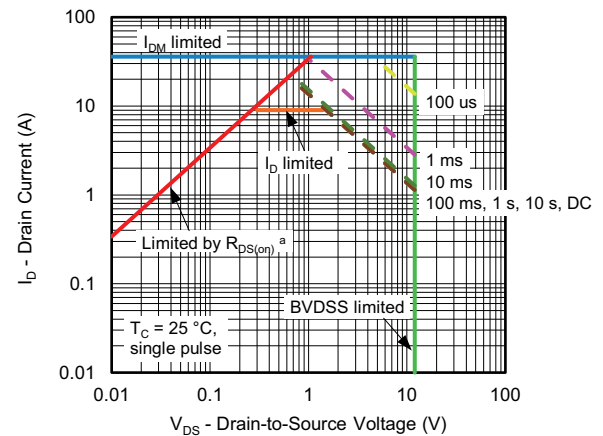
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Source-Drain Diode Forward Voltage



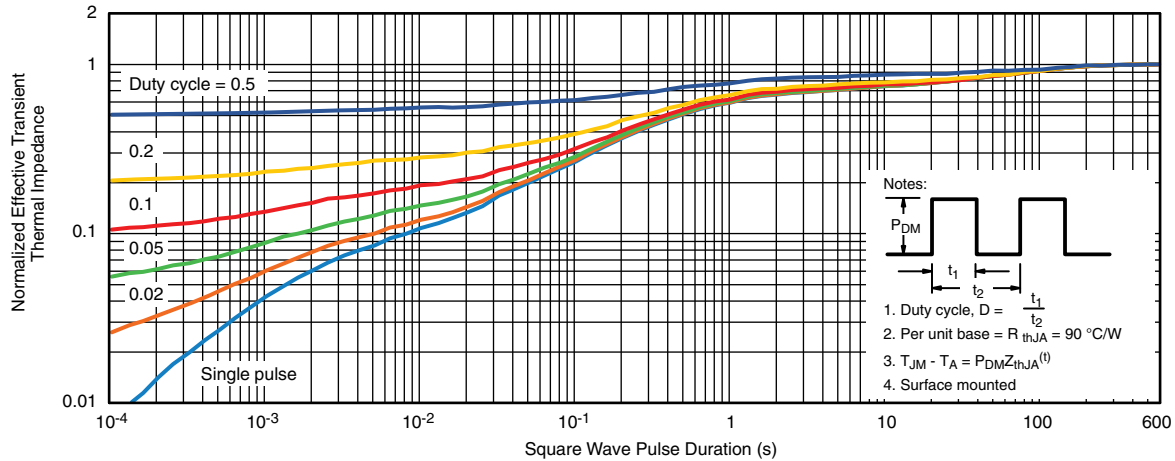
Safe Operating Area

Note

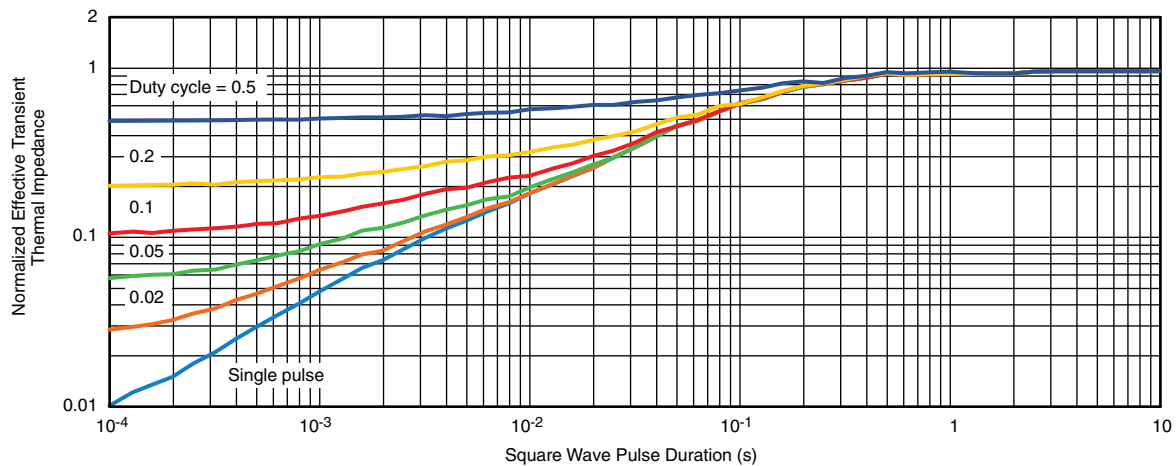
- a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

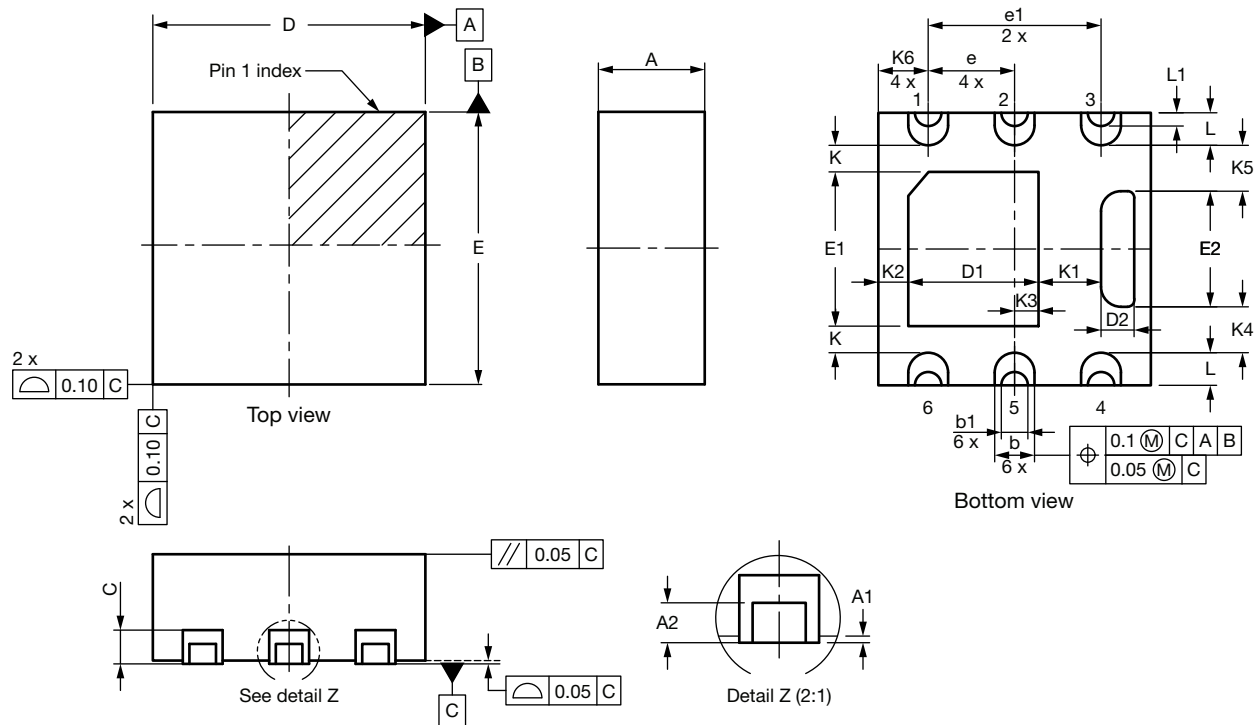


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62125.



PowerPAK® SC70W-6L SIDEWETTABLE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.10	-	-	0.004	-	-
b	0.25	0.30	0.35	0.010	0.012	0.014
b1	0.15	0.20	0.23	0.006	0.008	0.009
C	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.05	2.15	0.077	0.081	0.085
D1	0.88	0.98	1.08	0.035	0.039	0.043
D2	0.20	0.25	0.30	0.008	0.010	0.012
E	1.95	2.05	2.15	0.077	0.081	0.085
E1	1.06	1.16	1.26	0.042	0.046	0.050
E2	0.82	0.87	0.92	0.032	0.034	0.036
e	0.65 BSC			0.026 BSC		
e1	1.30 BSC			0.051 BSC		
K	0.20 typ.			0.008 typ.		
K1	0.47 typ.			0.019 typ.		
K2	0.23 typ.			0.009 typ.		
K3	0.18 typ.			0.007 typ.		
K4	0.35 typ.			0.014 typ.		
K5	0.35 typ.			0.014 typ.		
K6	0.38 typ.			0.015 typ.		
L	0.15	0.25	0.35	0.006	0.010	0.014
L1	-	0.10	-	-	0.004	-

ECN: C19-1644-Rev. A, 10-Jan-2020
DWG: 6076

Notes

- Package outline exclusive of mold flash and metal burr
- Package outline inclusive of plating



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