User's Guide

LV14360PEVM Evaluation Module

ABSTRACT

The Texas Instruments LV14360PEVM evaluation module (EVM) helps designers evaluate the operation and performance of the LV14360 wide-input Simple Switcher® buck regulator. This document describes the setup and the input/output connections of the EVM. Included are the board layout, schematic, and bill of materials.

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Trademarks

1 Introduction

The LV14360 is a 60-V, 3-A step-down regulator with 1-µA shutdown current. With a wide-input range from 4.3 V to 60 V, it is suitable for a wide range of applications from automotive to industry for power conditioning from unregulated sources. The LV14360PEVM evaluation board is designed to provide the design engineer with a fully functional power converter based on the buck topology to evaluate the LV14360 series operation and performance.

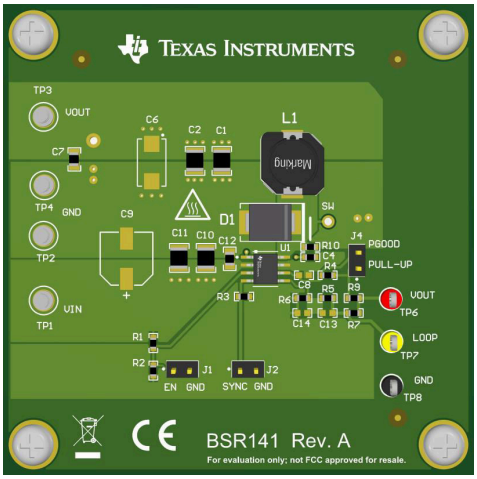

Figure 1-1. LV14360PEVM Board

EVM Features

- 7-V to 60-V input voltage range
- 5-V output voltage
- Up to 3-A output current
- 500-kHz switching frequency
- Power good flag output
- Internal compensation

Note

Risk of Electric Shock for Voltage Exceeding 50 VDC

Table 1-1. Device and Package Configurations

CONVERTER	EVM	IC	PACKAGE
U1	LV14360PEVM	LV14360PDDAR	SO-8

2 Setup

This section describes the jumpers and connectors on the EVM and how to properly connect, set up, and use the LV14360PEVM.

2.1 Input/Output Connector Description

VIN — Terminal TP1 – The power input terminal for the converter. Adjacent to it is the GND reference ground. Use this terminal to attach the EVM to a cable harness.

VOUT — Terminal TP3 – The regulated output voltage for the converter. Adjacent to it is the GND reference ground.

GND — Terminal TP2, TP4 – The ground reference for the converter. Use these terminals to attach the EVM to a cable harness.

EN — Jumper J1 – Used to enable the switch-mode converter. The device will be enabled when the respective jumper is high or floating, and disabled when low. EN turnon trip point also can be programmed by changing R1 or R2. Refer to LV14360 data sheet for enable and adjustable undervoltage lockout.

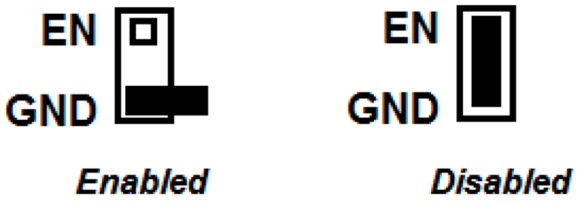

Figure 2-1. Enable Jumper Setting

SYNC — Jumper J2 – Used to synchronize the switching frequency to external clock. Refer to data sheet for detailed application information.

PGOOD — Jumper J4 – Used to monitor the Power-Good flag. This flag indicates whether the output voltage has reached its regulation point. The U1 PGOOD pin is an open-drain output that requires a pullup resistor to the appropriate logic voltage (any voltage less than 7 V). A pre-installed resistor R4 of 10.2 kΩ is tied to the PGOOD pin and R9 of 49.9 Ω brought output to J4 PULLUP pin.

Test point — TP6, TP7, TP8 – Test points used for loop response measurements

2.2 Adjusting the Output Voltage

The default setting output voltage is 5.0 V.

If other outputs need to be configured, then adjust the feedback resistors using Equation 1.

$$V_{OUT} = V_{FB} (1 + (R5 / R6)) \quad (1)$$

where

- V_{FB} = 0.75 V

CAUTION

CAUTION: R9 must be removed if the output voltage is changed higher than 7 V.

3 Board Layout

Figure 3-1 to Figure 3-4 show the board layout for the LV14360PEVM. The PCB consists of a 4-layer design. 2-oz copper planes are applied on all four layers to dissipate heat with an array of thermal vias under the thermal pad to connect to all four layers.

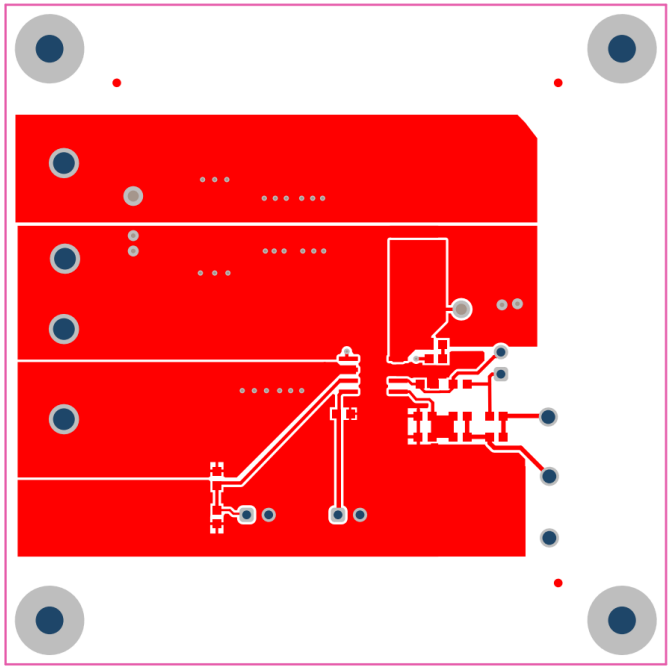

Figure 3-1. Top Layer

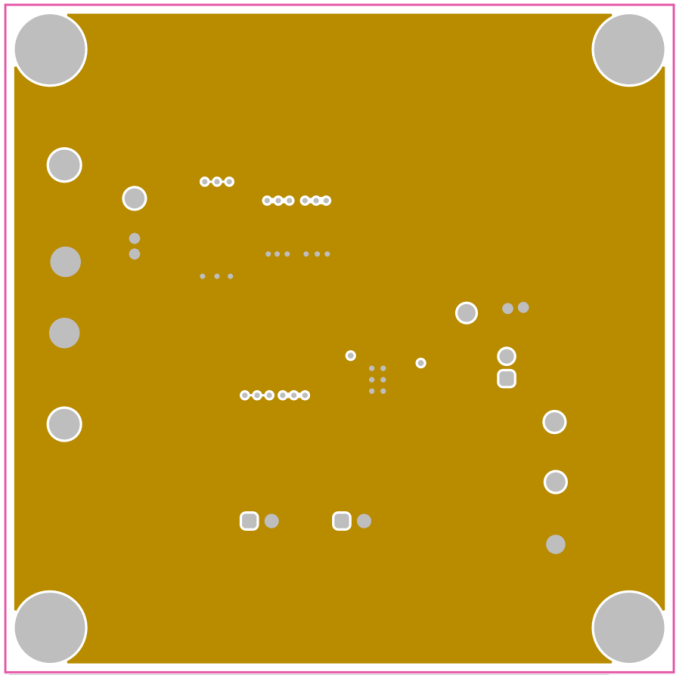

Figure 3-2. Middle Layer 1

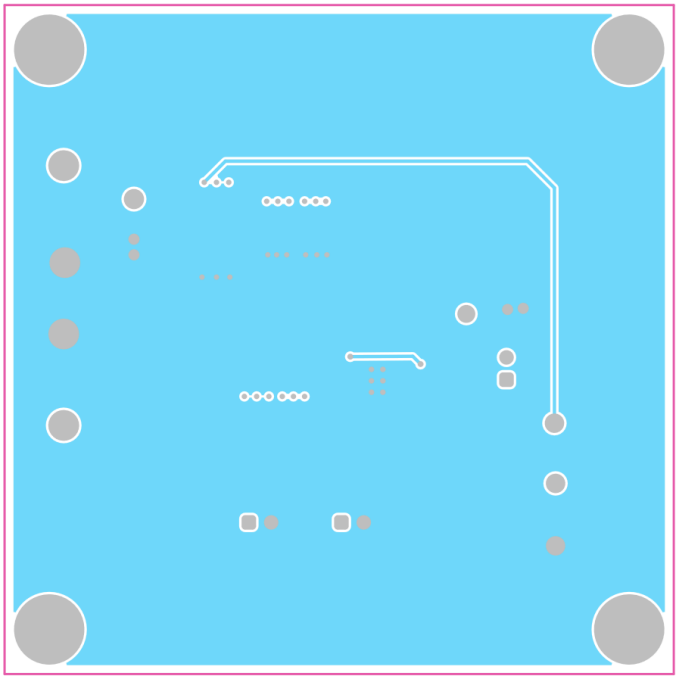

Figure 3-3. Middle Layer 2

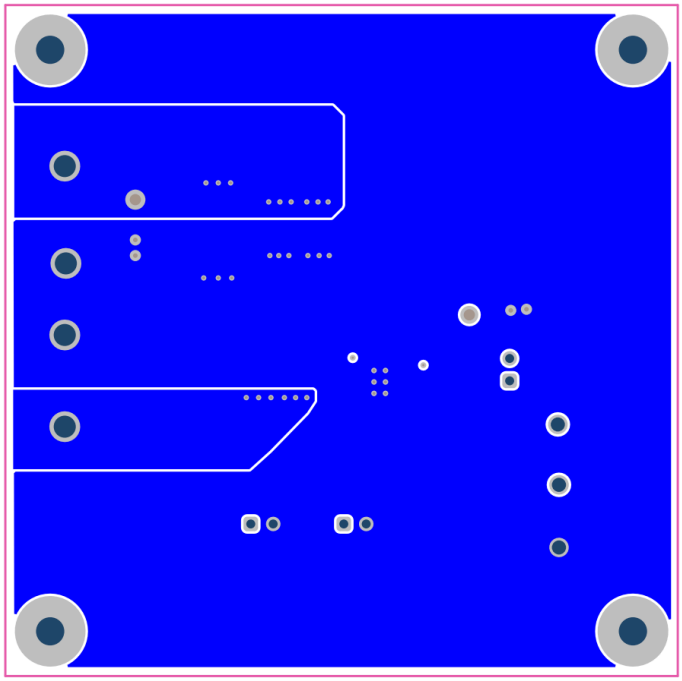

Figure 3-4. Bottom Layer

4 Schematic and Bill of Materials

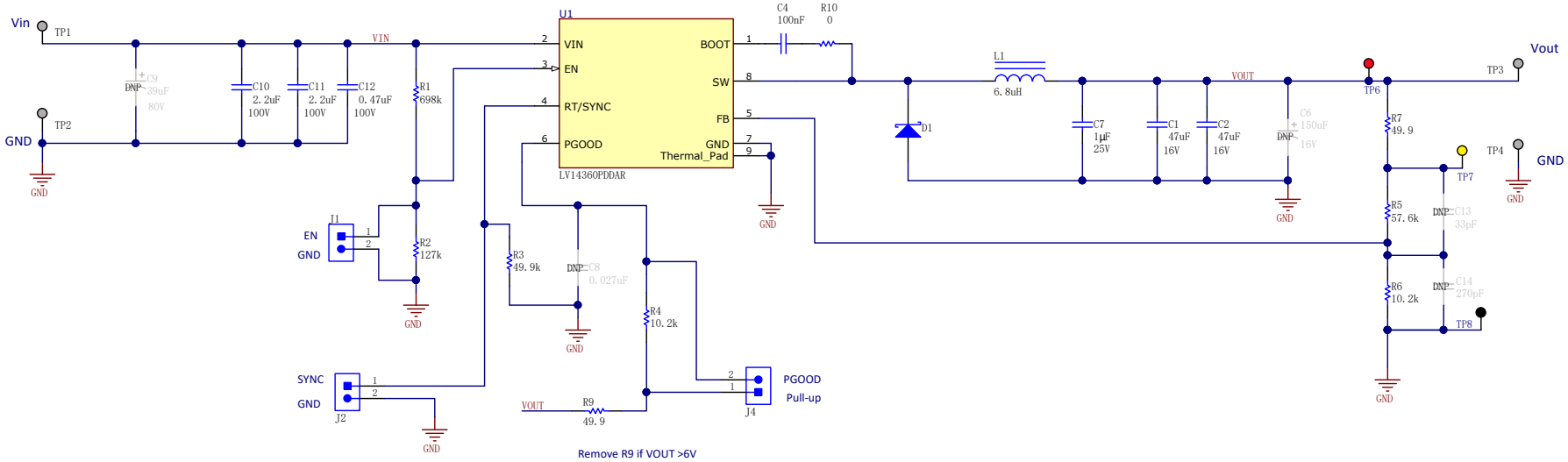

Figure 4-1. LV14360PEVM Schematic

Table 4-1. LV14360PEVM Bill of Materials (BOM)

DESIGNATOR	DESCRIPTION	PART NUMBER	FOOTPRINT	QTY
C1, C2	CAP, CERM, 47 µF, 16V, ±20%, X5R, 1210	GRM32ER61C476ME15L	1210	2
C4	CAP, CERM, 0.1 µF, 16 V ±10%, X7R, 0603	GCM188R71C104KA37J	0603	1
C7	CAP, CERM, 1 µF 25 V, ±10%, X7R, 0805	'GRM219R71E105KA88D	0805	1
C10, C11	CAP, CERM, 2.2 µF, 100 V, ±10%, X7R, 1210	GRM32ER72A225KA35L	1210	2
C12	CAP, CERM, 0.47 µF, 100 V, ±10%, X7R, 0805	GRM21BR72A474KA73L	0805	1
D1	Diode, Schottky, 60 V, 5 A, SMC	B560C-13-F	SMC	1
J1, J2, J4	Header, 100 mil, 2x1, Gold, TH	TSW-102-07-G-S	TSW-102-07-G-S	3
L1	Inductor, 6.8 µH, 5.2 A, 0.0185 Ω	7447714068	WE-HCI	1
R1	RES, 698 k, 1%, 0.1 W, 0603	CRCW0603698KFKEA	0603	1
R2	RES, 127 k, 1%, 0.1 W, 0603	CRCW0603127KFKEA	0603	1
R3	RES, 49.9 k, 1%, 0.1 W, 0603	CRCW060349K9FKEA	0603	1
R5	RES, 57.6k, 1%, 0.1W, 0603	CRCW060357K6FKEA	0603	1
R4, R6	RES, 10.2 k, 1%, 0.1 W, 0603	CRCW060310K2FKEA	0603	2
R7, R9	RES, 49.9 Ω, 1%, 0.1W, 0603	CRCW060349R9FKEA	0603	2
R10	RES, 0 Ω, 5%, 0.1 W, 0603	CRCW06030000Z0EA	0603	1
TP1, TP2, TP3, TP4	Terminal, Turret, TH, Double	1502-2	Keystone1502-2	4
TP6	Test Point, TH, Multipurpose, Red	5010	Keystone5010	1
TP7	Test Point, TH, Multipurpose, Yellow	5014	Keystone5014	1
TP8	Test Point, TH, Multipurpose, Black	5011	Keystone5011	1
U1	IC, 60 V, 3 A, Current Mode, Buck Regulator	LV14360PDDAR	SO-8	1

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