AN-1767 LME49721 Evaluation Board

1 Introduction

This application report provides information on how to use the LME49721 demonstration board for evaluation of the LME49721 Rail-to-Rail Input/Output, high performance, high fidelity operational amplifier. The LME49721 demonstration board is designed for the user to fully evaluate the LME49721 in either inverting, non-inverting, or unity gain voltage follower configuration. This board is shown in Figure 1.

2 General Description

The LME49721 is a low distortion (THD + N = 0.00008%, A_V = 2, V_{OUT} = 4V_{P-P}, f_{IN} = 1kHz), low noise (4nV/$\sqrt{Hz}$) Rail-to-Rail Input/Output operational amplifier optimized and fully specified for high performance, high fidelity applications. The Rail-to-Rail Input/Output operational amplifier delivers superior signal amplification for outstanding performance. The LME49721 has a slew rate of ±8.5V/μs, an output current capability of ±9.7mA, and an input bias current of 40fA. This operational amplifier can easily drive 10kΩ loads to within 10mV of each power supply voltage.

3 Operating Conditions

The LME49721 has a supply voltage range from +2.2V to +5.5V single supply or ±1.1V to ±2.75V dual supply. Please note the demonstration board is designed for dual supply operation only.

4 Demonstration Board Schematic

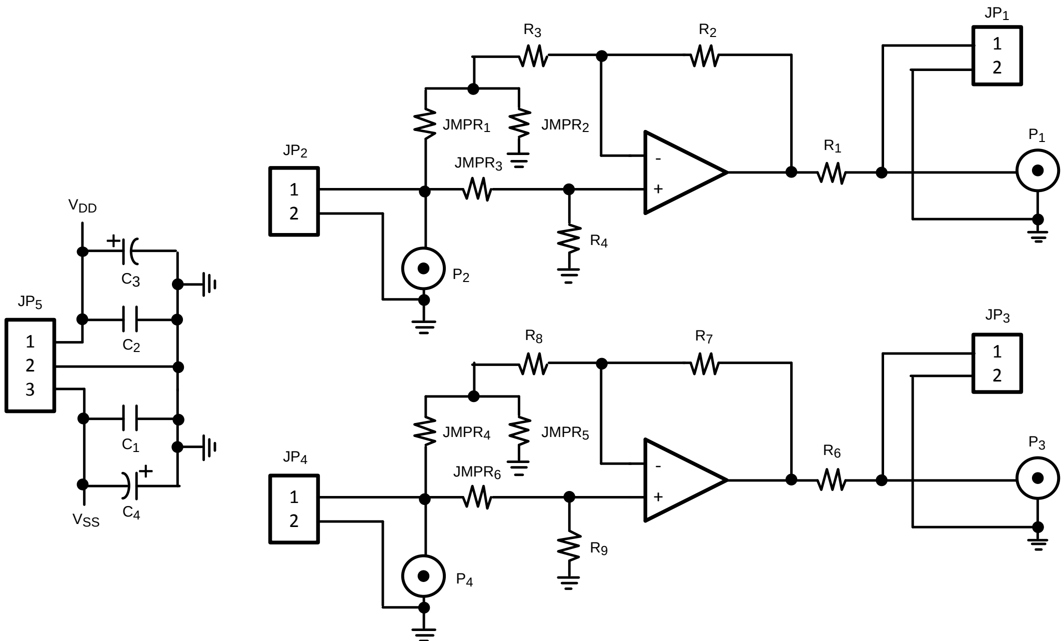


Figure 1. LME49721 Demo Board Schematic

Table 1. Demo Board Connections

Designator	Label	Function
JP1	OUT_1	Output Signal A
JP2	IN_1	Input Signal A
JP3	OUT_2	Output Signal B
JP4	IN_2	Input Signal B
JP5	$+V_{DD}$ GND $-V_{SS}$	Power Supply Connections
P1	OUT_1	Output Signal A
P2	IN_1	Input Signal A
P3	OUT_2	Output Signal B
P4	IN_2	Input Signal B

5 Configuring the LME49721 Amplifier

5.1 *Inverting Configuration*

Figure 2 shows the typical connection for a inverting amplifier. The output voltage is centered on zero with a gain of $A_V = -R_2/R_3$. Table 2 shows the recommended Bill of Materials for an inverting amplifier.

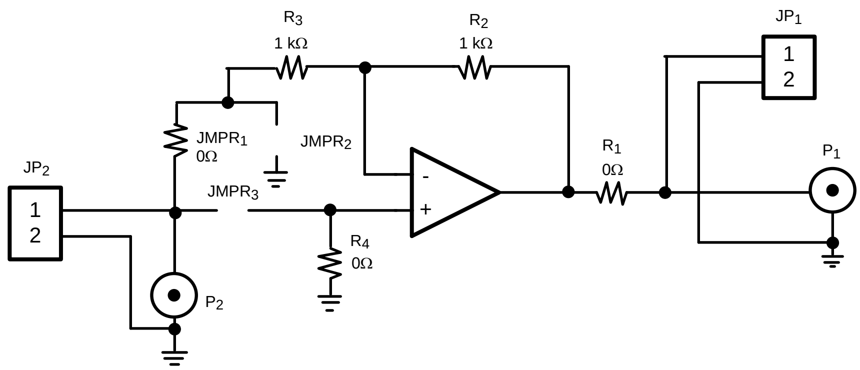


Figure 2. Inverting Amplifier

You can configure the LME49721 demonstration board in an inverting configuration by making the following changes:

1. Place 0Ω resistor (or short) $JMPR_1$ ($JMPR_4$).
2. Place 0Ω resistor (or short) R_4 (R_9).
3. Place the desired value resistor (1kΩ minimum) to set the inverting gain in R_3 (R_8) and R_2 (R_7).
4. Leave the $JMPR_2$ ($JMPR_5$) and $JMPR_3$ ($JMPR_6$) open.
5. Place 0Ω resistor (or short) R_1 (R_6).

Table 2. Example Demonstration Board Bill of Materials for Inverting Configuration

Description	Designator	Part Number	Manufacturer
Ceramic Capacitor 0.1µF, 10% 50V 0805 SMD	C1, C2	C0805C104K3RAC7533	Kemet
Tantalum Capacitor 10µF, 10% 20V, B-size	C3, C4	T491B106K025AT	Kemet
Resistor 0 Ω, 1/8W 1% 0805 SMD	$JMPR_1$, $JMPR_4$, R_1, R_4, R_6, R_9	CRCW0805000020EA	Vishay
Resistor 10kΩ, 1/8W, 1% 0805 SMD	R_2, R_3, R_8, R_7	CRCW080510KOFKEA	Vishay
Header, 2–Pin	JP_1, JP_2, JP_3, JP_4		
Header, 3–Pin	JP_5		
SMA standup connectors	P1–P4 (Optional)	132134	Amphenol Connex

5.2 Non-Inverting Configuration

Figure 3 shows the typical connection for a non-inverting amplifier. Again the output voltage is centered on zero but with a gain of $A_V = 1+ (R_2/R_3)$. Table 3 shows the recommended Bill of Materials for a non-inverting amplifier.

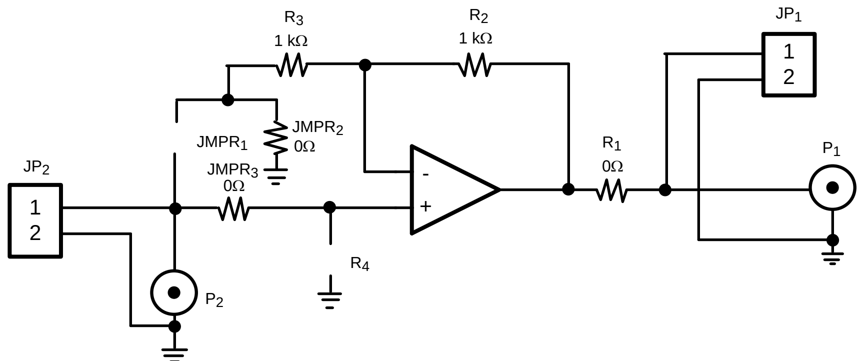


Figure 3. Non-Inverting Amplifier

You can configure the LME49721 demonstration board in Non-Inverting configuration by making the following changes:

1. Place 0Ω resistor (or short) $JMPR_2$ ($JMPR_5$) and $JMPR_3$ ($JMPR_6$).
2. Place the desired value resistors (1kΩ minimum) to set inverting gain in R_3 (R_8) and R_2 (R_7).
3. Leave the $JMPR_1$ ($JMPR_4$) and R_4 (R_9) open.
4. Place 0Ω resistor (or short) R_1 (R_6).

Table 3. Example Demonstration Board Bill of Materials for Non-Inverting Configuration

Description	Designator	Part Number	Manufacturer
Ceramic Capacitor 0.1μF, 10% 50V 0805 SMD	C1, C2	C0805C104K3RAC7533	Kemet
Tantalum Capacitor 10μF, 10% 20V, B-size	C3, C4	T491B106K025AT	Kemet
Resistor 0 Ω, 1/8W 1% 0805 SMD	$JMPR_2$, $JMPR_3$, $JMPR_5$, $JMPR_6$, R_1, R_6	CRCW0805000020EA	Vishay
Resistor 10kΩ, 1/8W, 1% 0805 SMD	R_2, R_3, R_7, R_8	CRCW080510KOFKEA	Vishay
Header, 2–Pin	JP_1, JP_2, JP_3, JP_4		
Header, 3–Pin	JP_5		
SMA standup connectors	P1–P4 (Optional)	132134	Amphenol Connex

5.3 Voltage Follower Configuration

Figure 4 shows the typical connection for a Voltage Follower amplifier or also called a Buffer. A Voltage Follower Amplifier can be used to solve impedance matching problems, to reduce power consumption in the source, or to drive heavy loads. The input impedance of the LME49721 is very high. Therefore, the input of the LME49721 does not load down the source. The Voltage Follower is a unity stable amplifier, 1V/V. Table 4 shows the recommended Bill of Materials for an inverting amplifier.

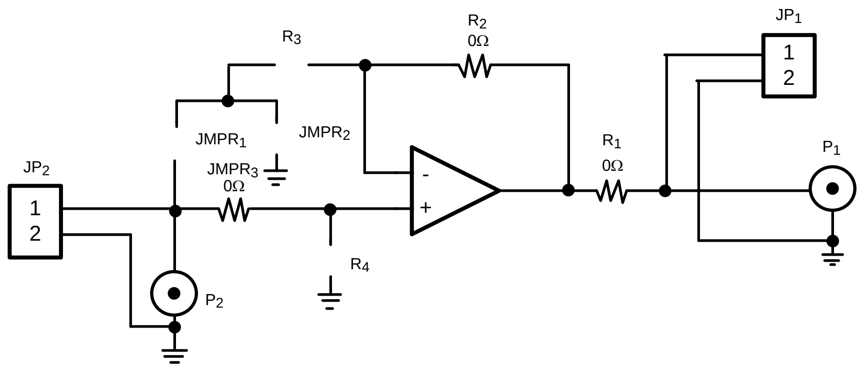


Figure 4. Voltage Follower Amplifier

You can configure the LME49721 demonstration board in a Voltage Follower configuration by making the following changes:

1. Place 0Ω resistor (or short) R_2 (R_7) and R_1 (R_6).
2. Place 0Ω resistor (or short) $JMPR_3$ ($JMPR_6$).
3. Leave R_3 (R_8) and R_4 (R_9) open.
4. Leave $JMPR_1$ ($JMPR_4$) and $JMPR_2$ ($JMPR_5$) open.

Table 4. Example Demonstration Board Bill of Materials for Voltage Follower Configuration

Description	Designator	Part Number	Manufacturer
Ceramic Capacitor 0.1μF, 10% 50V 0805 SMD	C1, C2	C0805C104K3RAC7533	Kemet
Tantalum Capacitor 10μF, 10% 20V, B-size	C3, C4	T491B106K025AT	Kemet
Resistor 0 Ω, 1/8W 1% 0805 SMD	$JMPR_3$, $JMPR_6$, R_1, R_2, R_6, R_7	CRCW0805000020EA	Vishay
Header, 2–Pin	JP_1, JP_2, JP_3, JP_4		
Header, 3–Pin	JP_5		
SMA standup connectors	P1–P4 (Optional)	132134	Amphenol Connex

6 Demonstration Board Layout

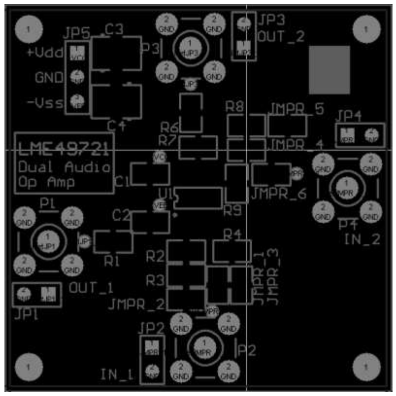


Figure 5. Top Silkscreen

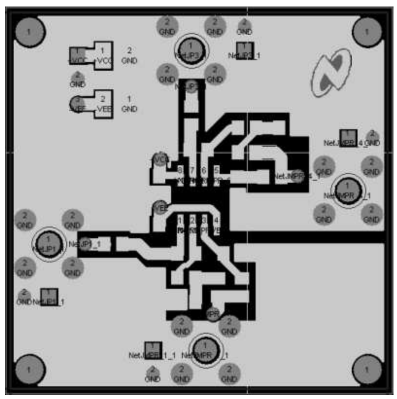


Figure 6. Top Layer

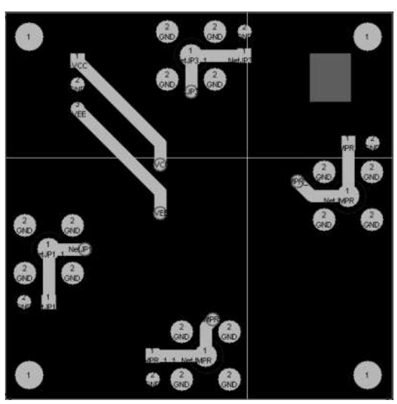
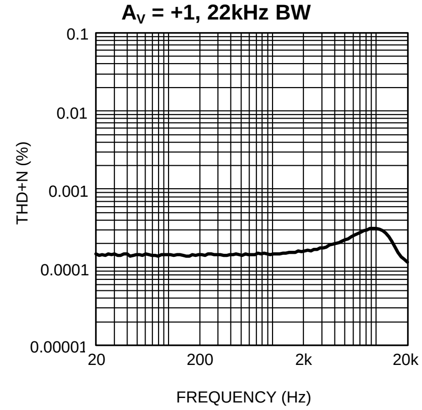


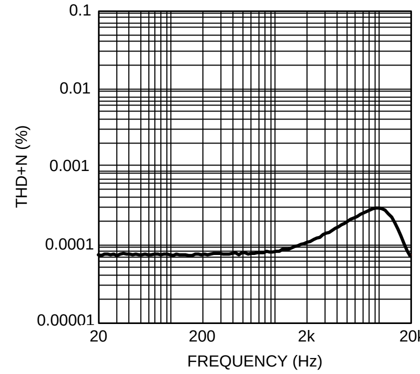
Figure 7. Bottom Layer

7 Typical Performance Characteristics

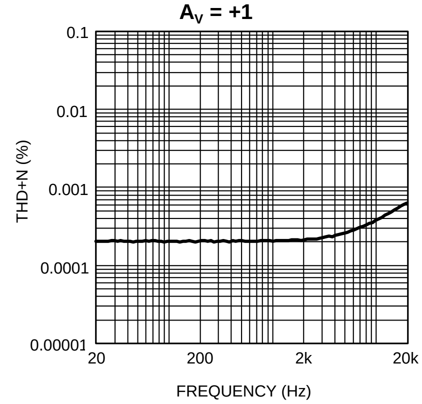
THD+N vs Frequency
V_S = 2.5V, V_{OUT} = 2V_{P-P}, R_L = 2kΩ
A_V = +1, 22kHz BW



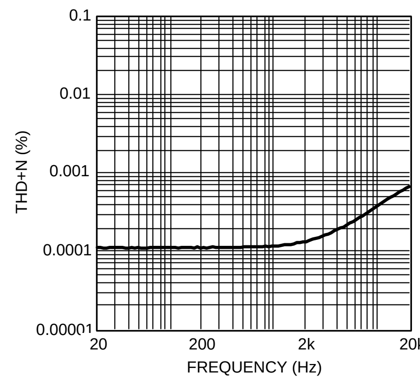
THD+N vs Frequency
V_S = ±2.5V, V_{OUT} = 4V_{P-P}, R_L = 2kΩ
A_V = 2, 22kHz BW



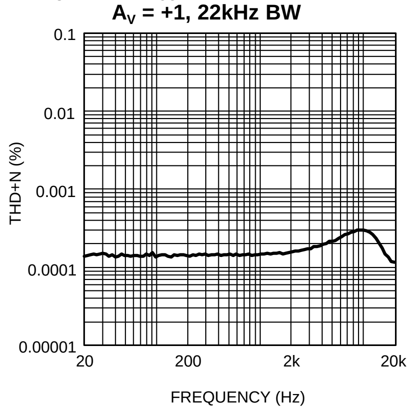
THD+N vs Frequency
V_S = 2.5V, V_{OUT} = 2V_{P-P}, R_L = 2kΩ
A_V = +1



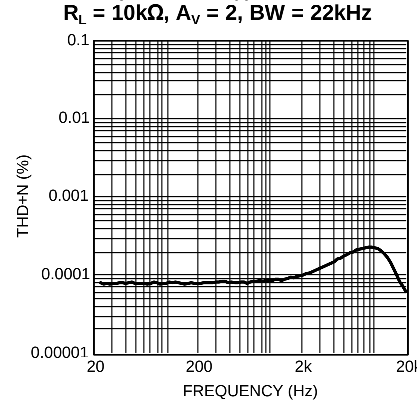
THD+N vs Frequency
V_S = ±2.5V, V_{OUT} = 4V_{P-P}
R_L = 2kΩ, A_V = 2



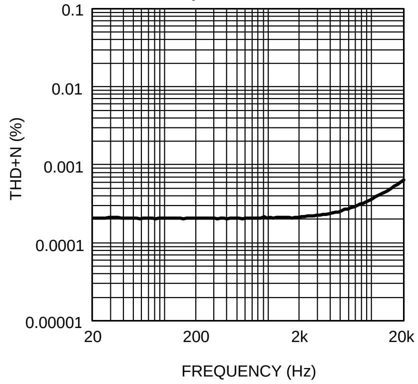
THD+N vs Frequency
V_S = 2.5V, V_{OUT} = 2V_{P-P}, R_L = 10kΩ
A_V = +1, 22kHz BW



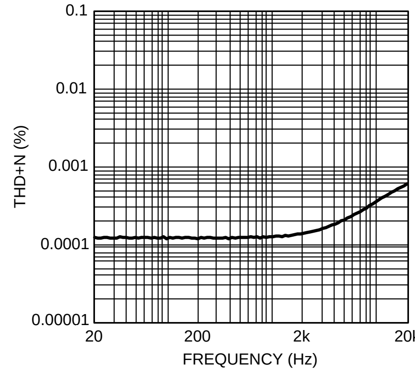
THD+N vs Frequency
V_S = ±2.5V, V_{OUT} = 4V_{P-P}
R_L = 10kΩ, A_V = 2, BW = 22kHz



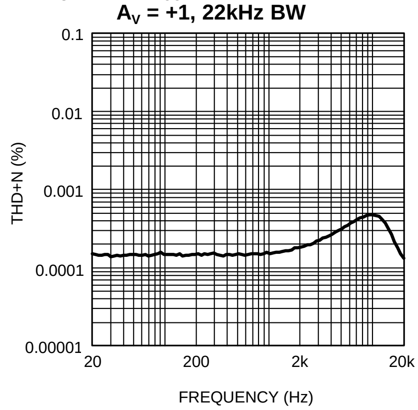
THD+N vs Frequency
V_S = 2.5V, V_{OUT} = 2V_{P-P}, R_L = 10kΩ
A_V = +1



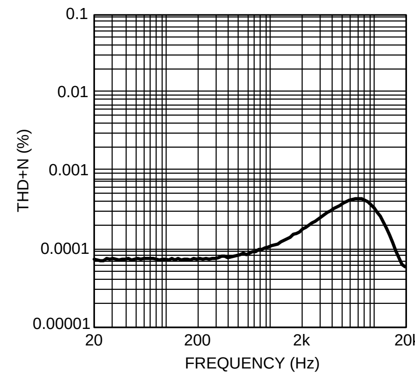
THD+N vs Frequency
V_S = ±2.5V, V_{OUT} = 4V_{P-P}
R_L = 10kΩ, A_V = 2



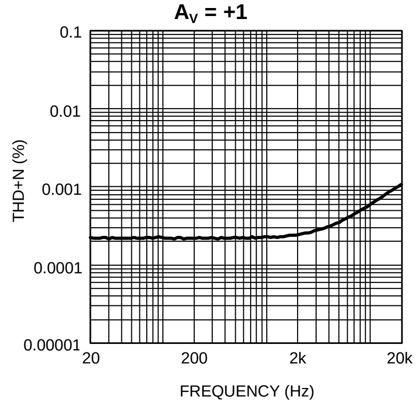
THD+N vs Frequency
V_S = 2.5V, V_{OUT} = 2V_{P-P}, R_L = 600Ω
A_V = +1, 22kHz BW



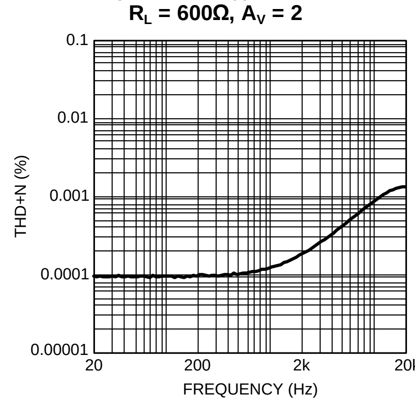
THD+N vs Frequency
V_S = ±2.5V, V_{OUT} = 4V_{P-P}
R_L = 600Ω, A_V = 2, BW = 22kHz



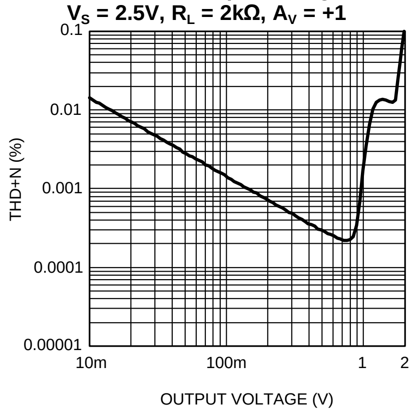
THD+N vs Frequency
V_S = 2.5V, V_{OUT} = 2V_{P-P}, R_L = 600Ω
A_V = +1



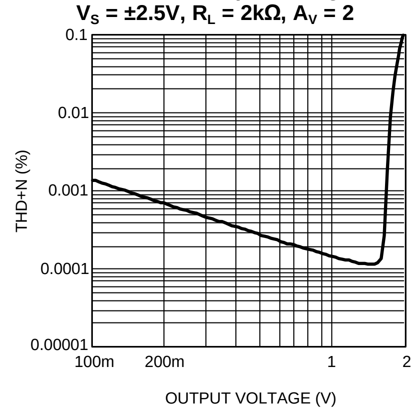
THD+N vs Frequency
V_S = ±2.5V, V_{OUT} = 4V_{P-P}
R_L = 600Ω, A_V = 2



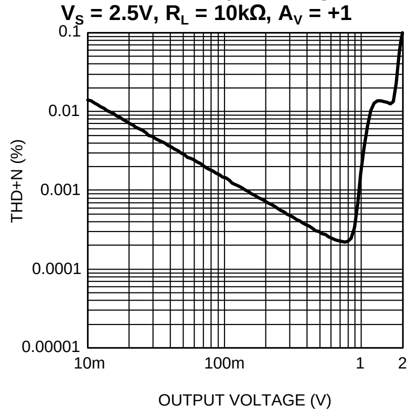
THD+N vs Output Voltage
V_S = 2.5V, R_L = 2kΩ, A_V = +1



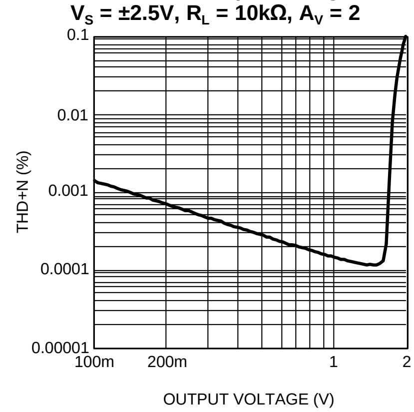
THD+N vs Output Voltage
V_S = ±2.5V, R_L = 2kΩ, A_V = 2



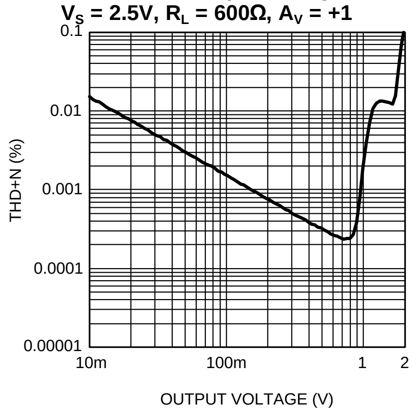
THD+N vs Output Voltage
V_S = 2.5V, R_L = 10kΩ, A_V = +1



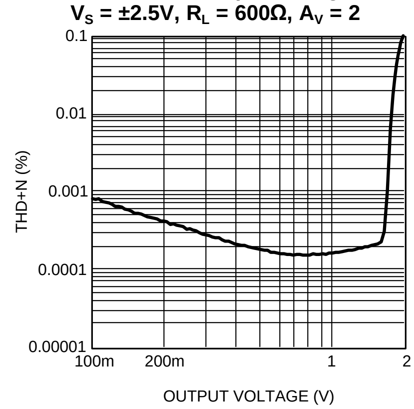
THD+N vs Output Voltage
V_S = ±2.5V, R_L = 10kΩ, A_V = 2



THD+N vs Output Voltage
V_S = 2.5V, R_L = 600Ω, A_V = +1



THD+N vs Output Voltage
V_S = ±2.5V, R_L = 600Ω, A_V = 2



8 Revision Table

Rev	Date	Description
1.0	02/22/08	Initial release.

IMPORTANT NOTICE

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