SN74LV594A-Q1 Automotive 8-Bit Parallel-Out Serial Shift Registers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classifcation Level C6
- Available in wettable flank QFN (WBQB) package
- 2 V to 5.5 V V_{CC} operation
- Maximum tpd of 6.5 ns at 5 V
- Typical V_{OLP} (output ground bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Support mixed-mode voltage operation on all ports
- 8-bit serial-in, parallel-out shift registers with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for shift and storage registers
- Latch-up performance exceeds 100 mA per JESD 78, Class II

2 Applications

- Output expansion
- LED matrix control
- 7-segment display control

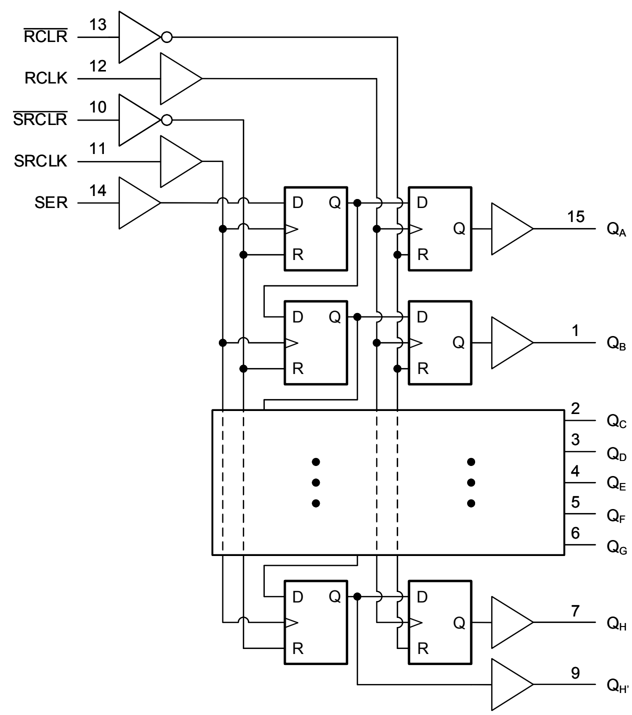
3 Description

The SN74LV594A-Q1 devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV594A-Q1	BQB (WQFN, 16)	3.60 mm × 2.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

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4 Revision History

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions

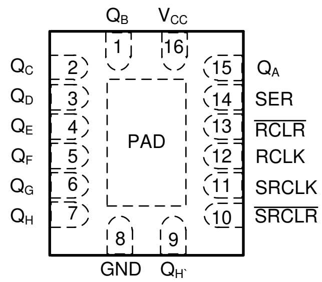


Figure 5-1. D, DB, or PW Package 16-Pin SOIC, SSOP, or TSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
Q_B	1	O	Output B
Q_C	2	O	Output C
Q_D	3	O	Output D
Q_E	4	O	Output E
Q_F	5	O	Output F
Q_G	6	O	Output G
Q_H	7	O	Output H
GND	8	G	Ground pin
$Q_{H'}$	9	O	Q_H inverted
$\overline{\text{SRCLR}}$	10	I	Serial clear
SRCLK	11	I	Serial clock
RCLK	12	I	Storage clock
$\overline{\text{RCLR}}$	13	I	Storage clear
SER	14	I	Serial input
Q_A	15	O	Output A
Vcc	16	P	Power pin
Thermal Pad		-	Thermal Pad[(1)]

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
V_I	Input voltage[(2)]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[(2)]		−0.5	7	V
V_O	Output voltage[(2)] [(3)]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$	−20		mA
I_{OK}	Output clamp current	$V_O < 0$	−50		mA
I_O	Continuous output current	V_O = 0 to V_{CC}	−25	25	mA
T_{stg}	Storage temperature		−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 [(1)]	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level input current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[(1)]		SN74LV594A-Q1	UNIT
		BQB (WQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.9	
Ψ_{JT}	Junction-to-top characterization parameter	9.5	
Ψ_{JB}	Junction-to-board characterization parameter	54.9	
Ψ_{JC}	Junction-to-bottom characterization parameter	32.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –2 µA	2.3 V	2			
	I_{OH} = –6 µA	3 V	2.48			
	I_{OH} = –12 µA	4.5 V	3.8			
V_{OL}	I_{OH} = –50 µA	2 V to 5.5 V			0.1	V
	I_{OH} = –2 µA	2.3 V			0.4	
	I_{OH} = –6 µA	3 V			0.44	
	I_{OH} = –12 µA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{CC}	V_I = V_{CC} of GND, I_O = 0	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		3.5		pF

6.6 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted). See Figure 6-1.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	65	80		35		MHz
			C_L = 50 pF	60	70		30		
t_{PLH}	SRCLK	Q_A – Q_H	C_L = 15 pF		6.4	10.6	1	12.5	ns
t_{PHL}					6.3	10.4	1	12.5	
t_{PLH}		$Q_{H'}$			7.4	12.1	1	15	
t_{PHL}	RCLK				7.2	11.6	1	15	
t_{PHL}		Q_A – Q_H			7.9	12.7	1	15.5	
		$Q_{H'}$			7.4	11.9	1	15.5	
t_{PLH}	$\overline{SRCLR}$	Q_A – Q_H	C_L = 50 pF		9.5	14.1	1	17	ns
t_{PHL}					10.8	15.5	1	19.5	
t_{PLH}		$Q_{H'}$			10.6	15.7	1	18.5	
t_{PHL}	$\overline{RCLR}$				11.3	16.1	1	20.5	
t_{PHL}		Q_A – Q_H			12.1	17.4	1	21	
		$Q_{H'}$			11.6	16.5	1	20.6	

6.7 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted). See Figure 6-1.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80	120		60		MHz
			C_L = 50 pF	55	105		40		
t_{PLH}	SRCLK	$Q_A – Q_H$	C_L = 15 pF		4.6	8	1	10.5	ns
t_{PHL}					4.9	8.2	1	10.5	
t_{PLH}		$Q_{H'}$			5.4	9.1	1	11.5	
t_{PHL}	RCLK				5.5	9.2	1	11.6	
t_{PHL}		$Q_A – Q_H$			6	9.8	1	12.1	
		$Q_{H'}$			5.6	9.2	1	12	
t_{PLH}	$\overline{\text{SRCLR}}$	$Q_A – Q_H$	C_L = 50 pF				1	12.5	ns
t_{PHL}							1	15	
t_{PLH}		$Q_{H'}$					1	14	
t_{PHL}	$\overline{\text{RCLR}}$						1	15.5	
t_{PHL}		$Q_A – Q_H$					1	16.1	
		$Q_{H'}$					1	16	

6.8 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted). See Figure 6-1.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C TO 125°C		UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	135	170		105		MHz
			C_L = 50 pF	120	140		85		
t_{PLH}	SRCLK	$Q_A – Q_H$	C_L = 15 pF		3.3	6.2	1	8	ns
t_{PHL}					3.7	6.5	1	8.5	
t_{PLH}		$Q_{H'}$			3.7	6.8	1	8.5	
t_{PHL}	RCLK				4.1	7.2	1	9	
t_{PHL}		$Q_A – Q_H$			4.5	7.6	1	9.5	
		$Q_{H'}$			4.1	7.1	1	9	
t_{PLH}	$\overline{\text{SRCLR}}$	$Q_A – Q_H$	C_L = 50 pF		4.9	7.8	1	9.6	ns
t_{PHL}					5.8	8.9	1	11	
t_{PLH}		$Q_{H'}$			5.5	8.6	1	10.5	
t_{PHL}	$\overline{\text{RCLR}}$				6	9.2	1	11.5	
t_{PHL}		$Q_A – Q_H$			6.6	10	1	12	
		$Q_{H'}$			6	9.2	1	11.5	

6.9 Timing Requirements: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range. See Figure 6-1.

			T_A = 25°C		–40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	7		8.5		ns
		$\overline{\text{RCKR}}$ or $\overline{\text{SCRCLR}}$ low	6		7.5		
t_{su}	Setup time	SER before SRCLK↑	5.5		6		ns
		SRCLK↑ before RCLK↑	8		10		
		$\overline{\text{SCRCLR}}$ low before RCLK↑(1)	8.5		10.5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	6		7.5		
		$\overline{\text{RCLK}}$ high (inactive) before RCLK↑	6.7		8.5		
t_h	Hold time	SER after SRCLK↑	1.5		2		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

6.10 Timing Requirements: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range. See Figure 6-1.

			T_A = 25°C		–40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5.5		6.5		ns
		$\overline{\text{RCKR}}$ or $\overline{\text{SCRCLR}}$ low	5		6		
t_{su}	Setup time	SER before SRCLK↑	3.5		4		ns
		SRCLK↑ before RCLK↑	8		9.5		
		$\overline{\text{SCRCLR}}$ low before RCLK↑(1)	8		10		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	4.2		5.5		
		$\overline{\text{RCLK}}$ high (inactive) before RCLK↑	4.6		6		
t_h	Hold time	SER after SRCLK↑	1.5		2		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

6.11 Timing Requirements: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range. See Figure 6-1.

			T_A = 25°C		–40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5		6		ns
		$\overline{\text{RCKR}}$ or $\overline{\text{SCRCLR}}$ low	5.2		6.2		
t_{su}	Setup time	SER before SRCLK↑	3		3.5		ns
		SRCLK↑ before RCLK↑	5		6		
		$\overline{\text{SCRCLR}}$ low before RCLK↑(1)	5		5.5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2.9		4		
		$\overline{\text{RCLK}}$ high (inactive) before RCLK↑	3.2		4.5		
t_h	Hold time	SER after SRCLK↑	2		2.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

6.12 Noise Characteristics

over operating free-air temperature range (unless otherwise noted), V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C[(1)]

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(V)}$	High-level dynamic input voltage	2.31			V
$V_{IL(V)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	3.3 V	93	pF
			5 V	112	

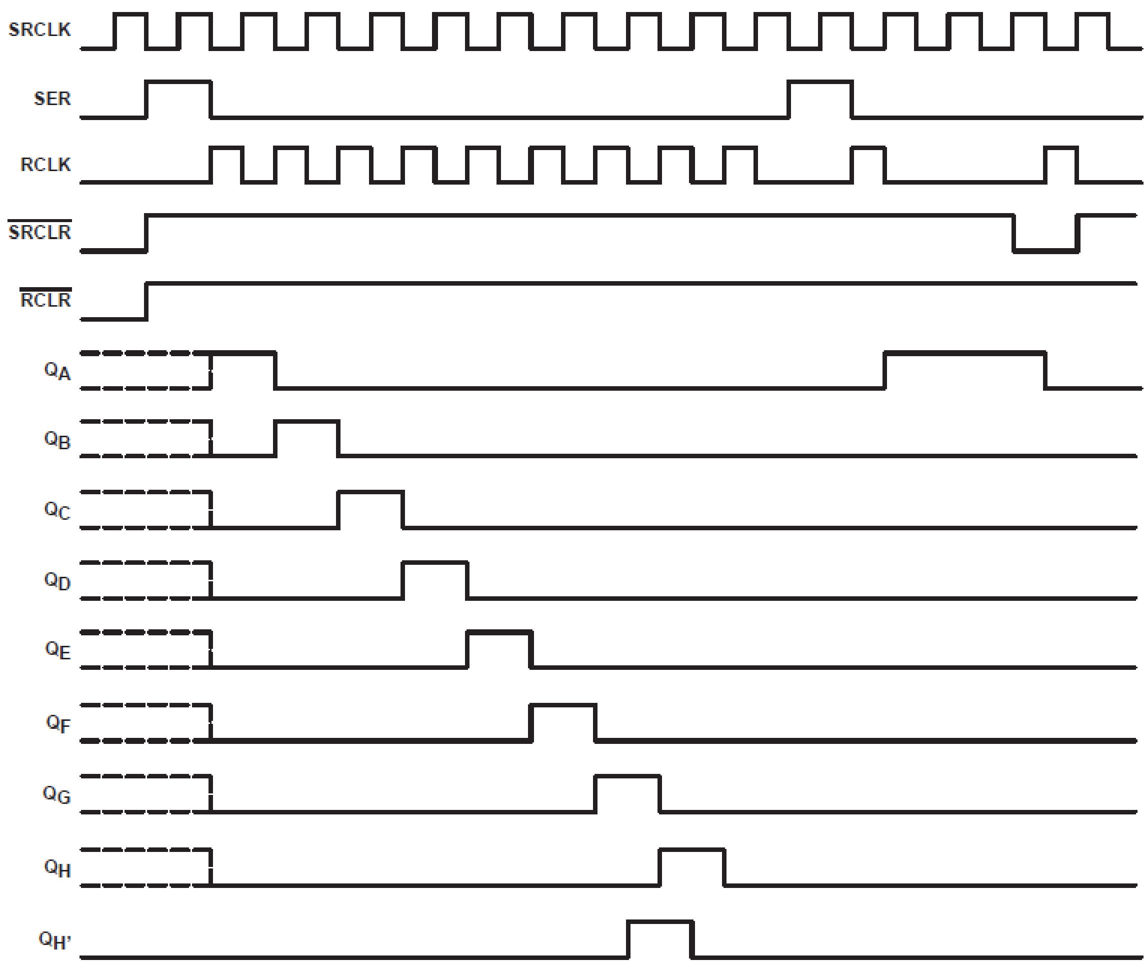


Figure 6-1. Timing Diagram

6.14 Typical Characteristics

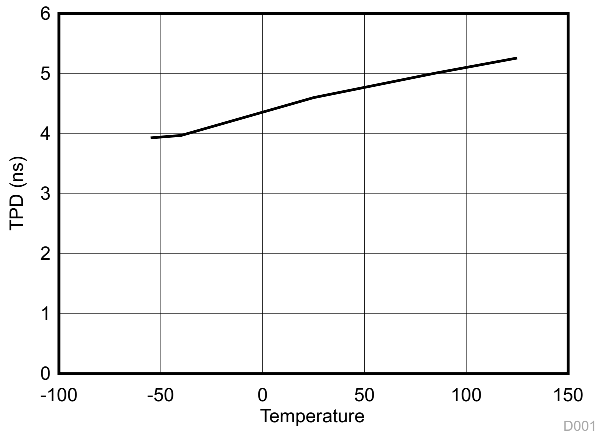


Figure 6-2. TPD vs. Temperature at 3.3 V

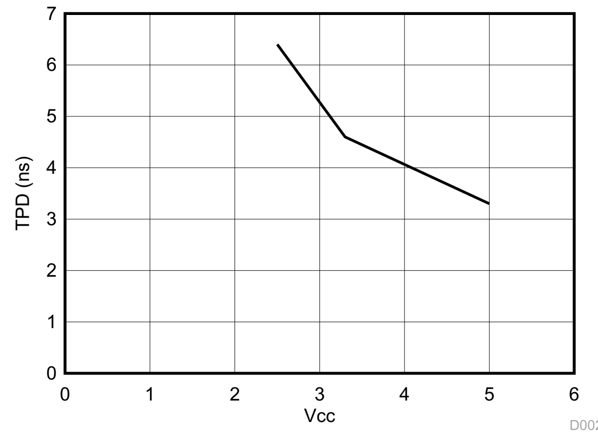
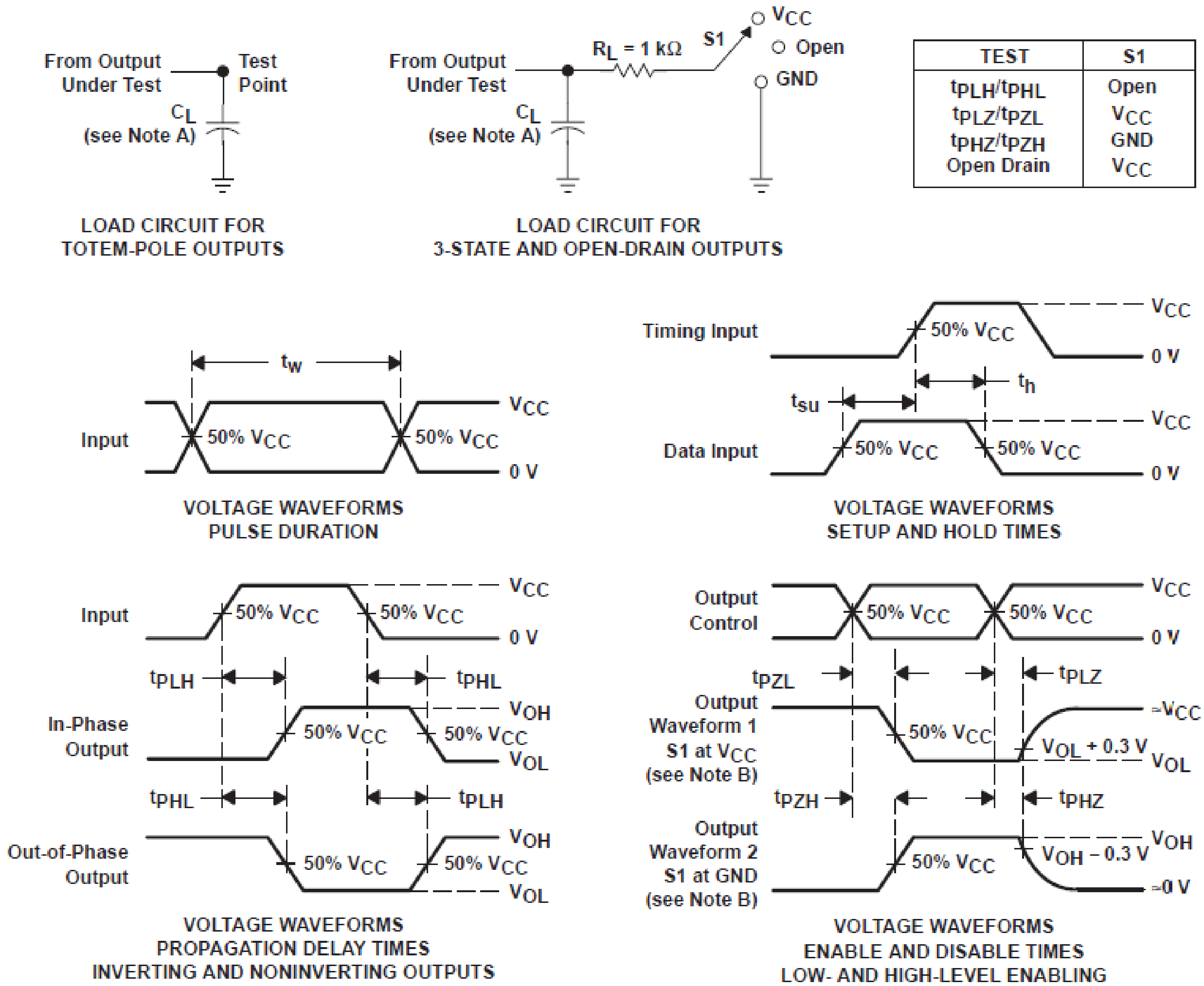


Figure 6-3. TPD vs. Vcc at 25°C

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PHL} and t_{PLH} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

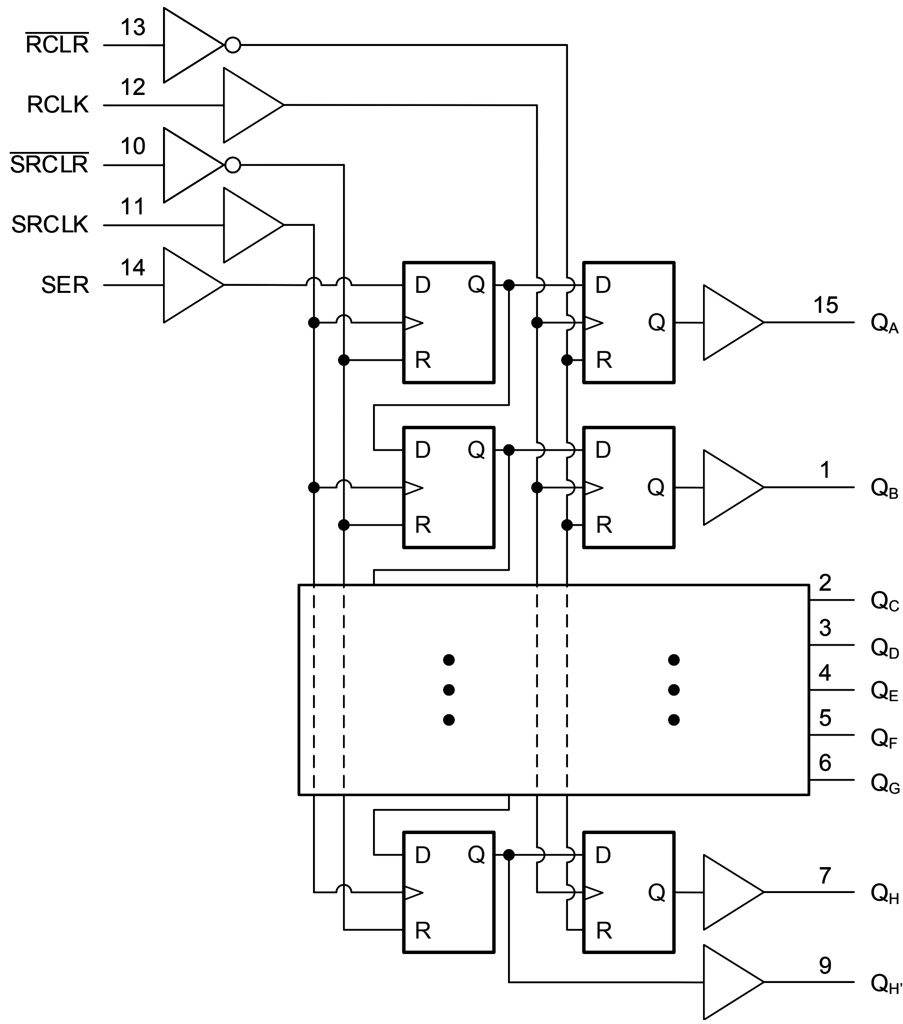
8 Detailed Description

8.1 Overview

The SN74LV594A-Q1 devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on the shift and storage registers. A serial output ($Q_{H'}$) is provided for cascading purposes. The shift-register (SRCLK) and storage-register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, then the shift register always is one clock pulse ahead of the storage register.

8.2 Functional Block Diagram



8.3 Feature Description

The device’s wide operating range allows it to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, repectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV594A-Q1 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

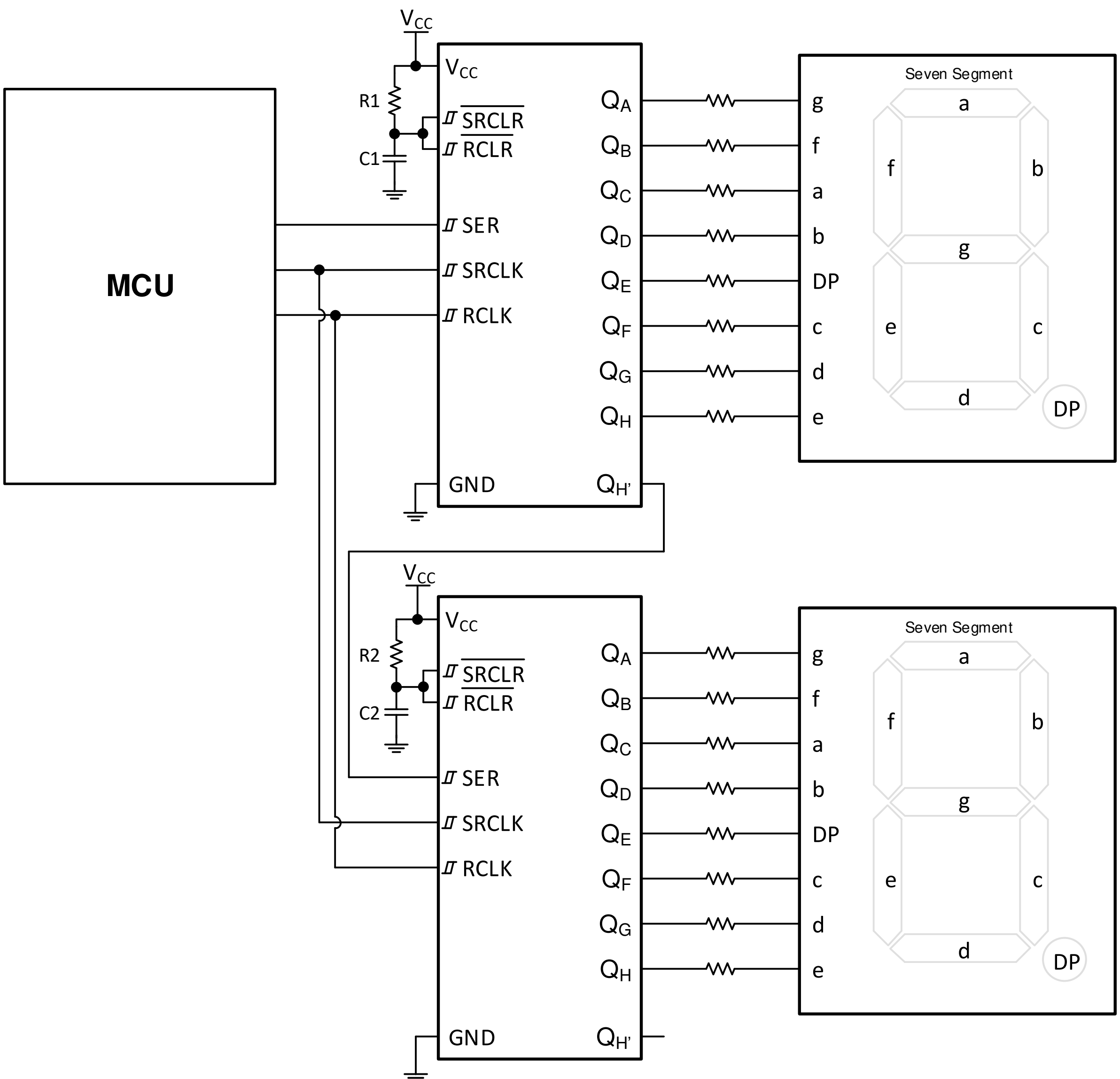


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs. See (Δt/ΔV) in *Section 6.3*.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Section 6.3*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

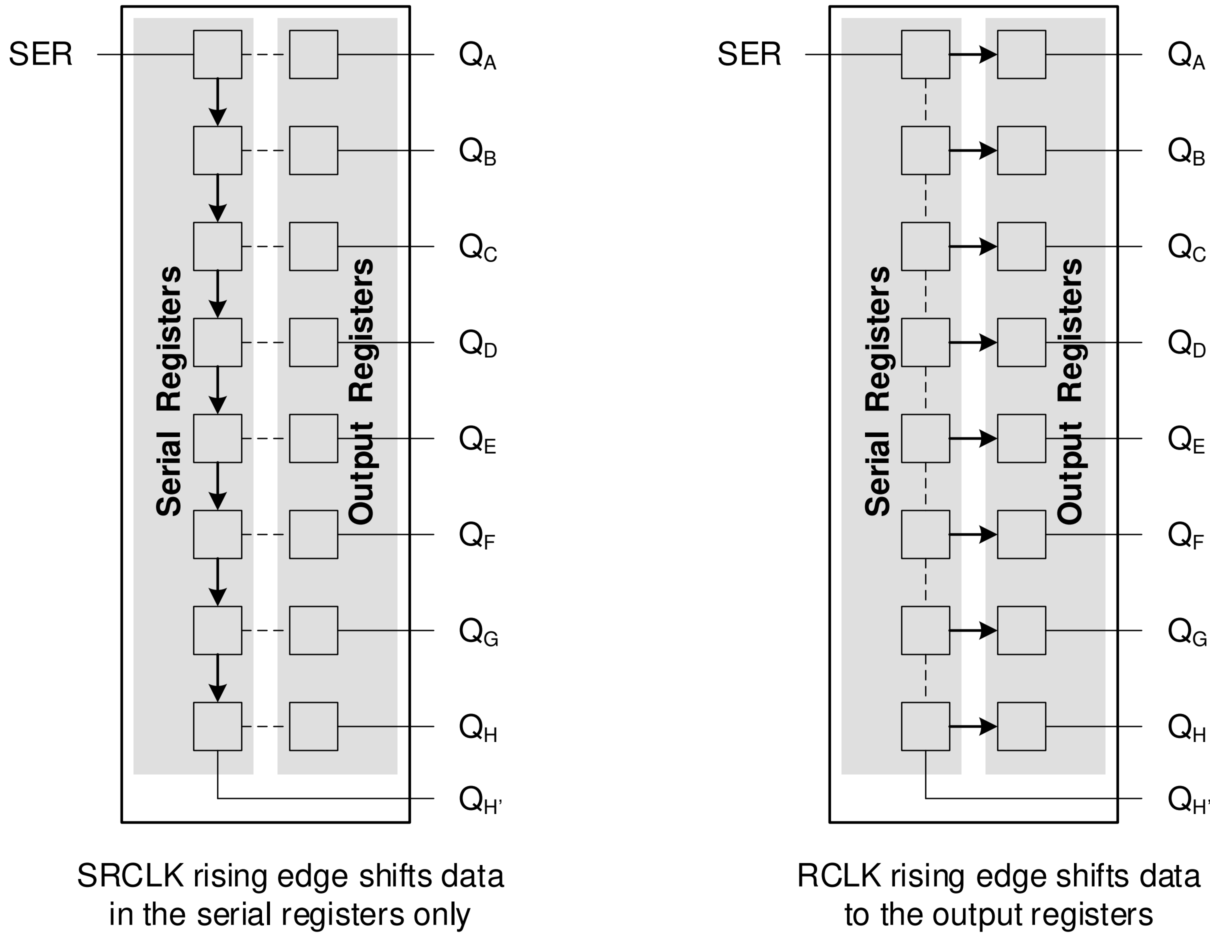


Figure 9-2. Simplified functional diagram showing clock operation

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV594AQWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV594A-Q1 :

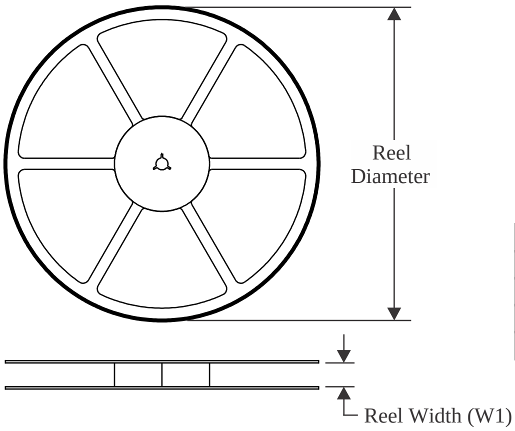
- Catalog : SN74LV594A

NOTE: Qualified Version Definitions:

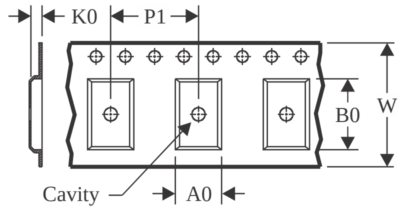
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

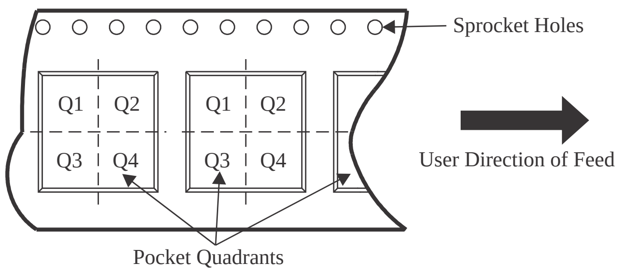


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

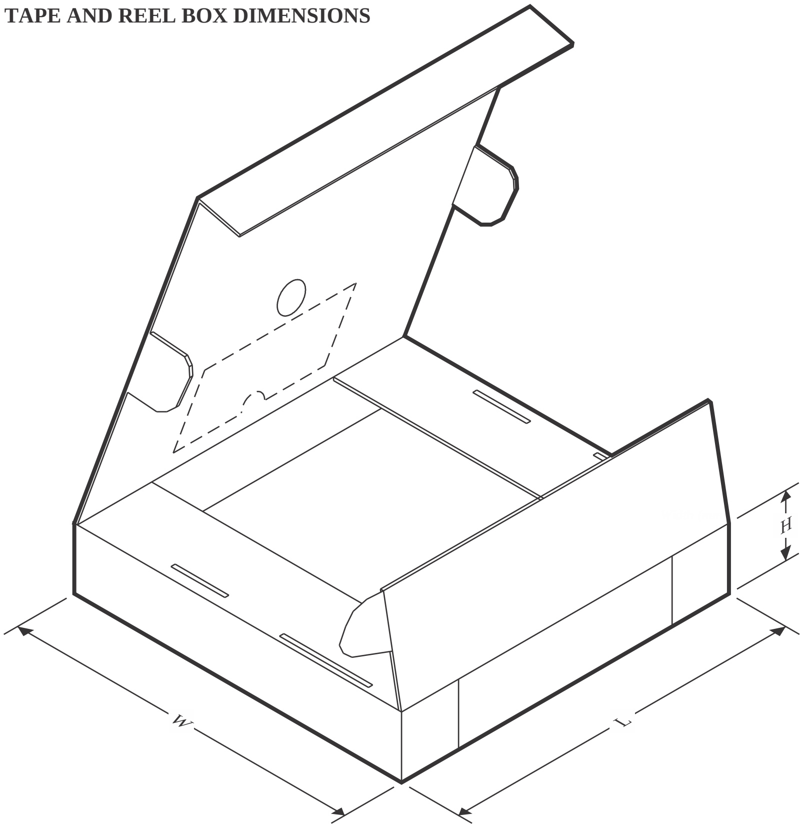
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV594AQWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV594AQWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

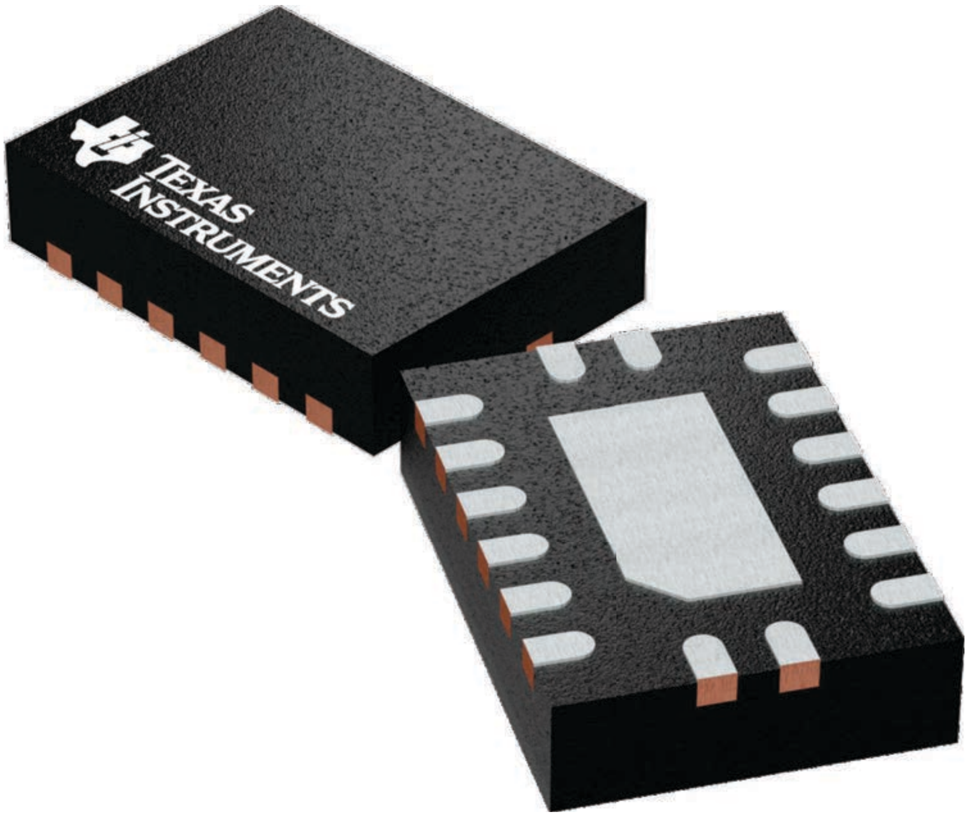
BQB 16

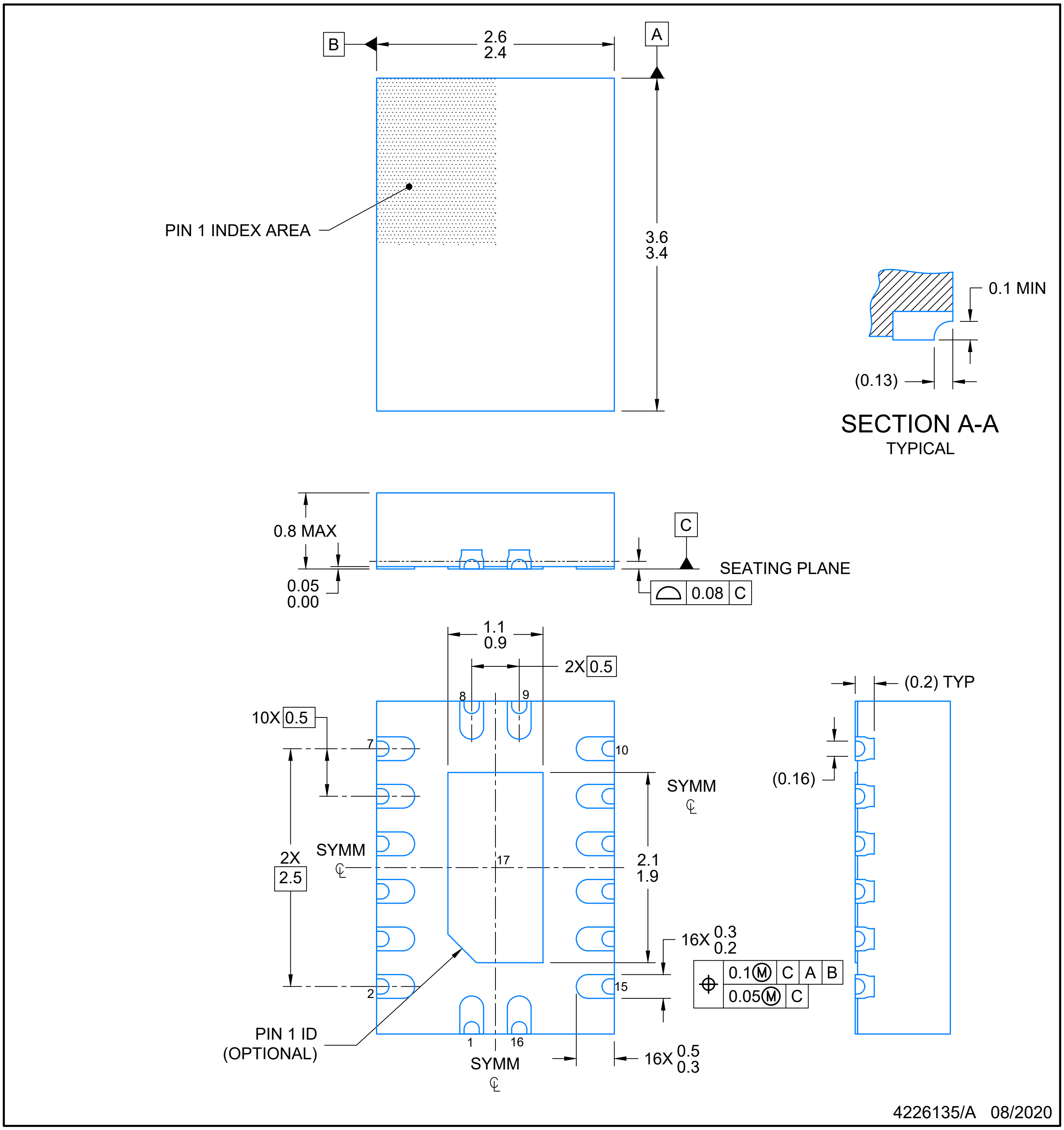
WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

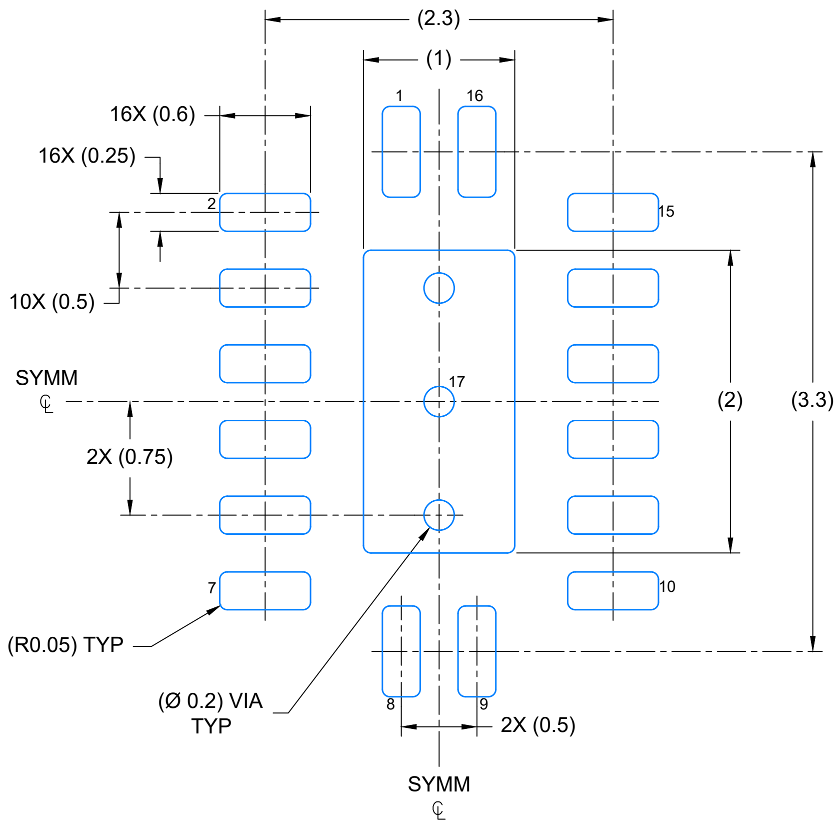
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

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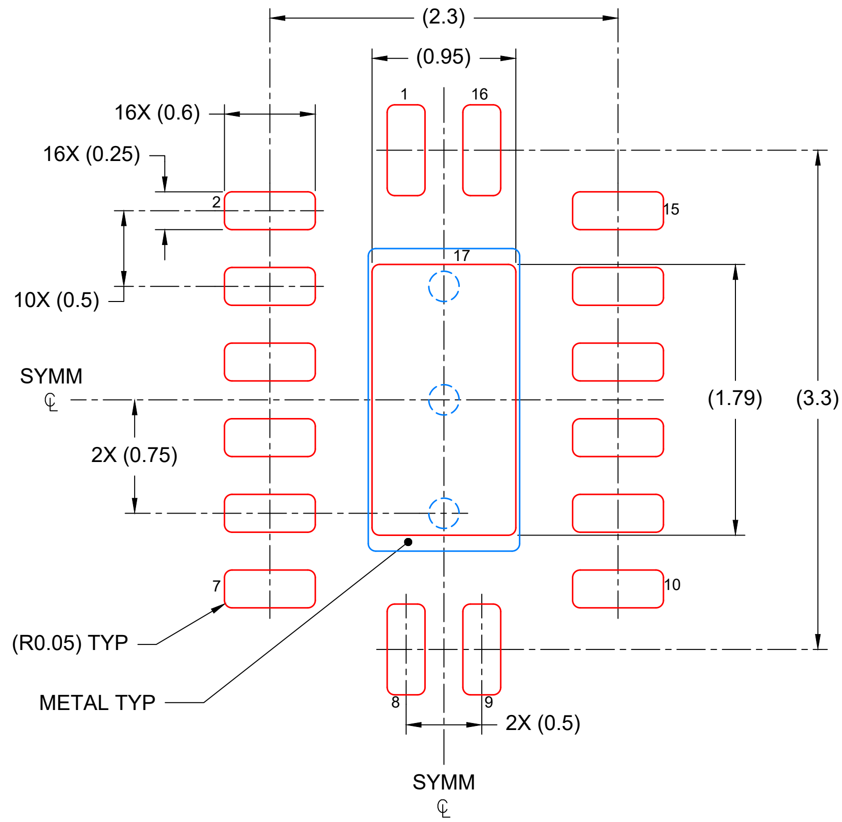
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.