

# SN74HSTL16919

## 9-BIT TO 18-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH WITH INPUT PULLUP RESISTORS

SCES348 – MARCH 2001

- Member of Texas Instruments' Widebus™ Family
- Inputs Meet JEDEC HSTL Std JESD 8-6, and Outputs Meet Level III Specifications
- 10-kΩ Pullup Resistor on Data and  $\overline{LE}$  Inputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### description

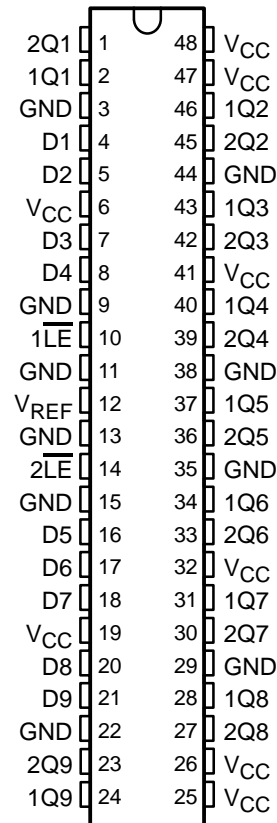
This 9-bit to 18-bit D-type latch is designed for 3.15-V to 3.45-V  $V_{CC}$  operation. The D inputs accept HSTL levels and the Q outputs provide LVTTL levels.

The SN74HSTL16919 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable ( $\overline{LE}$ ) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While  $\overline{LE}$  is low, the Q outputs of the corresponding nine latches follow the D inputs. When  $\overline{LE}$  is taken high, the Q outputs are latched at the levels set up at the D inputs.

To ensure low  $I_{CC}$  during power up or power down, 10-kΩ pullup resistors are included on the D and  $\overline{LE}$  inputs to ensure a differential voltage relative to  $V_{REF}$ .  $V_{REF}$  must be applied prior to or at the same time as  $V_{CC}$ , or  $V_{REF}$  must be pulled down to ground.

DGG PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – DGG   Tape and reel	SN74HSTL16919DGGR	HSTL16919

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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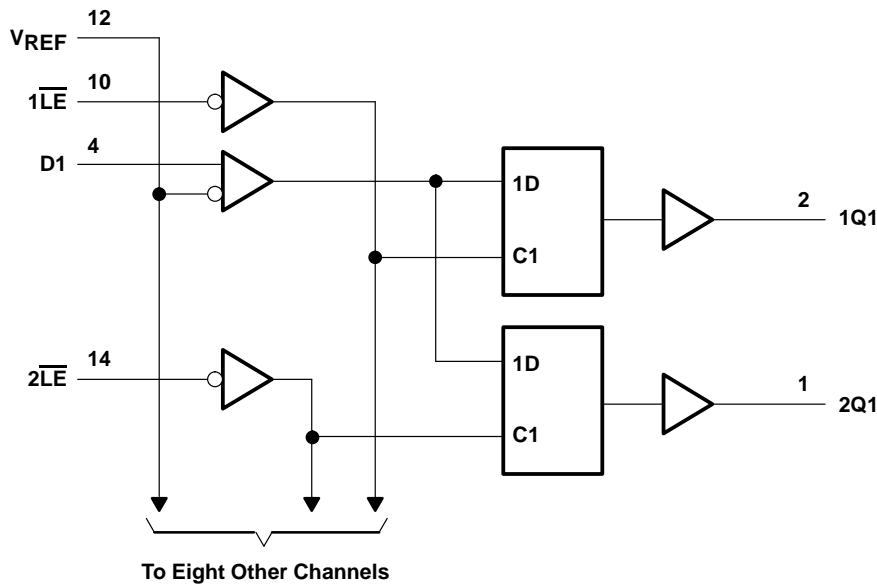
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**FUNCTION TABLE**

INPUTS		OUTPUT
LE	D	Q
L	H	H
L	L	L
H	X	Q <sub>0</sub> <sup>†</sup>

<sup>†</sup> Output level before the indicated steady-state input conditions were established

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>**

Supply voltage range, V <sub>CC</sub>	-0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	-0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Note 1)	-0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	-50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±50 mA
Continuous current through each V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	89°C/W
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3.15		3.45	V
V <sub>REF</sub>	Reference voltage	0.68	0.75	0.9	V
V <sub>I</sub>	Input voltage	0		1.5	V
V <sub>IH</sub>	AC high-level input voltage	All inputs		V <sub>REF</sub> +200 mV	V
V <sub>IL</sub>	AC low-level input voltage	All inputs		V <sub>REF</sub> -200 mV	V
V <sub>IH</sub>	DC high-level input voltage	All inputs		V <sub>REF</sub> +100 mV	V
V <sub>IL</sub>	DC low-level input voltage	All inputs		V <sub>REF</sub> -100 mV	V
I <sub>OH</sub>	High-level output current			-24	mA
I <sub>OL</sub>	Low-level output current			24	mA
T <sub>A</sub>	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must maintain a minimum differential voltage of 100 mV between data inputs and V<sub>REF</sub> to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 3.15 V,	I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 3.15 V,	I <sub>OH</sub> = -24 mA	2.4			V
V <sub>OL</sub>		V <sub>CC</sub> = 3.15 V,	I <sub>OL</sub> = 24 mA			0.5	V
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.45 V	V <sub>I</sub> = 0 or 1.5 V			-500	μA
	Data inputs		V <sub>I</sub> = 0 or 1.5 V			-500	
	V <sub>REF</sub>		V <sub>REF</sub> = 0.68 V or 0.9 V			90	
I <sub>CC</sub>		V <sub>CC</sub> = 3.45 V,	V <sub>I</sub> = 0 or 1.5 V		50	100	mA
C <sub>i</sub>	Control inputs	V <sub>CC</sub> = 0 or 3.3 V,	V <sub>I</sub> = 0 or 3.3 V		2.5		pF
	Data inputs	V <sub>CC</sub> = 0 or 3.3 V,	V <sub>I</sub> = 0 or 3.3 V		2.5		
C <sub>o</sub>	Outputs	V <sub>CC</sub> = 0,	V <sub>O</sub> = 0		2.5		pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 3.3 V ± 0.15 V		UNIT	
		MIN	MAX		
t <sub>w</sub>	Pulse duration, $\overline{LE}$ low	3		ns	
t <sub>su</sub>	Setup time, D before $\overline{LE}$ ↑	2		ns	
t <sub>h</sub>	Hold time		D after $\overline{LE}$ ↑	1	ns
t <sub>ldr</sub> ‡	Data race condition time		D after $\overline{LE}$ ↓	0	ns

‡ This is the maximum time after  $\overline{LE}$  switches low that the data input can return to the latched state from the opposite state without producing a glitch on the output.



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**switching characteristics over recommended operating free-air temperature range,  $V_{REF} = 0.75 V$**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 V$ $\pm 0.15 V$		UNIT
			MIN	MAX	
$t_{pd}$	D	Q	1.9	3.5	ns
	$\overline{LE}$		1.9	4.3	

**simultaneous switching characteristics over recommended operating free-air temperature range,  $V_{REF} = 0.75 V$ †**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 V$ $\pm 0.15 V$		UNIT
			MIN	MAX	
$t_{pd}$	D	Q	1.9	4.5	ns
	$\overline{LE}$		1.9	5.3	

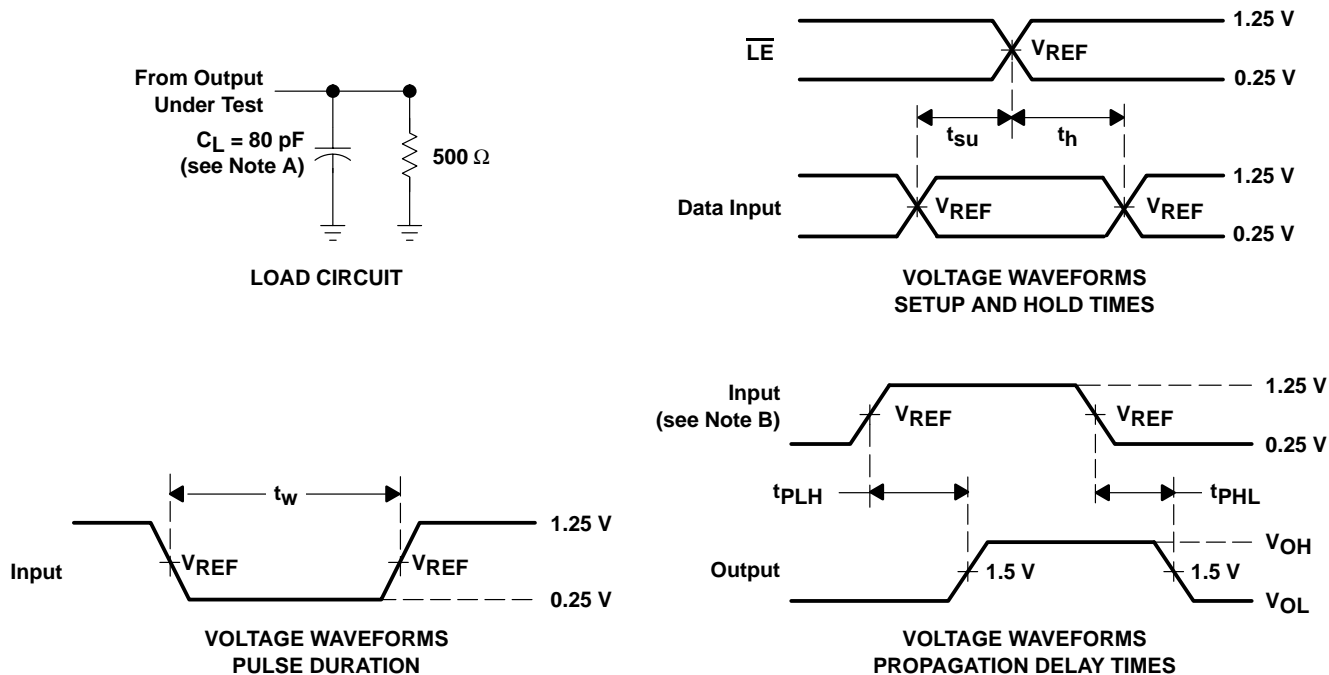
† All outputs switching.



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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 1$  ns,  $t_f \leq 1$  ns.  
 C. The outputs are measured one at a time with one transition per measurement.  
 D.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

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