

Quadruple 2-Line to 1-Line Data Select RS/Multiplexers With 3-State Outputs

1 Features

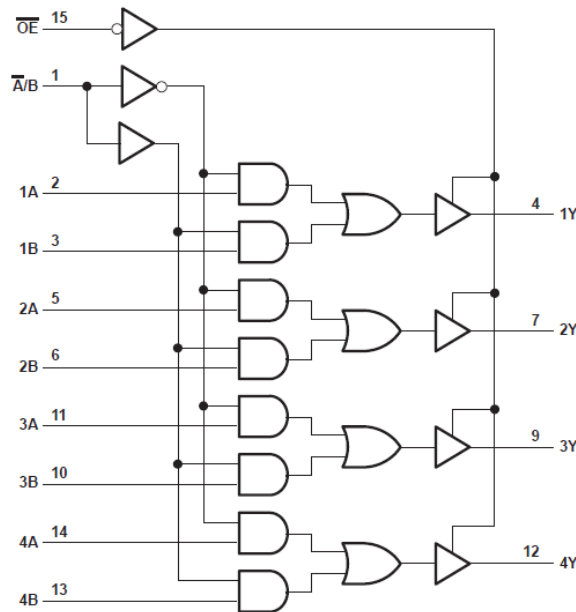
- Operating voltage range of 4.5 V to 5.5 V
- High-current 3-state outputs interface directly with system bus
- Typical $t_{pd} = 17$ ns
- Low power consumption, 80- μ A max I_{CC}
- ± 6 -mA output drive at 5 V
- Low input current of 1 μ A max
- Inputs are TTL-voltage compatible
- Provide bus interface from multiple sources in high-performance systems
- Buffered inputs and outputs

2 Description

The 'HCT257 devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems.

Device Information

ORDERABLE PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCT257	N (PDIP, 16)	19.31 mm × 6.35 mm
	D (SOIC, 16)	9.90 mm × 3.90 mm
SNJ54HCT257	J (CDIP, 16)	24.38 mm × 6.92 mm



A. Pin numbers shown are for the D, J, and N packages.

Logic Diagram (Positive Logic)

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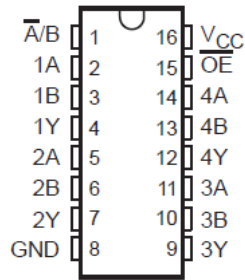
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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2003) to Revision E (July 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

4 Pin Configuration and Functions



**Figure 4-1. J, N and D Package
16-Pin CDIP, PDIP or SOIC
Top View**

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	\bar{A}/B	I	Address select
2	1A	I	Channel 1, data input A
3	1B	I	Channel 1, data input B
4	1Y	I	Channel 1, data output
5	2A	O	Channel 2, data input A
6	2B	O	Channel 2, data input B
7	2Y	I	Channel 2, data output
8	GND	—	Ground
9	3Y	I	Channel 3, data output
10	3B	I	Channel 3, data input B
11	3A	I	Channel 3, data input A
12	4Y	I	Channel 4, data output
13	4B	I	Channel 4, data input B
14	4A	I	Channel 4, data input A
15	\bar{G}	I	Output strobe, active low
16	V _{CC}	—	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}	±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±35	mA
	Continuous current through V _{CC} or GND		±70	mA
T _J	Junction Temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

		SN54HCT257			SN74HCT257			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V		2	2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V		0.8	0.8			V
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
t _t	Input transition (rise and fall) time			500	500			ns
T _A	Operating free-air temperature	-55	125		-40	85		°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		16 PINS	16 PINS	
R _{θJA}	Package thermal impedance	73	67	°C/W

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT257		SN74HCT257		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	High level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
					3.98	4.3		3.7		3.84		
V _{OL}	L Low level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5 V	0.001	0.1		0.1		0.1	V	
					0.17	0.26		0.4		0.33		

5.4 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT257		SN74HCT257		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I _I	Input leakage current	V _I = V _{CC} or 0	5.5 V	±0.1	±100		±1000	±1000	nA	
I _{oz}	Off-State (High-Impedance State) Output Current	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL}	5.5 V	±0.01	±0.5		±10	±5	μA	
I _{CC}	Supply current	V _I = V _{CC} or 0, I _O = 0	5.5 V		8		160	80	μA	
ΔI _{CC} ⁽²⁾	Supply-Current Change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V	1.4	2.4		3	2.9	mA	
C _i	Input Capacitance		4.5 V to 5.5 V	3	10		10 ⁽¹⁾	10	pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
	A̅/B	Y	4.5 V		20	30		45		38	
			5.5 V		17	27		40		34	
t _{en}	OE̅	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
t _{dis}	OE̅	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
t _t		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see [Figure 6-1](#))

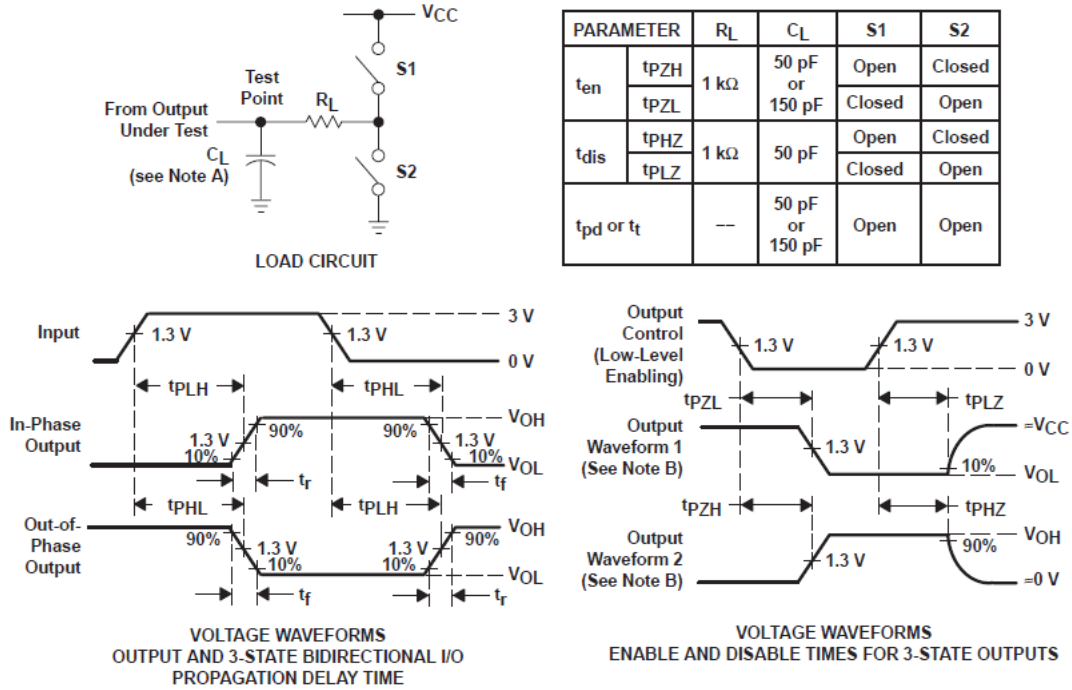
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C	T _A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.5 V		22	38		57		48	ns
			5.5 V		19	35		53		44	
	A̅/B	Y	4.5 V		22	38		57		48	
			5.5 V		19	35		53		44	
t _{en}	OE̅	Y	4.5 V		23	40		60		50	ns
			5.5 V		20	38		57		48	
t _t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

5.7 Operating Characteristics

 T_A 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	13	pF

6 Parameter Measurement Information



- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The 'HCT257 devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (\overline{OE}) input is at the high logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

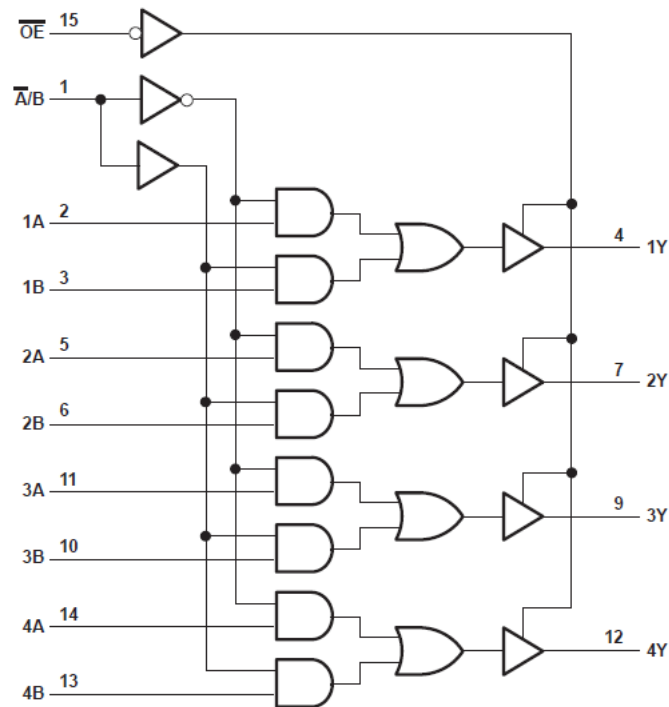


Figure 7-1. Function Diagram

8 Device Functional Modes

Table 8-1. Function Table

INPUTS ⁽¹⁾				OUTPUT ⁽²⁾ Y
OE	SELECT A/B	DATA		
		A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
 (2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

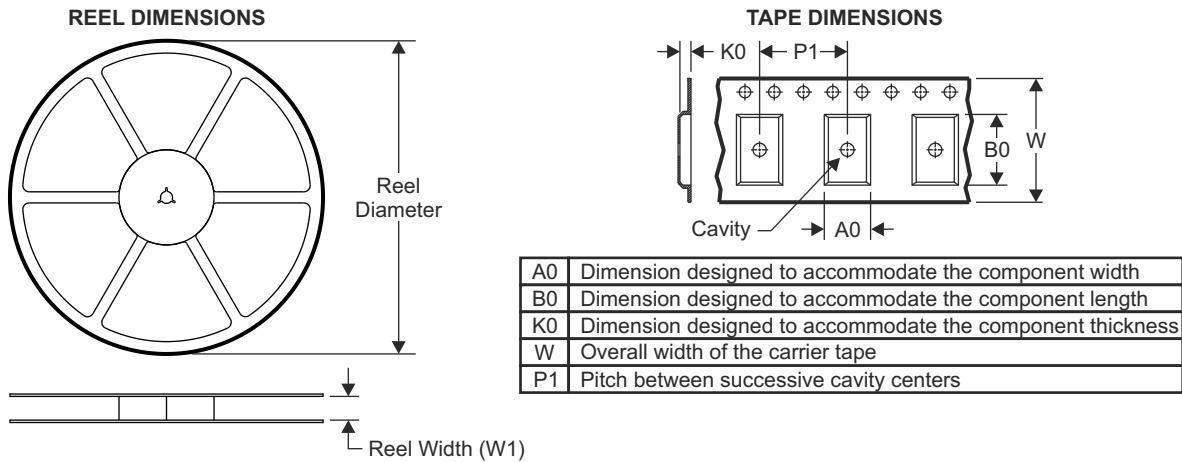
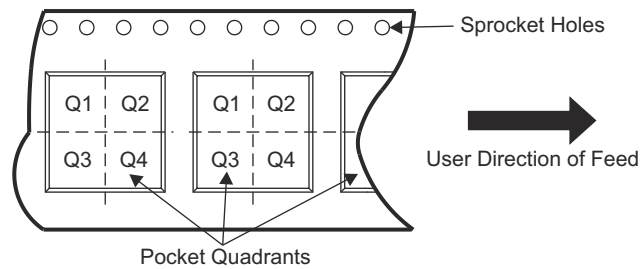
[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

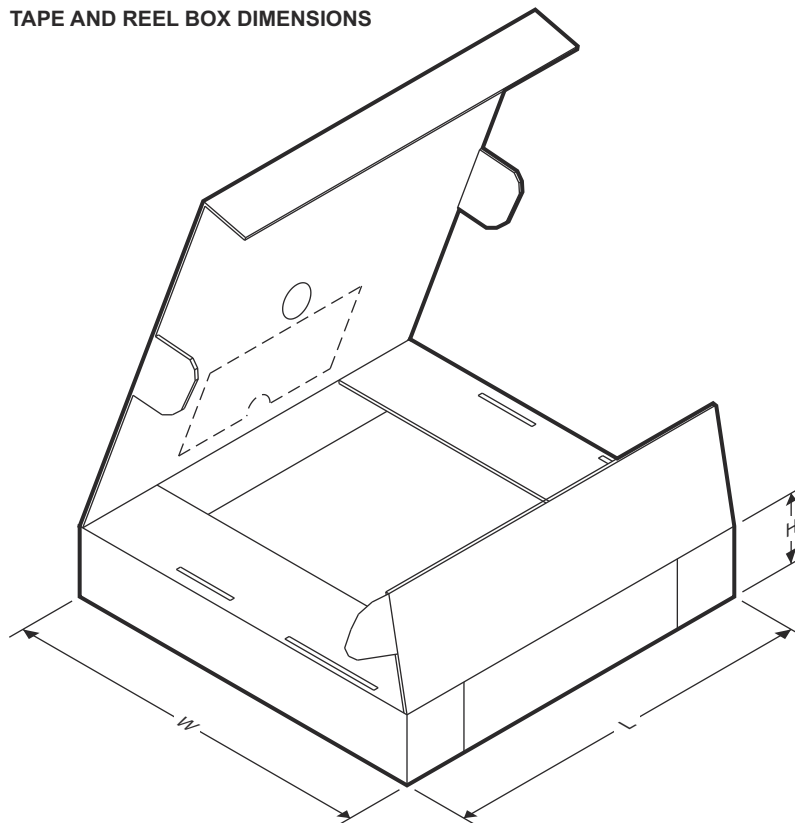
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

SN54HCT257, SN74HCT257

SCLS072E – NOVEMBER 1988 – REVISED JUNE 2023

12.1 Tape and Reel Information

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

TAPE AND REEL BOX DIMENSIONS


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
--------	--------------	-----------------	------	-----	-------------	------------	-------------

12.2 Mechanical Data

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT257DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HCT257	Samples
SN74HCT257N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT257N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT257DR	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCT257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCT257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT257DR	SOIC	D	16	2500	366.0	364.0	50.0
SN74HCT257DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HCT257DR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE


*All dimensions are nominal



Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HCT257N	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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