SN65LVDS302 Programmable 27-Bit Serial-to-Parallel Receiver

1 Features

- Serial interface technology
- Compatible with FlatLink™3G such as SN65LVDS301
- Supports video interfaces up to 24-bit RGB data and 3 control bits received over 1, 2 or 3 SubLVDS differential lines
- SubLVDS differential voltage levels
- Up to 1.755-Gbps Data Throughput
- Three operating modes to conserve power
  - Active mode QVGA: 17 mW
  - Typical shutdown: 0.7 µW
  - Typical standby mode: 27 µW Typical
- Bus-swap function for PCB-layout flexibility
- ESD rating > 4 kV (HBM)
- Pixel clock range of 4 MHz to 65 MHz
- Failsafe on all CMOS inputs
- Packaged in 5-mm × 5-mm nFBGA with 0.5-mm ball pitch
- Very low EMI meets SAE J1752/3 'Kh'-spec

2 Applications

- Wearables (non-medical)
- Tablets
- Mobile phones
- Portable electronics
- Gaming
- Retail automation & payment
- Building automation

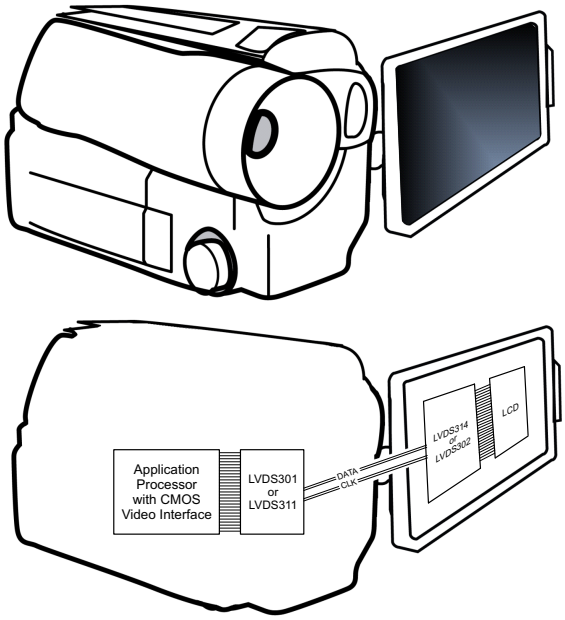
3 Description

The SN65LVDS302 receiver de-serializes FlatLink™3G compliant serial input data to 27 parallel data outputs. The SN65LVDS302 receiver contains one shift register to load 30 bits from 1, 2 or 3 serial inputs and latches the 24 pixel bits and 3 control bits out to the parallel CMOS outputs after checking the parity bit. If the parity check confirms correct parity, the Channel Parity Error (CPE) output remains low. If a parity error is detected, the CPE output generates a high pulse while the data output bus disregards the newly-received pixel. Instead, the last data word is held on the output bus for another clock cycle.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS302	nFBGA (80)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Implementation Example

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2016) to Revision E (October 2020)	Page
• NOTE: The device in the MicroStar Jr. BGA packaging were redesigned using a laminate nFBGA package. This nFBGA package offers datasheet-equivalent electrical performance. It is also footprint equivalent to the MicroStar Jr. BGA. The new package designator in place of the discontinued package designator will be updated throughout the datasheet	1
• Changed u*jr ZQE to nFBGA ZXH	1
• Changed u*jr ZQE to nFBGA ZXH	3
• Changed u*jr ZQE to nFBGA ZXH, updated thermal information	7
• Correct SN65LVDS822 to SN65LVDS302	39

Changes from Revision C (August 2012) to Revision D (May 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

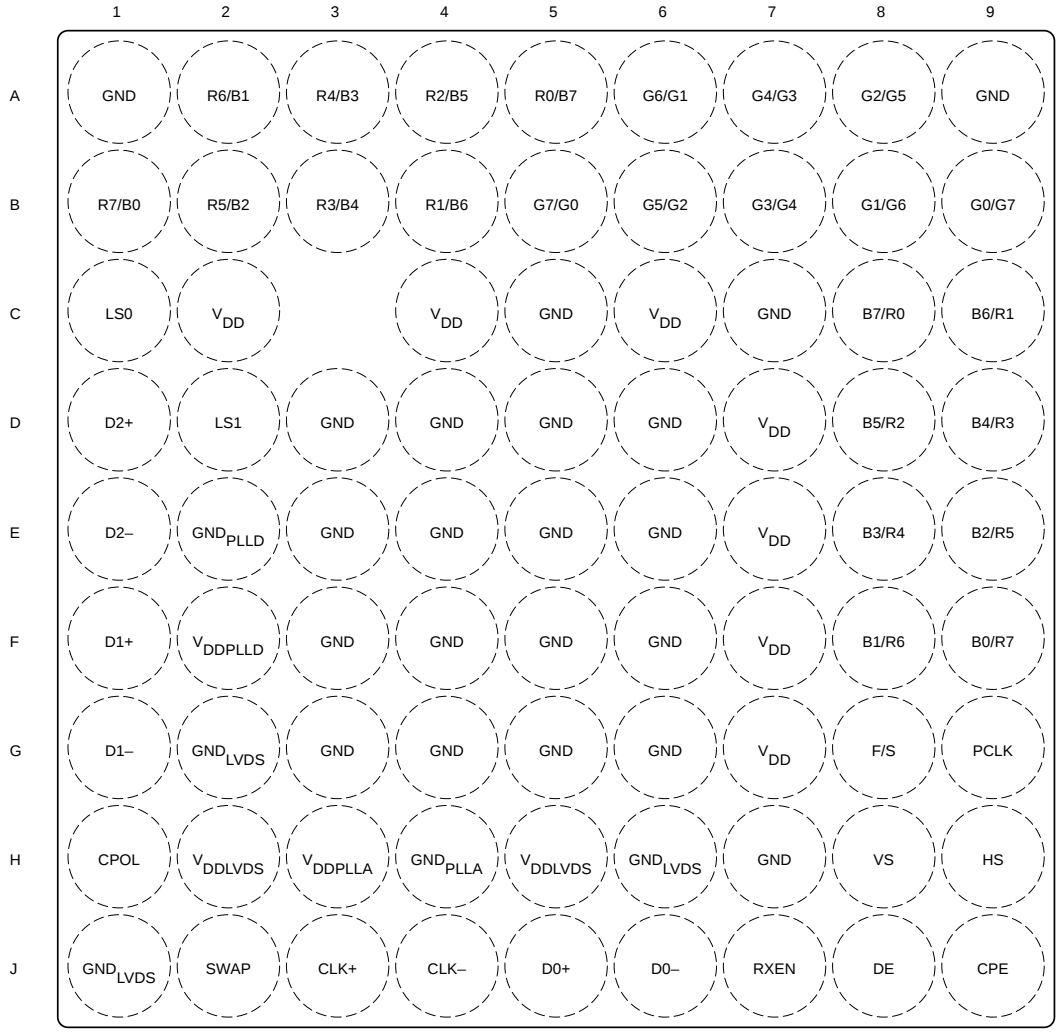


Figure 5-1. ZXH Package 80-Pin nFBGA Top View

Table 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
CMOS			
B0 to B7	See (1)	CMOS Out	Blue pixel data
G0 to G7	See (1)	CMOS Out	Green pixel data
R0 to R7	See (1)	CMOS Out	Red pixel data
CPE	J9	CMOS Out	Channel parity error This output indicates the detection of a parity error by generating an output high-pulse for half of a PCLK clock cycle; this allows counting parity errors with a simple counter. 0: no error high-pulse: bit error detected

Table 5-1. Pin Functions (continued)

PIN			DESCRIPTION
NAME	NO.	I/O	
CPOL	H1	CMOS In	Output clock polarity selection: 0: rising edge clocking 1: falling edge clocking
DE	J8	CMOS Out	Data Enable
F/S	G8	CMOS In	CMOS bus rise time select: 1: fast output rise time 0: slow output rise time
HS	H9	CMOS Out	Horizontal sync
LS0	C1	CMOS In	Link select: determines active SubLVDS Data Links and PLL Range) (see Table 8-1)
LS1	D2		
PCLK	G9	CMOS Out	Output Pixel Clock; rising or falling clock polarity is selected by control input CPOL
RXEN	J7	CMOS In	Disables the CMOS Drivers and turns off the PLL, putting device in shutdown mode.(2) 1: Receiver enabled 0: Receiver disabled (shutdown)
SWAP	J2	CMOS In	Bus swap: swaps the bus pins to allow device placement on top or bottom of PCB. See pinout drawing and Table 5-2 for pin assignments. 0: data output from R7 to B0 1: data output from B0 to R7
VS	H8	CMOS Out	Vertical sync
SUBLVDS			
CLK+, CLK–	J3, J4	SubLVDS In	SubLVDS input pixel clock (polarity is fixed)
D0+, D0–	J5, J6	SubLVDS In	SubLVDS data link (active during normal operation)
D1+, D1–	F1, G1	SubLVDS In	SubLVDS data link (active during normal operation when LS0 = high and LS1 = low, or LS0 = low and LS1 = high; high impedance if LS0 = LS1 = low); input can be left open if unused.
D2+, D2–	D1, E1	SubLVDS In	SubLVDS data link (active during normal operation when LS0 = low and LS1 = high, high-impedance when LS1 = low); input can be left open if unused.
POWER SUPPLY			
V_{DD}	C2, C4, C6, D7 to G7	Power Supply	Supply voltage
V_{DDLVDS}	H2, H5	Power Supply	SubLVDS I/O supply voltage
V_{DDPLLA}	H3	Power Supply	PLL analog supply voltage
V_{DDPLLD}	F2	Power Supply	PLL digital supply voltage
GND	A1, A9, C5, C7, D3 to D6, E3 to E6, F3 to F6, G3 to G6, H7	Ground	Supply ground
GND_{LVDS}	G2, H6, J1	Ground	SubLVDS ground
GND_{PLLA}	H4	Ground	PLL analog ground

Table 5-1. Pin Functions (continued)

PIN			DESCRIPTION
NAME	NO.	I/O	
GND_{PLLD}	E2	Ground	PLL digital ground

(1) Pin assignment depends on SWAP pin setting. Swappable pins are detailed in Table 5-2.

(2) RXEN input incorporates glitch suppression logic to avoid unwanted switching. The input must be pulled low for longer than 10 µs continuously to force the receiver to enter Shutdown. The input must be pulled high for at least 10 µs continuously to activate the receiver. An input pulse shorter than 5 µs is interpreted as glitch and becomes ignored. At power up, the receiver is enabled immediately if RXEN = H and disabled if RXEN = L.

Table 5-2. Swappable Pins

SIGNAL	SWAP(1)	PIN	SIGNAL	SWAP(1)	PIN	SIGNAL	SWAP(1)	PIN
B0	L	F9	G0	L	B9	R0	L	A5
	H	B1		H	B5		H	C8
B1	L	F8	G1	L	B8	R1	L	B4
	H	A2		H	A6		H	C9
B2	L	E9	G2	L	A8	R2	L	A4
	H	B2		H	B6		H	D8
B3	L	E8	G3	L	B7	R3	L	B3
	H	A3		H	A7		H	D9
B4	L	D9	G4	L	A7	R4	L	A3
	H	B3		H	B7		H	E8
B5	L	D8	G5	L	B6	R5	L	B2
	H	A4		H	A8		H	E9
B6	L	C9	G6	L	A6	R6	L	A2
	H	B4		H	B8		H	F8
B7	L	C8	G7	L	B5	R7	L	B1
	H	A5		H	B9		H	F9

(1) The SWAP pin is either set to GND (L) or V_{DD} (H).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{DD} (2), V_{DDPLLA}, V_{DDPLLD}, V_{DDLVDS}	–0.3	2.175	V
Voltage range at any input or output terminal	When VDDx > 0 V	–0.5	2.175	V
	When VDDx ≤ 0 V	–0.5	V_{DD} + 2.175	
Ouput current, I_O		±5		mA
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the GND terminals

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (1)

			MIN	NOM	MAX	UNIT
V_{DD} V_{DDPLLA} V_{DDPLLD} V_{DDLVDS}	Supply voltages		1.65	1.8	1.95	V
$V_{DDn(PP)}$	Supply voltage noise magnitude 50 MHz (all supplies)	Test set-up see Figure 7-1				mV
		f_{CLK} ≤ 50 MHz; f(noise) = 1 Hz to 2 GHz			100	
		f_{CLK} > 50 MHz; f(noise) = 1 Hz to 1 MHz			100	
		f_{CLK} > 50 MHz; f(noise) > 1 MHz			40	
T_A	Operating free-air temperature		–40		85	°C
CLK+ and CLK–						
$f_{CLK±}$	Input Pixel clock frequency	1-Channel receive mode, see Figure 8-4	4		15	MHz
		2-Channel receive mode, see Figure 8-5	8		30	
		3-Channel receive mode, see Figure 8-6	20		65	
		Standby mode(2), see Figure 7-10			500	kHz
t_{DUTCLK}	CLK Input Duty Cycle		35%		65%	

see (1)

			MIN	NOM	MAX	UNIT
D0+, D0–, D1+, D1–, D2+, D2–, CLK+, and CLK–						
$\|V_{ID}\|$	Magnitude of differential input voltage	$\|V_{D0+} - V_{D0-}\|$, $\|V_{D1+} - V_{D1-}\|$, $\|V_{D2+} - V_{D2-}\|$, $\|V_{CLK+} - V_{CLK-}\|$ during normal operation	70		200	mV
V_{ICM}	Input voltage common mode range	Receive or Acquire mode	0.6		1.2	V
		Stand-by mode	0.9 × V_{DDLVDS}			
ΔV_{ICM}	Input voltage common mode variation between all SubLVDS inputs	$V_{ICM(n)} - V_{ICM(m)}$ with n = {D0, D1, D2, or CLK} and m = {D0, D1, D2, or CLK}	–100		100	mV
ΔV_{ID}	Differential input voltage amplitude variation between all SubLVDS inputs	$V_{ID(n)} - V_{ID(m)}$ with n = {D0, D1, D2, or CLK} and m = {D0, D1, D2, or CLK}	–10%		10%	
$t_{R/F}$	Input rise and fall time	RXEN at VDD; see figure 10			800	ps
$\Delta t_{R/F}$	Input rise or fall time mismatch between all SubLVDS inputs	$t_{R(n)} - t_{R(m)}$ and $t_{F(n)} - t_{F(m)}$ with n = {D0, D1, D2, or CLK} and m = {D0, D1, D2, or CLK}	–100		100	ps
LS0, LS1, CPOL, SWAP, RXEN, F/S						
V_{ICMOSH}	High-level input voltage		0.7 × V_{DD}		V_{DD}	V
V_{ICMOSL}	Low-level input voltage		0		0.3 × V_{DD}	V
t_{inRXEN}	RXEN input pulse duration		10			µs
R[7:0], G[7:0], B[7:0], VS, HS, PCLK, CPE						
C_L	Output load capacitance			10		pF

(1) Unused single-ended inputs must be held high or low to prevent them from floating.

(2) PCLK input frequencies lower than 500 kHz forces the SN65LVDS302 into standby mode. Input frequencies from 500 kHz to 3 MHz may or may not activate the SN65LVDS302. Input frequencies beyond 3 MHz activate the SN65LVDS302. TI recommends against input frequencies from 500 kHz to 4 MHz, which can cause PLL malfunction.

6.4 Thermal Information

THERMAL METRIC(1)		SN65LVDS302 ZXH (nFBGA) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
I_{DD}	RMS supply current	1ChM	Alternating 1010 Test pattern (see Table 7-5). All CMOS outputs terminated with 10 pF, F/S and RXEN at V_{DD}. $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, $V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$	f_{PCLK} = 4 MHz		9.8	14	mA
				f_{PCLK} = 6 MHz		11.7	15.9	
				f_{PCLK} = 15 MHz		19.3	25	
			Typical power test pattern (see Table 7-2). V_{ID} = 70 mV. All CMOS outputs terminated with 10 pF, F/S at GND, and RXEN at V_{DD}. $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, $V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$	f_{PCLK} = 4 MHz		4.7		mA
				f_{PCLK} = 6 MHz		6		
				f_{PCLK} = 15 MHz		13.2		
		2ChM	Alternating 1010 Test pattern (see Table 7-5). All CMOS outputs terminated with 10 pF, F/S and RXEN at V_{DD}. $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, $V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$	f_{PCLK} = 8 MHz		14.3	19.4	mA
				f_{PCLK} = 22 MHz		25	33	
				f_{PCLK} = 30 MHz		26.8	37	
			Typical power test pattern (see Table 7-3). V_{ID} = 70 mV. All CMOS outputs terminated with 10 pF, F/S at GND, and RXEN at V_{DD}. $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, $V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$	f_{PCLK} = 8 MHz		6.4		mA
				f_{PCLK} = 22 MHz		13.7		
				f_{PCLK} = 30 MHz		18.3		
		3ChM	Alternating 1010 Test pattern (see Table 7-5). All CMOS outputs terminated with 10 pF, F/S and RXEN at V_{DD}. $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, $V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$	f_{PCLK} = 20 MHz		17.1	27	mA
				f_{PCLK} = 65 MHz		60.8	68	
			Typical power test pattern (see Table 7-4). V_{ID} = 70 mV. All CMOS outputs terminated with 10 pF, F/S at GND, and RXEN at V_{DD}. $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, $V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$	f_{PCLK} = 20 MHz		8.6		mA
				f_{PCLK} = 65 MHz		22.2		
		CLK and D[0:2] inputs are left open. All control inputs held static high or low. All CMOS outputs terminated with 10 pF. $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, $V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$		Standby mode; RXEN = V_{IH}		15	100	µA
				Shutdown mode; RXEN = V_{IL}		0.4	10	µA

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.

6.6 Input Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
D0+, D0–, D1+, D1–, D2+, D2–, CLK+, and CLK–						
V_{thstby}	Input voltage common mode threshold to switch between receive and acquire mode and standby mode	RXEN at V_{DD}	1.3		0.9 × V_{DDLVDS}	V
V_{THL}	Low-level differential input voltage threshold	$V_{D0+} – V_{D0–}$, $V_{D1+} – V_{D1–}$, $V_{D2+} – V_{D2–}$, $V_{CLK+} – V_{CLK–}$	–40			mV
V_{THH}	High-level differential input voltage threshold	$V_{D0+} – V_{D0–}$, $V_{D1+} – V_{D1–}$, $V_{D2+} – V_{D2–}$, $V_{CLK+} – V_{CLK–}$			40	mV
I_{I+}, $I_{I–}$	Input leakage current	V_{DD} = 1.95 V, $V_{I+} = V_{I–}$, V_I = 0.4 V and V_I = 1.5 V			75	µA
I_{IOFF}	Power-off input current	V_{DD} = GND; V_I = 1.5 V			–75	µA
R_{ID}	Differential input termination resistor value		78	100	122	Ω
C_{IN}	Input capacitance	Measured between input terminal and GND		1		pF
ΔC_{IN}	Input capacitance variation	Within one signal pair			0.2	pF
		Between all signals			1	
R_{BBDC}	Pull-up resistor for standby detection		21	30	39	kΩ
LS0, LS1, CPOL, SWAP, RXEN, F/S						
V_{IK}	Input clamp voltage	I_I = –18 mA, V_{DD} = V_{DD}(min)			–1.2	V
I_{ICMOS}	Input current(2)	0 V ≤ V_{DD} ≤ 1.95 V; V_I = {GND, 1.95 V}			100	nA
C_{IN}	Input capacitance			2		pF
I_{IH}	High-level input current	V_{IN} = 0.7 × V_{DD}	–200		200	nA
I_{IL}	Low-level input current	V_{IN} = 0.3 × V_{DD}	–200		200	nA
V_{IH}	High-level input voltage		0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{DD}	V

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.
(2) Do not leave any CMOS Input unconnected or floating to minimize leakage currents. Every input must be connected to a valid logic level V_{IH} or V_{OL} while power is supplied to V_{DD}.

6.7 Output Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R[0:7], G[0:7], B[0:7], VS, HS, PCLK, CPE						
V_{OH}	High-level output current	1-ChM, F/S = L, I_{OH} = –250 µA	0.8 × V_{DD}		V_{DD}	V
		2- or 3-ChM, F/S = L, I_{OH} = –500 µA				
		1-ChM, F/S = H, I_{OH} = –500 µA				
		2- or 3-ChM, F/S = H, I_{OH} = –2 mA				
V_{OL}	Low-level output current	1-ChM, F/S = L, I_{OL} = 250 µA	0		0.2 × V_{DD}	V
		2- or 3-ChM, F/S = L, I_{OL} = 500 µA				
		1-ChM, F/S = H, I_{OL} = 500 µA				
		2- or 3-ChM, F/S = H, I_{OL} = 2 mA				
I_{OH}	High-level output current	1-ChM, F/S = L	–250			µA
		2- or 3-ChM, F/S = L; 1-ChM, F/S = H	–500			
		2- or 3-ChM, F/S = H	–2000			

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current	1-ChM, F/S = L			250	µA
		2- or 3-ChM, F/S = L; 1-ChM, F/S = H			500	
		2- or 3-ChM, F/S = H			2000	

6.8 Timing Requirements

PARAMETER		TEST CONDITIONS		MIN	UNIT
t_{RSKMx} (2) (3)	Receiver input skew margin(1) (see Figure 9-2)	1ChM: x = 0.29, f_{PCLK} = 15 MHz, RXEN at V_{DD}, V_{IH} = V_{DD}, V_{IL} = GND, R_L = 100 Ω, test setup as in Figure 7-2, test pattern as in Table 7-7	f_{CLK} = 15 MHz(4)	630	ps
			f_{CLK} = 4 MHz to 15 MHz(5)	1 / (60 × f_{CLK}) – 480	
		2ChM: x = 0.14, f_{PCLK} = 30 MHz, RXEN at V_{DD}, V_{IH} = V_{DD}, V_{IL} = GND, R_L = 100 Ω, test setup as in Figure 7-2, test pattern as in Table 7-8	f_{CLK} = 30 MHz(4)	630	
			f_{CLK} = 8 MHz to 30 MHz(5)	1 / (30 × f_{CLK}) – 480	
		3ChM: RXEN at V_{DD}, V_{IH} = V_{DD}, V_{IL} = GND, test setup as in Figure 7-2, test pattern as in Table 7-9	f_{CLK} = 65 MHz(4)	360	
			f_{CLK} = 20 MHz to 65 MHz(5)	1 / (20 × f_{CLK}) – 410	

(1) This includes the receiver internal set-up and hold time uncertainty, all PLL related high-frequency random and deterministic jitter components that impact the jitter budget, ISI and duty cycle distortion from the front end receiver, and the skew from CLK to data D0, D1, and D2; The pulse position minimum and maximum variation is given with a bit error rate target of 10^{-12}; Measurements of the total jitter are taken over a sample amount of > 10^{-12} samples.

(2) Receiver Input Skew Margin (t_{RSKM}) is the timing margin available for transmitter output pulse position (t_{PPOS}), interconnect skew, and interconnect inter-symbol interference. tRSKM represents the reminder of the serial bit time not taken up by the receiver strobe uncertainty;. The t_{RSKM} assumes a bit error rate better than 10^{-12}.

(3) t_{RSKM} is indirectly proportional to the internal set-up and hold time uncertainty, ISI and duty cycle distortion from the front end receiver, the skew mismatch from CLK to data D0, D1, and D2, as well as the PLL cycle-to-cycle jitter.

(4) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temp ranges.

(5) These Minimum and Maximum Limits are simulated only.

6.9 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
D0+, D0–, D1+, D1–, D2+, D2–, CLK+, and CLK–							
$t_{R/F}$	Input rise and fall time	RXEN at V_{DD}; see Figure 7-4				800	ps
$\Delta t_{R/F}$	Input rise or fall time mismatch between all SubLVDS inputs	t_R(n) – t_R(m) and t_F(n) – t_F(m) with n = {D0, D1, D2, or CLK} and m = {D0, D1, D2, or CLK}		–100		100	ps
R[7:0], G[7:0], B[7:0], VS, HS, PCLK, CPE							
$t_{R/F}$	Rise and fall time 20% to 80% of V_{DD} (2)	C_L = 10 pF(3) (see Figure 7-3)	1-channel mode, F/S = L	8		16	ns
			2-channel mode, F/S = L	4		8	
			3-channel mode, F/S = L	4		8	
			1-channel mode, F/S = H	4		8	
			2-channel mode, F/S = H	1		2	
			3-channel mode, F/S = H	1		2	
t_{OUTP}	PCLK output duty cycle	1-channel and 3-channel mode		45%	50%	55%	
		CPOL = V_{IL}, 2-channel mode		48%	53%	59%	
		CPOL = V_{IH}, 2-channel mode		41%	47%	52%	
t_{OSK}	Output skew from PCLK to R[0:7], G[0:7], B0:7], HS, VS, and DE	see Figure 7-3		–500		500	ps
INPUT TO OUTPUT RESPONSE TIME							

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$t_{PD(L)}$	Propagation delay time from CLK+ input to PCLK output	RXEN at V_{DD}, V_{IH} = V_{DD}, V_{IL} = GND, C_L = 10 pF, see Figure 7-8		1.4 / f_{PCLK}	1.9 / f_{PCLK}	2.5 / f_{PCLK}	s
t_{GS}	RXEN glitch suppression pulse width(4)	V_{IH} = V_{DD}, V_{IL} = GND, RXEN toggles from V_{IL} to V_{IH}; see Figure 7-9 and Figure 7-10				3.8	µs
t_{pwrup}	Enable time from power down (↑RXEN)	Time from RXEN pulled high to data outputs enabled and outputs valid data; see Figure 7-10				2	ms
t_{pwrdn}	Disable time from active mode (↓RXEN)	RXEN is pulled low during receive mode; time measurement until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high, DE = PCLK = low and PLL is Shutdown; see Figure 7-10				11	µs
t_{wakeup}	Enable time from Standby (↑↓CLK)	RXEN at V_{DD}; device is in standby; time measurement from CLK input starts switching to PCLK and data outputs enabled and outputting valid data; see Figure 7-11				2	ms
t_{sleep}	Disable time from active mode (CLK transitions to high-impedance)	RXEN at V_{DD}; device is receiving data; time measurement from CLK input signal stops (input open or input common mode VICM exceeds threshold voltage V_{thstby}) until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high, DE = PCLK = low and PLL is Shutdown; see Figure 7-11				3	µs
f_{BW}	PLL bandwidth(5)	Tested from CLK input to PCLK output	2-ChM; f_{PCLK} = 22 MHz	0.087 × f_{PCLK}			MHz
			3-ChM; f_{PCLK} = 65 MHz	0.075 × f_{PCLK}			

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.

(2) $t_{R/F}$ depends on the F/S setting and the capacitive load connected to each output. Some application information of how to calculate $t_{R/F}$ based on the output load and how to estimate the timing budget to interconnect to an LCD driver are provided in the application section near the end of this data sheet.

(3) The output rise and fall time is optimized for an output load of 10 pF. The rise and fall time can be adjusted by changing the output load capacitance.

(4) The RXEN input incorporates a glitch-suppression logic to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.

(5) When using the SN65LVDS302 receiver in conjunction with the SN65LVDS301 transmitter in one link, the PLL bandwidth of the SN65LVDS302 receiver always exceed the bandwidth of the SN65LVDS301 transmit PLL. This ensures stable PLL tracking under all operating conditions and maximizes the receiver skew margin.

6.10 Device Power Dissipation

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
P_D	Device Power Dissipation	V_{DDx} = 1.8 V, T_A = 25°C, all outputs terminated with 10 pF	f_{CLK} = 4 MHz	16.8		mW
			f_{CLK} = 65 MHz	64.7		
		V_{DDx} = 1.95 V, T_A = –40°C, all outputs terminated with 10 pF	f_{CLK} = 4 MHz		27.4	mW
			f_{CLK} = 65 MHz		128.8	

Typical Characteristics

Some of the plots in this section show more than one curve representing various device pin relationships. Taken together, they represent a working range for the tested parameter.

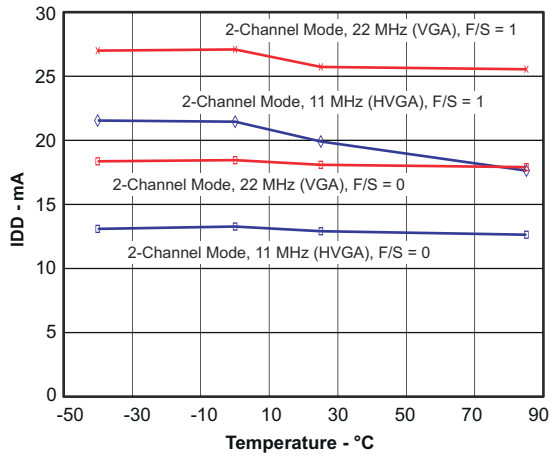


Figure 6-1. Supply Current vs Temperature

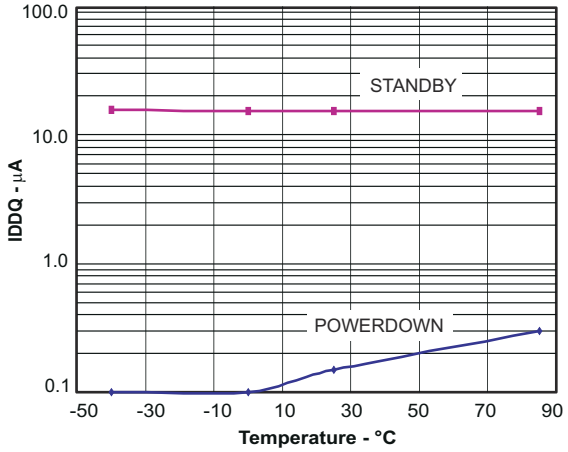


Figure 6-2. Quiescent Supply Current vs Temperature

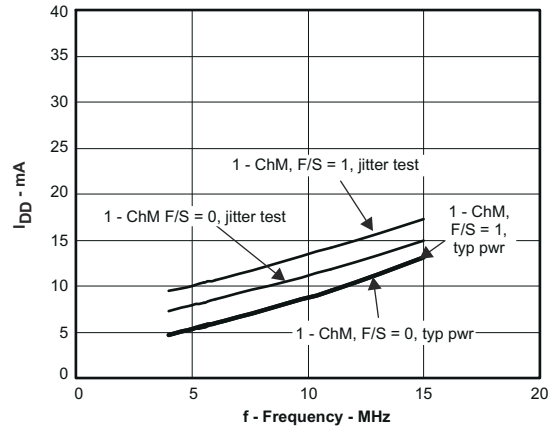


Figure 6-3. Supply Current vs Frequency, 1-Channel Mode

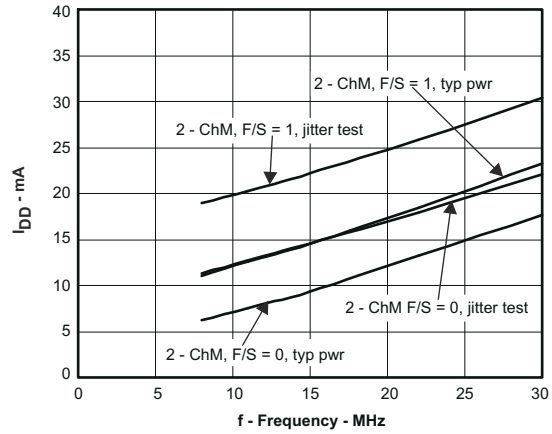


Figure 6-4. Supply Current vs Frequency, 2-Channel Mode

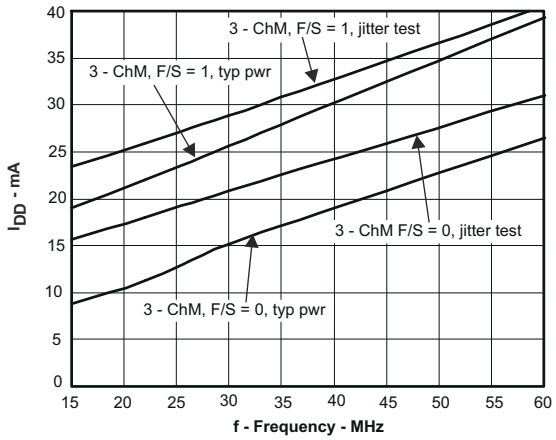


Figure 6-5. Supply Current vs Frequency, 3-Channel Mode

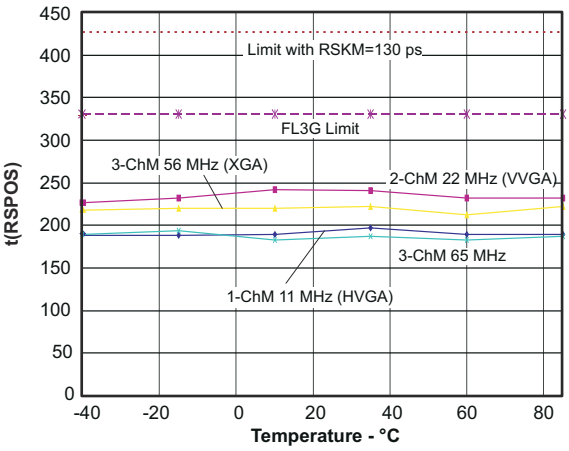


Figure 6-6. Receiver Strobe Position vs Temperature

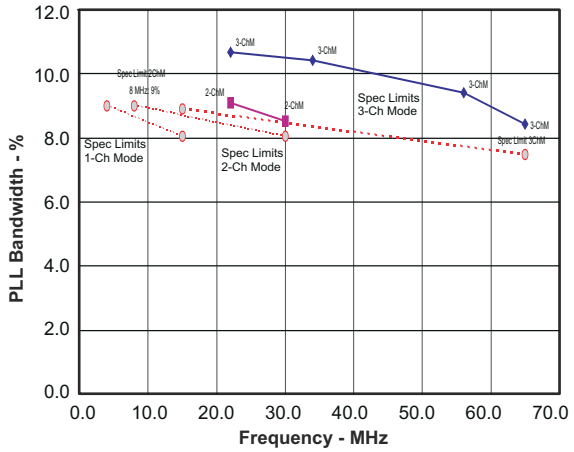


Figure 6-7. PLL Bandwidth

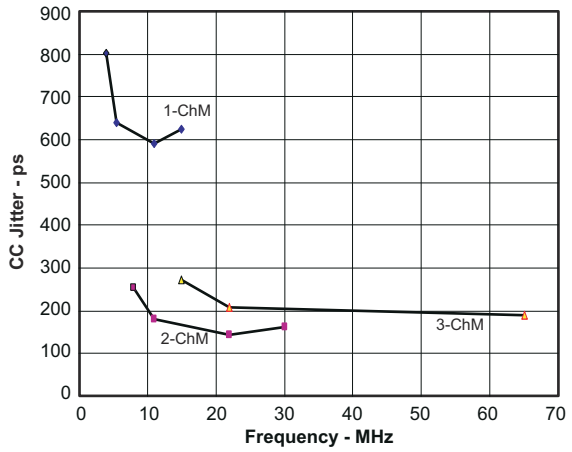


Figure 6-8. PCLK Cycle-to-Cycle Output Jitter

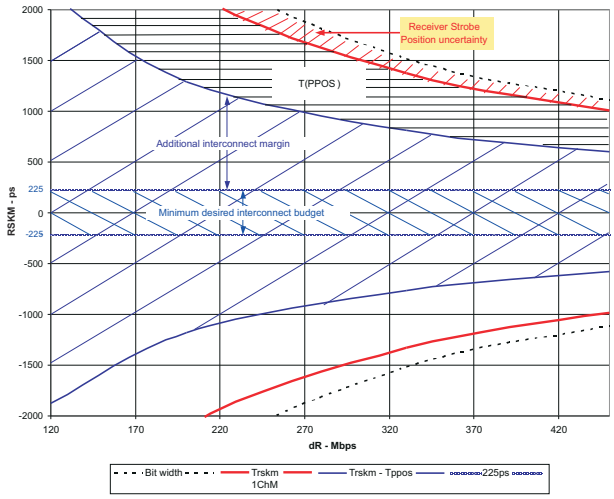


Figure 6-9. RSKM, 1-Channel Mode vs Bit Rate

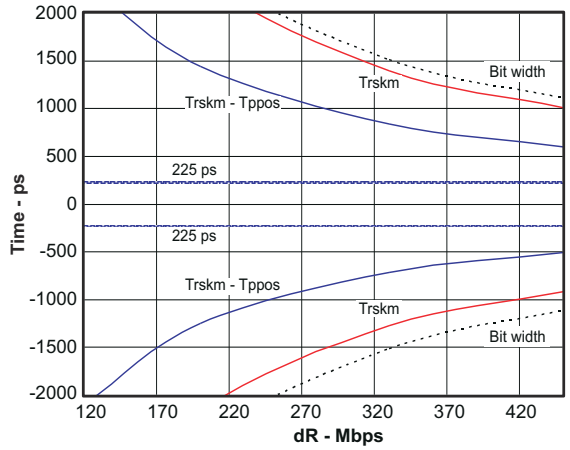


Figure 6-10. RSKM, 2-Channel Mode vs Bit Rate

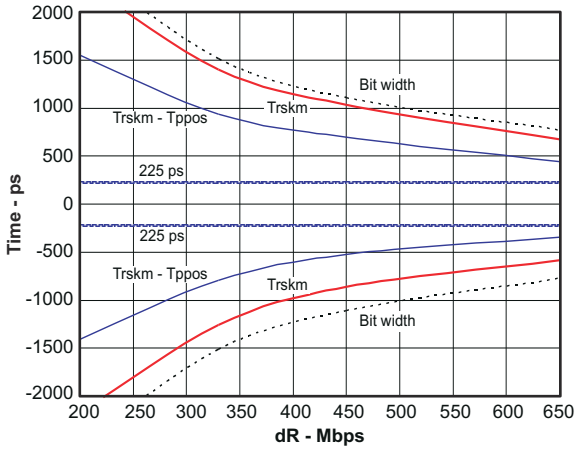


Figure 6-11. RSKM, 3-Channel Mode vs Bit Rate

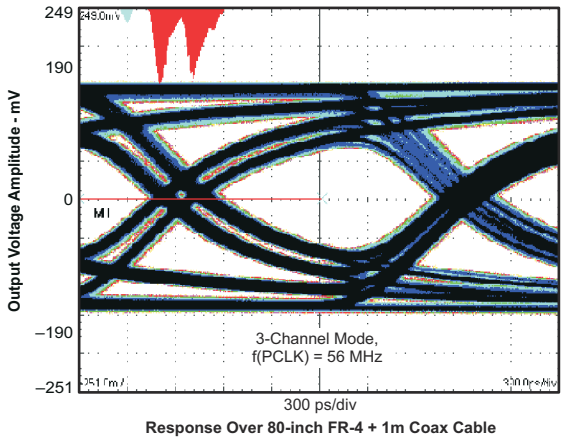


Figure 6-12. XGA 3-Channel Output Waveform

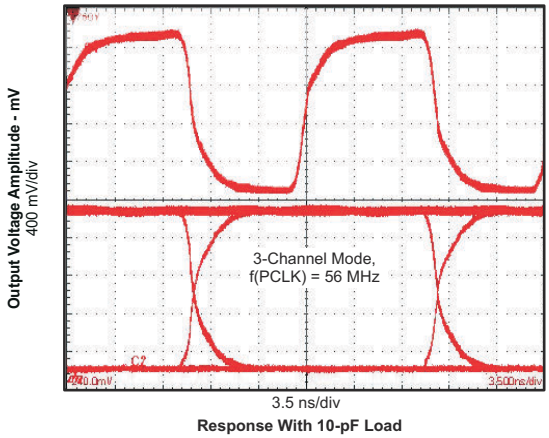


Figure 6-13. XGA 3-Channel Output Waveform

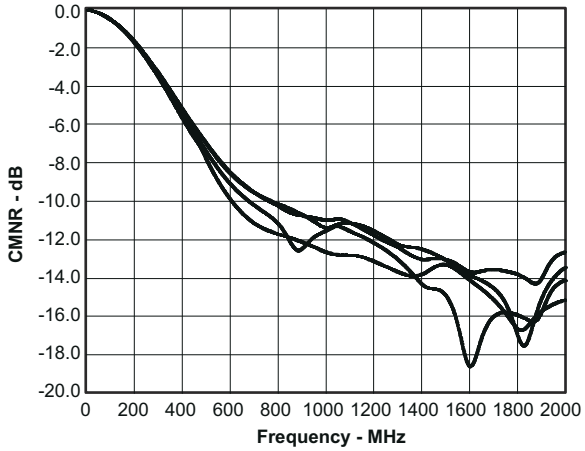


Figure 6-14. Input Common-Mode Noise Rejection vs Frequency

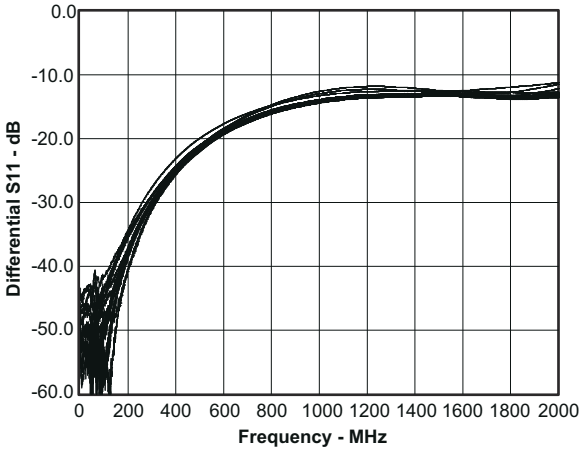


Figure 6-15. Input Return Loss

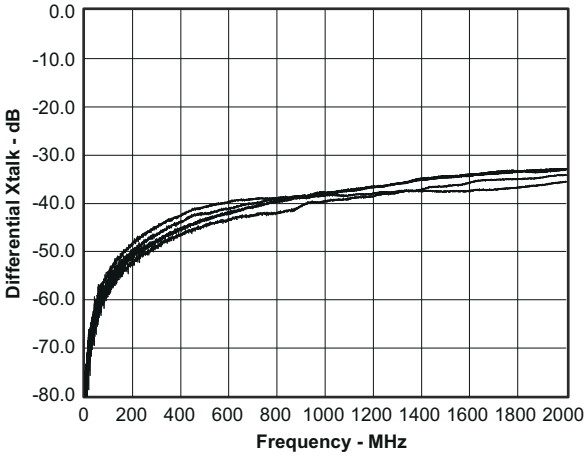


Figure 6-16. Input Differential Crosstalk vs Frequency

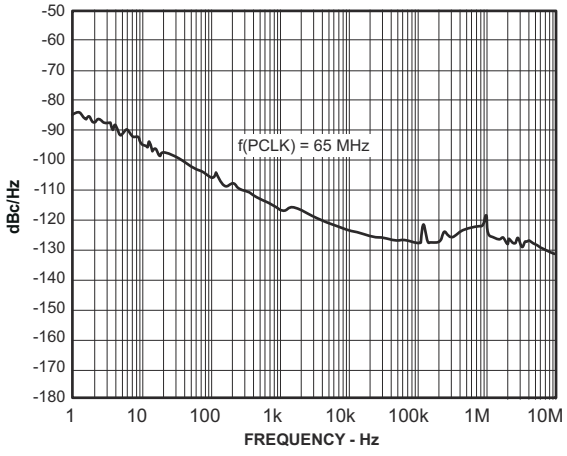


Figure 6-17. Phase Noise

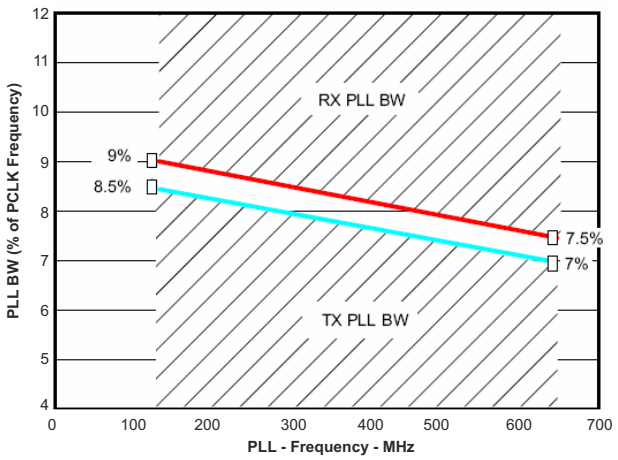


Figure 6-18. SN65LVDS302 PLL Bandwidth

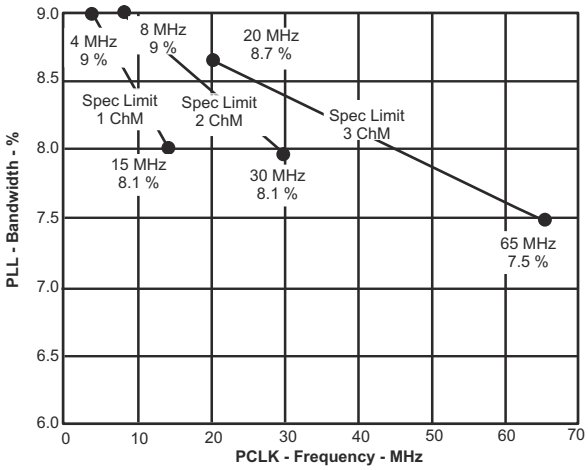


Figure 6-19. SN65LVDS301 PLL Bandwidth

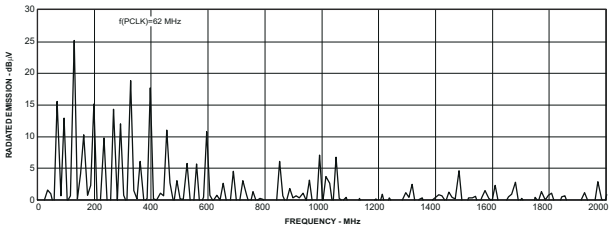


Figure 6-20. GTEM SAE J1752/3 EMI Test

7 Parameter Measurement Information

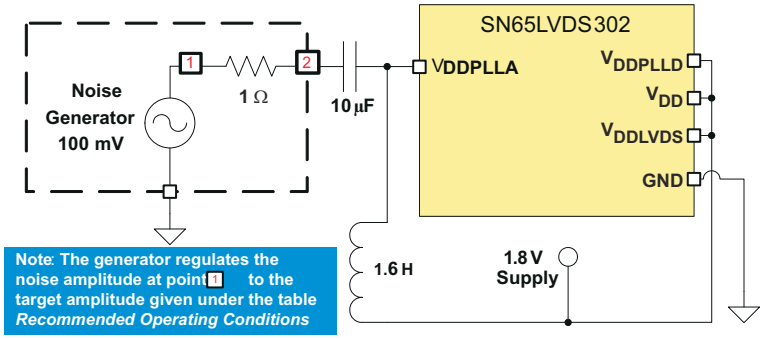


Figure 7-1. Power Supply Noise Test Set-Up

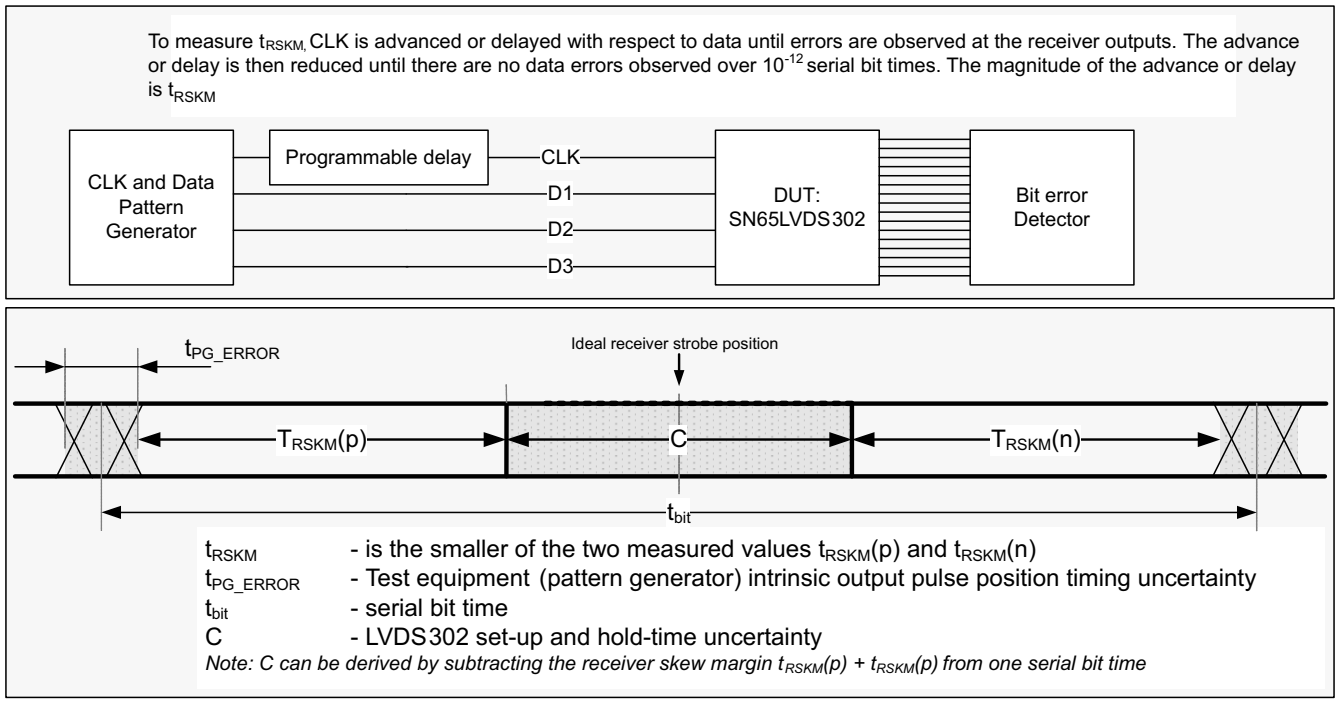


Figure 7-2. Jitter Budget

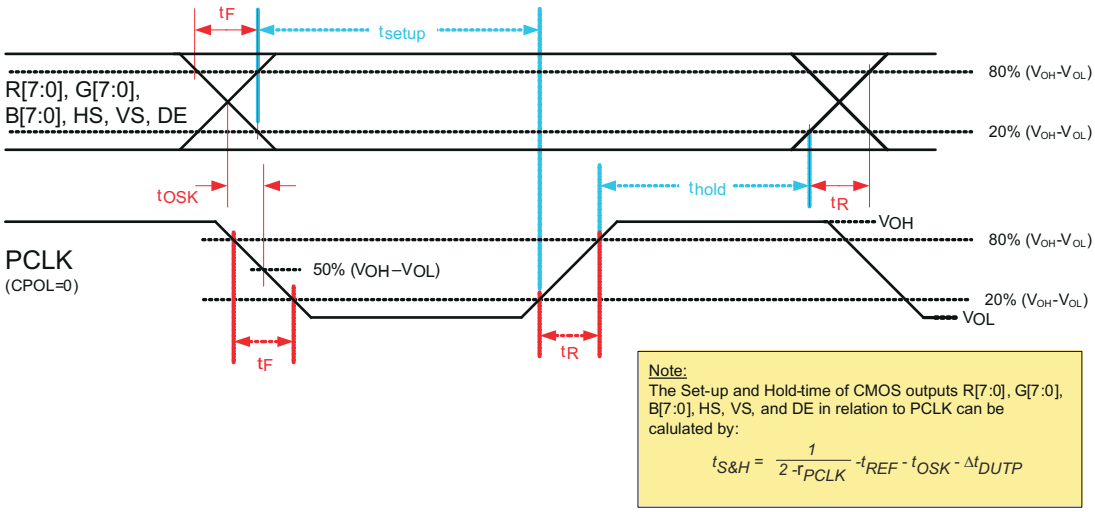


Figure 7-3. Output Rise and Fall, Setup and Hold Time

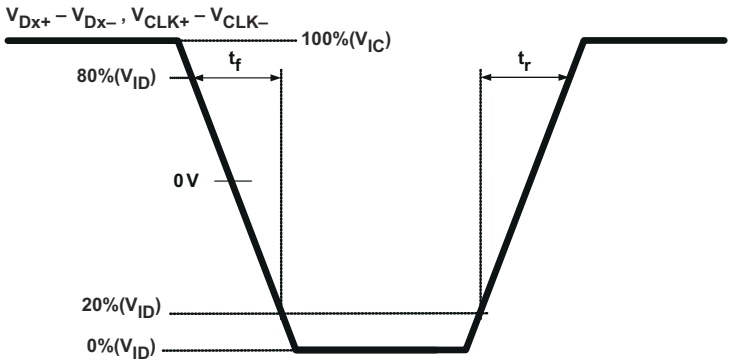


Figure 7-4. SubLVDS Differential Input Rise and Fall Time Defintion

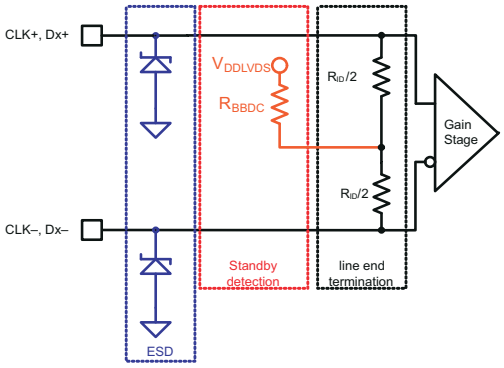


Figure 7-5. Equivalent Input Circuit Design

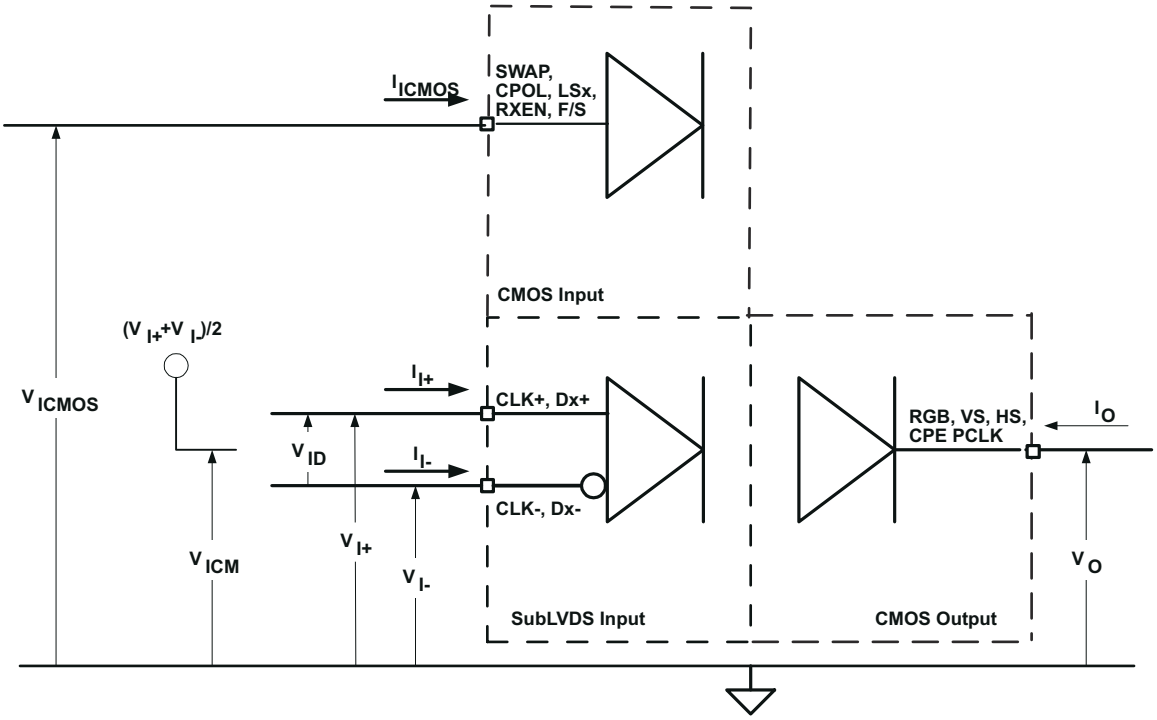


Figure 7-6. I/O Voltage and Current Definition

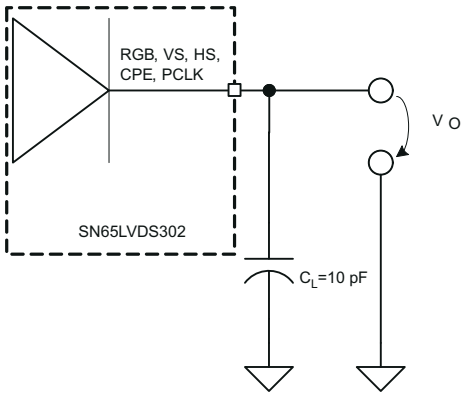


Figure 7-7. CMOS Output Test Circuit, Signal and Timing Definition

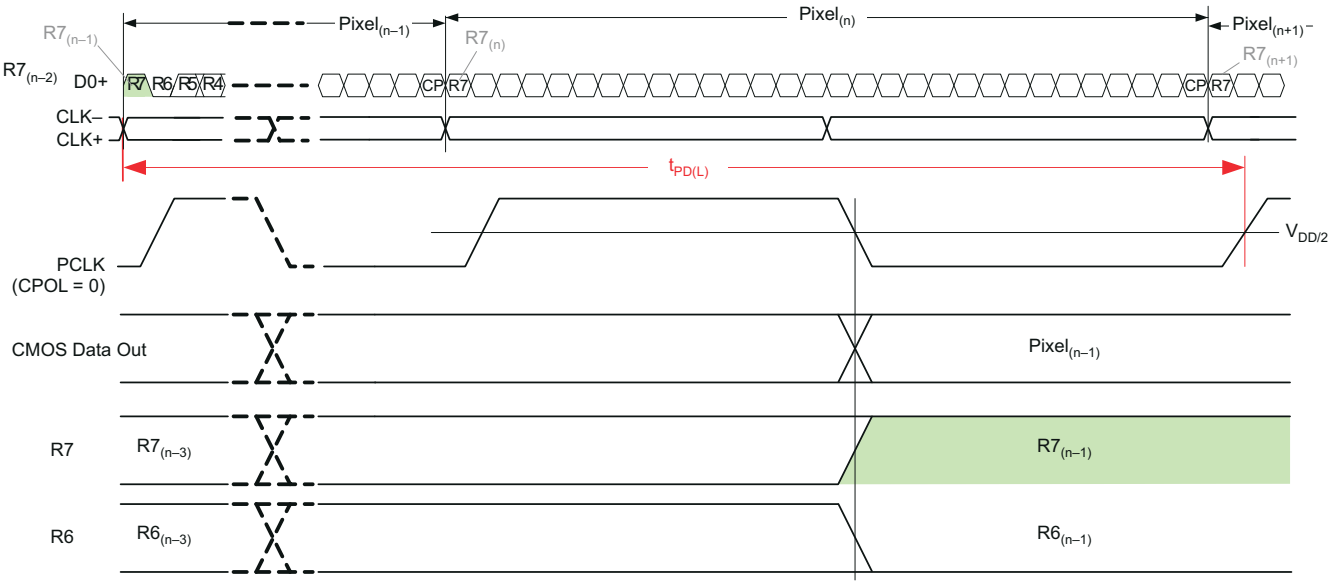


Figure 7-8. Propagation Delay Input to Output (LS0 = LS1 = 0)

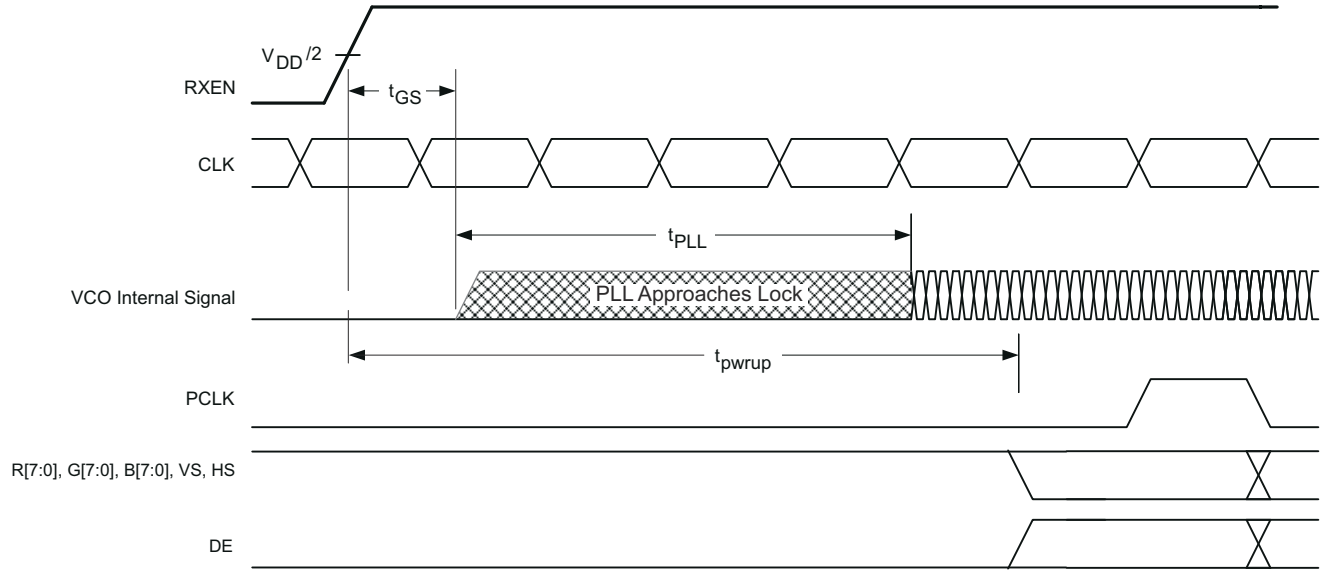


Figure 7-9. Receiver Phase Lock Loop Set Time and Receiver Enable Time

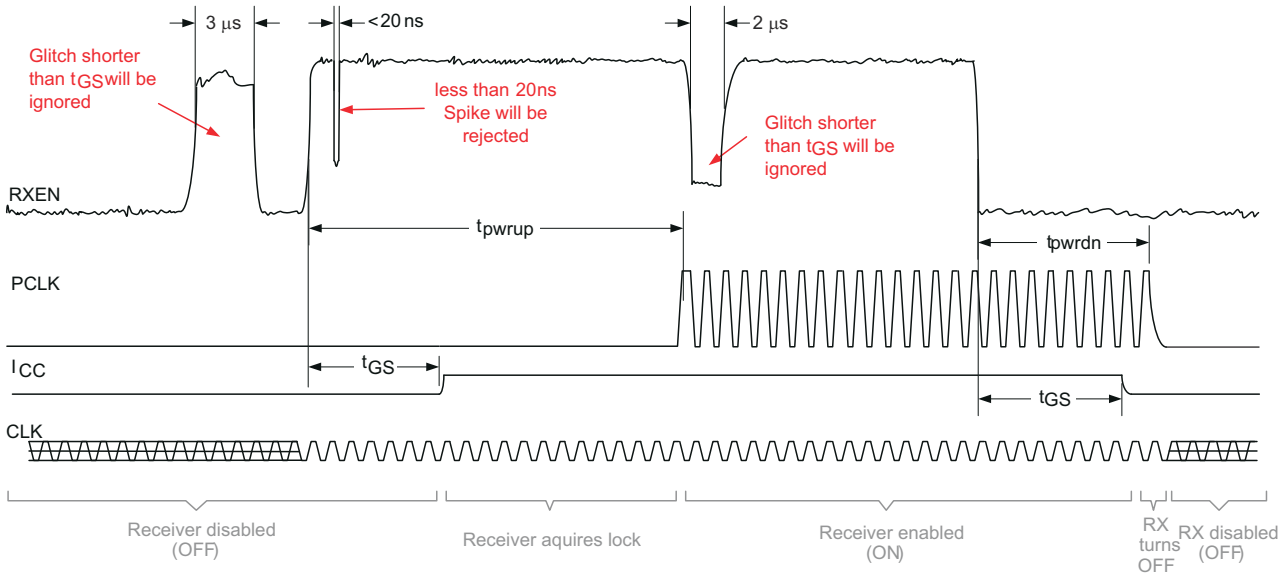


Figure 7-10. Receiver Enable and Disable Glitch Suppression Time

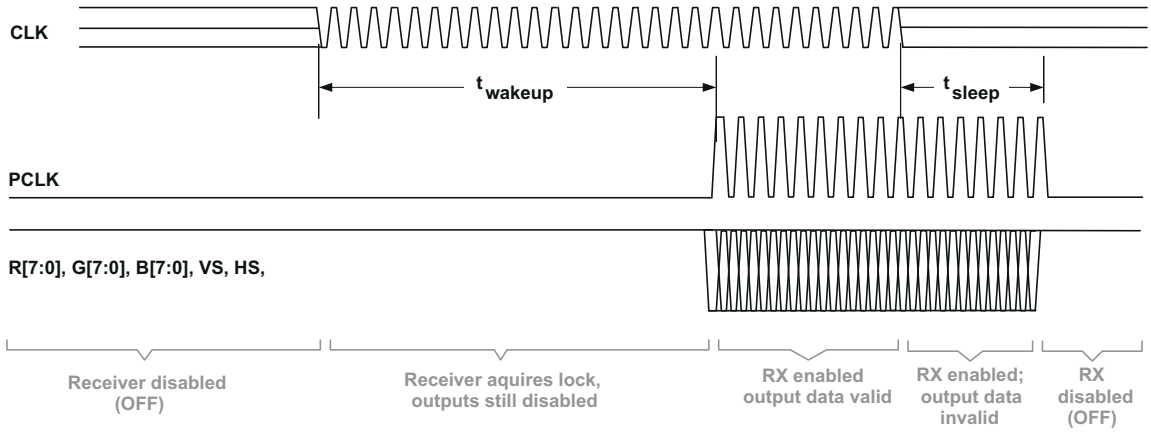


Figure 7-11. Standby Detection

7.1 Power Consumption Tests

Table 7-1 shows an example test pattern word.

Table 7-1. Example Test Pattern Word

WORD	R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0x7C3E1E7

7				C				3				E				1				E				7			
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	0	VS	HS	DE
0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1

7.2 Typical IC Power Consumption Test Pattern

Typical power-consumption test patterns consist of sixteen 30-bit receive words in 1-channel mode, eight 30-bit receive words in 2-channel mode and five 30-bit receive words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible code on the RGB outputs has the same probability to occur during typical device operation.

Table 7-2. Typical IC Power Consumption Test Pattern, 1-Channel Mode

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0x0000007
2	0xFFF0007
3	0x01FFF47
4	0xF0E07F7
5	0x7C3E1E7
6	0xE707C37
7	0xE1CE6C7
8	0xF1B9237
9	0x91BB347
10	0xD4CCC67
11	0xAD53377
12	0xACB2207
13	0xAAB2697
14	0x5556957
15	0xAAAAAB3
16	0xAAAAAA5

Table 7-3. Typical IC Power Consumption Test Pattern, 2-Channel Mode

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0x0000001
2	0x03F03F1
3	0xBFFBFF1
4	0x1D71D71
5	0x4C74C71
6	0xC45C451
7	0xA3aA3A5
8	0x5555553

Table 7-4. Typical IC Power Consumption Test Pattern, 3-Channel Mode

WORD	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0xFFFFFF1
2	0x0000001
3	0xF0F0F01
4	0xCCCCCC1
5	0xAAAAAA7

7.3 Maximum Power Consumption Test Pattern

The maximum (or worst-case) power consumption of the SN65LVDS302 is tested using the two different test pattern shown in table. Test patterns consist of sixteen 30-bit receive words in 1-channel mode, eight 30-bit receive words in 2-channel mode, and five 30-bit receive words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible code on RGB outputs has the same probability to occur during typical device operation.

Table 7-5. Worst-Case Power Consumption Test Pattern

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0xAAAAAA5
2	0x5555555

Table 7-6. Worst-Case Power Consumption Test Pattern

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0x0000000
2	0xFFFFFF7

7.4 Output Skew Pulse Position and Jitter Performance

The following test patterns are used to measure the output skew pulse position and the jitter performance of the SN65LVDS302. The jitter test pattern stresses the interconnect, particularly to test for ISI, using very long run-lengths of consecutive bits, and incorporating very high and low data rates, maximizing switching noise. Each pattern is self-repeating for the duration of the test.

Table 7-7. Receive Jitter Test Pattern, 1-Channel Mode

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0x0000001
2	0x0000031
3	0x00000F1
4	0x00003F1
5	0x0000FF1
6	0x0003FF1
7	0x000FFF1
8	0x0F0F0F1
9	0x0C30C31
10	0x0842111
11	0x1C71C71
12	0x18C6311
13	0x1111111
14	0x3333331
15	0x2452413
16	0x22A2A25
17	0x5555553
18	0xDB6DB65
19	0xCCCCCC1
20	0xEEEEEE1
21	0xE739CE1
22	0xE38E381
23	0xF7BDEE1
24	0xF3CF3C1
25	0xF0F0F01
26	0xFFF0001
27	0xFFFC001
28	0xFFFF001
29	0xFFFFC01

Table 7-7. Receive Jitter Test Pattern, 1-Channel Mode (continued)

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
30	0xFFFFF01
31	0xFFFFFC1
32	0xFFFFFF1

Table 7-8. Receive Jitter Test Pattern, 2-Channel Mode

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0x0000001
2	0x000FFF3
3	0x8008001
4	0x0030037
5	0xE00E001
6	0x00FF001
7	0x007E001
8	0x003C001
9	0x0018001
10	0x1C7E381
11	0x3333331
12	0x555AAA5
13	0x6DBDB61
14	0x7777771
15	0x555AAA3
16	0xAAAAAA5
17	0x5555553
18	0xAAA5555
19	0x8888881
20	0x9242491
21	0xAAA5571
22	0xCCCCCC1
23	0xE3E1C71
24	0xFFE7FF1
25	0xFFC3FF1
26	0xFF81FF1
27	0xFE00FF1
28	0x1FF1FF1
29	0xFFCFFC3
30	0x7FF7FF1
31	0xFFF0007
32	0xFFFFFF1

Table 7-9. Receive Jitter Test Pattern, 3-Channel Mode

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
1	0x0000001
2	0x0000001
3	0x0000003

Table 7-9. Receive Jitter Test Pattern, 3-Channel Mode (continued)

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7–4], B[3–0], 0, VS, HS, DE
4	0x0101013
5	0x0303033
6	0x0707073
7	0x1818183
8	0xE7E7E71
9	0x3535351
10	0x0202021
11	0x5454543
12	0xA5A5A51
13	0xADADAD1
14	0x5555551
15	0xA6A2AA3
16	0xA6A2AA5
17	0x5555553
18	0x5555555
19	0xAAAAAA1
20	0x5252521
21	0x5A5A5A1
22	0xABABAB1
23	0xFDFCFD1
24	0xCAAACA1
25	0x1818181
26	0xE7E7E71
27	0xF8F8F81
28	0xFCFCFC1
29	0xFEFEFE1
30	0xFFFFFF1
31	0xFFFFFF5
32	0xFFFFFF5

8 Detailed Description

8.1 Overview

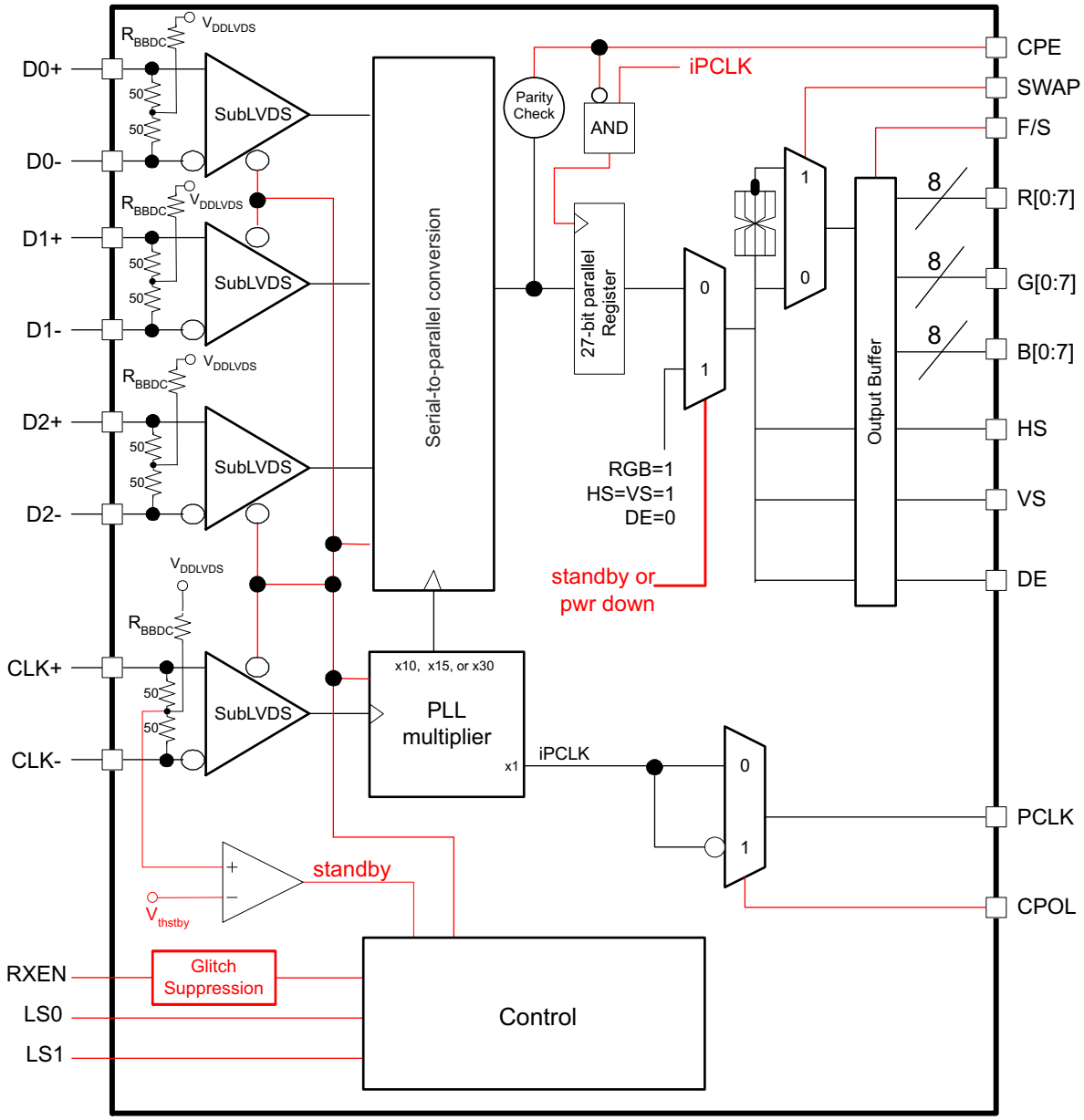
The SN65LVDS302 is a de-serialising device where the input serial data and clock are received through Sub Low-Voltage Differential Signaling (SubLVDS) lines. The SN65LVDS302 supports three operating power modes (Shutdown, Standby, and Active) to conserve power.

Two Link Select lines LS0 and LS1 select whether 1, 2, or 3 serial links are used. The RXEN input may be used to put the SN65LVDS302 in a Shutdown mode. The SN65LVDS302 enters an active Standby mode if the common mode voltage of the CLK input becomes shifted to V_{DDLVDS}, as when the transmitter releases the CLK output into high-impedance. This minimizes power consumption without the need of switching an external control pin. The SN65LVDS302 is characterized for operation over ambient air temperatures of –40°C to 85°C. All CMOS and SubLVDS signals are 2-V tolerant with V_{DD} = 0 V. This feature allows signal power-up before V_{CC} is stabilized.

When receiving, the PLL locks to the incoming clock (CLK) and generates an internal high-speed clock at the line rate of the data lines. The data is serially loaded into a shift register using the internal high-speed clock. The de-serialized data is presented on the parallel output bus with a recreation of the Pixel clock (PCLK) generated from the internal high-speed clock. If no input CLK signal is present, the output bus is held static with the PCLK and DE held low, while all other parallel outputs are pulled high.

The parallel (CMOS) output bus offers a bus-swap feature. The SWAP control pin controls the output pin order of the output pixel data to be either R[7:0]. G[7:0], B[7:0], VS, HS, DE or B[0:7], G[0:7], R[0:7], VS, HS, DE. This gives a PCB designer the flexibility to better match the bus to the LCD driver pinout or to put the receiver device on the top side or the bottom side of the PCB. The F/S control input selects between a slow CMOS bus output rise time for best EMI and power consumption and a fast CMOS output for increased speed or higher load designs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Swap Pin Functionality

The SWAP pin allows the pcb designer to reverse the RGB bus, minimizing potential signal crossovers due to signal routing. The two drawings beneath show the RGB signal pin assignment based on the SWAP pin setting.

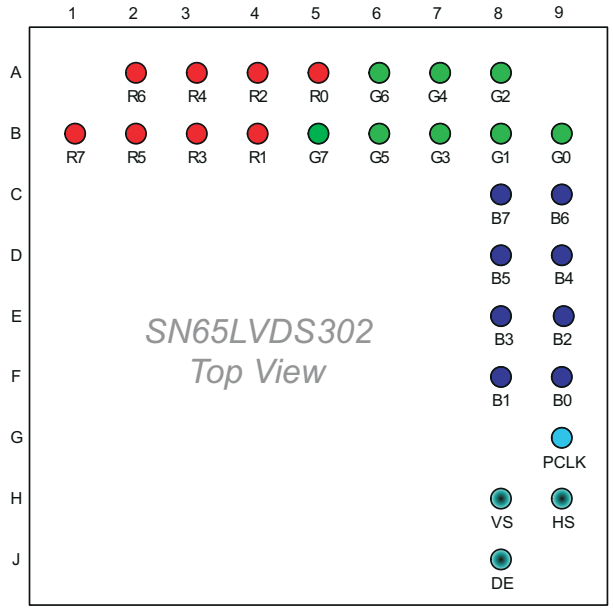


Figure 8-1. Pinout With SWAP PIN = GND

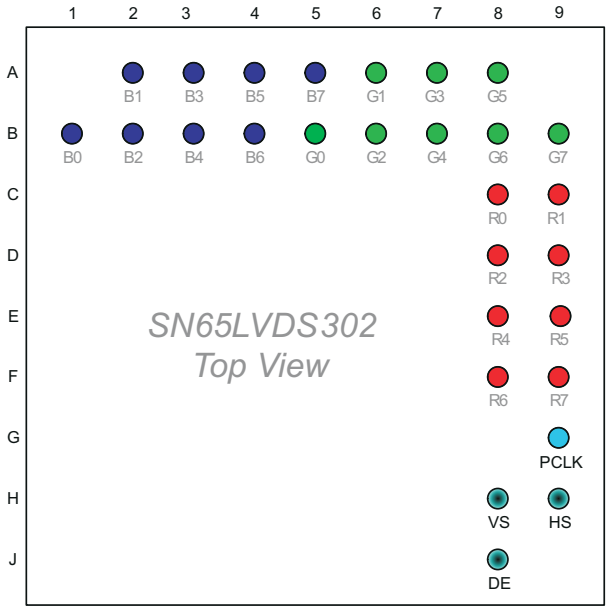
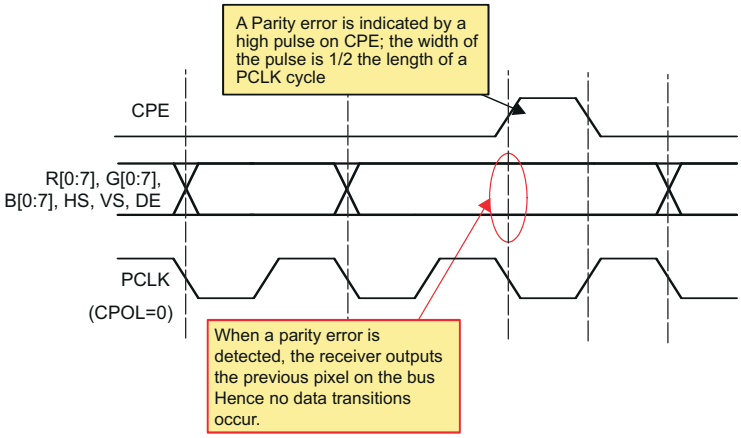


Figure 8-2. Pinout With SWAP PIN = VDD

8.3.2 Parity Error Detection and Handling

The SN65LVDS302 receiver performs error checking on the basis of a parity bit that is transmitted across the subLVDS interface from the transmitting device. Once the SN65LVDS302 detects the presence of the clock and the PLL has locked onto PCLK, then the parity is checked. Parity-error detection ensures detection of all single bit errors in one pixel and 50% of all multi-bit errors.

The parity bit covers the 27 bit data payload consisting of 24 bits of pixel data plus VS, HS, and DE. Odd Parity bit signalling is used. The parity error is output on the CPE pin. If the sum of the 27 data bits and the parity bit result in an odd number, the receive data are assumed to be valid. The CPE output is held low. If the sum equals an even number, parity error is declared. The CPE output indicates high for half a PCLK period. The CPE output is set with the data bit transition and cleared after 1/2 the data bit time. This allows counting every detected parity error with a simple counter connected to CPE.



Also if there is a parity error detected then the data on that PCLK cycle is not output. Instead, the last valid data from a previous PCLK cycle is repeated on the output bus. This is to prevent any bit error that may occur on the LVDS link from causing perturbations in VS, HS, or DE that may be visually disruptive to a display.

The reserved bits are not covered in the parity calculations.

Figure 8-3. Parity Error Detection and Handling

8.4 Device Functional Modes

8.4.1 Deserialization Modes

The SN65LVDS302 receiver has three modes of operation controlled by link-select pins LS0 and LS1. Table 8-1 shows the deserializer modes of operation.

Table 8-1. Logic Table: Link Select Operating Modes

LS1	LS0	MODE OF OPERATION		DATA LINKS STATUS
0	0	1ChM	1-channel mode (30-bit serialization rate)	D0 active; D1, D2 disabled
0	1	2ChM	2-channel mode (15-bit serialization rate)	D0, D1 active; D2 disabled
1	0	3ChM	3-channel mode (10-bit serialization rate)	D0, D1, D2 active
1	1		Reserved	Reserved

8.4.1.1 1-Channel Mode

While LS0 and LS1 are held low, the SN65LVDS302 receives payload data over a single SubLVDS data pair, D0. The PLL locks to the SubLVDS clock input and internally multiplies the clock by a factor of 30. The internal high speed clock is used to shift in the data payload on D0 and to deserialize 30 bits of data. Figure 8-4 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high speed clock is divided by a factor of 30 to recreate the pixel clock and the data payload with the pixel clock is presented on the output bus. The reserved bits and parity bit are not output. While in this mode, the PLL can lock to a clock that is in the range of 4 MHz through 15 MHz. This mode is intended for smaller video display formats that do not need the full bandwidth capabilities of the SN65LVDS302.

Figure 8-4. Data and Clock Input in 1-ChM (LS0 and LS1 = low)

8.4.1.2 2-Channel Mode

While LS0 is held high and LS1 is held low, the SN65LVDS302 receives payload data over two SubLVDS data pairs, D0 and D1. The PLL locks to the SubLVDS clock input and internally multiplies the clock by a factor of 15. The internal high speed clock is used to shift in the data payload on D0 and D1 and to deserialize 15 bits of data from each pair. Figure 8-5 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high speed clock is divided by a factor of 15 to recreate the pixel clock, and the data payload with pixel clock is presented on the output bus. The reserved bits and parity bit are not output. While in this mode the PLL can lock to a clock that is in the range of 8 MHz through 30 MHz.

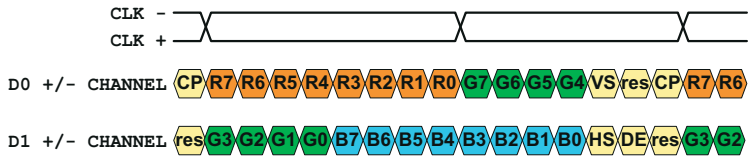


Figure 8-5. Data and Clock Input in 2-ChM (LS0 = high; LS1 = low)

8.4.1.3 3-Channel Mode

While LS0 is held low and LS1 is held high the SN65LVDS302 receives payload data over three SubLVDS data pairs: D0, D1, and D2. The PLL locks to the SubLVDS clock input and internally multiplies the clock by a factor of 10. The internal high speed clock is used to shift in the data payload on D0, D1, and D2, and to deserialize 10 bits of data from each pair. Figure 8-6 illustrates the timing and the mapping of the data payload into the 30-bit frame. While in this mode the PLL can lock to a clock that is in the range of 20 MHz through 65 MHz.

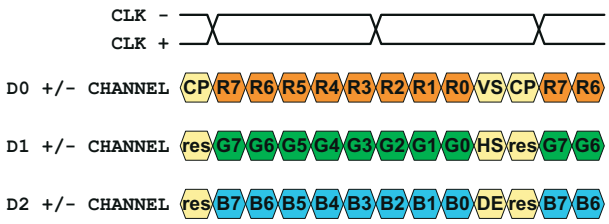


Figure 8-6. Data and Clock Input in 3-ChM (LS0 = low; LS1 = high)

8.4.2 Powerdown Modes

The SN65LVDS302 Receiver has two powerdown modes to facilitate efficient power management.

8.4.2.1 Shutdown Mode

A low input signal on the RXEN pin puts the SN65LVDS302 into Shutdown mode. This turns off most of the receiver circuitry including the SubLVDS receivers, PLL, and deserializers. The subLVDS differential-input resistance remains 100 Ω, while any input signal is ignored. All outputs hold a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

The current draw in Shutdown mode is nearly zero if the SubLVDS inputs are left open or pulled high.

8.4.2.2 Standby Mode

The SN65LVDS302 enters the Standby mode when the SN65LVDS302 is not in Shutdown mode but the SubLVDS clock-input common-mode voltage is above 0.9 × V_{DDLVDS}. The CLK input incorporates a pull-up circuit to shift the SubLVDS clock-input common-mode voltage to V_{DDLVDS} in the absence of an input signal. All circuitry except the SubLVDS clock-input Standby monitor is shut down. The SN65LVDS302 also enters Standby mode when the input clock frequency on the CLK input is less than 500 kHz. The SubLVDS input resistance remains 100 Ω while any input signal on the data inputs D0, D1, and D2 becomes ignored. All outputs holds a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

The current drawn in Standby mode is very low.

8.4.3 Active Modes

A high input signal on RXEN combined with a CLK input signal switching faster than 3 MHz and V_{ICM} smaller than 1.3 V forces the SN65LVDS302 into Active mode. Current consumption in active mode depends on operating frequency and the number of data transitions in the data payload. CLK-input frequencies from 3 MHz to 4 MHz activates the device but proper PLL functionality is not secured. The SN65LVDS302 must not be operated in active mode at CLK frequencies below 4 MHz.

8.4.3.1 Acquire Mode (PLL Approaches Lock)

When the SN65LVDS302 is enabled and a SubLVDS clock input present, the PLL pursues lock to the input clock. While the PLL pursues lock the output data bus holds a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

For proper device operation, the pixel clock frequency must fall within the valid f_{PCLK} range specified under recommended operating conditions. If the pixel clock frequency is larger than 3 MHz but smaller than $f_{PCLK(min)}$, the SN65LVDS302 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into active receive mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

8.4.3.2 Receive Mode

After the PLL achieves lock the device enters the normal receive mode. The output data bus presents the de-serialized data. The PCLK output pin outputs the recovered pixel clock.

8.4.4 Status Detect and Operating Modes Flow

The SN65LVDS302 switches between the power saving and active modes in the following way:

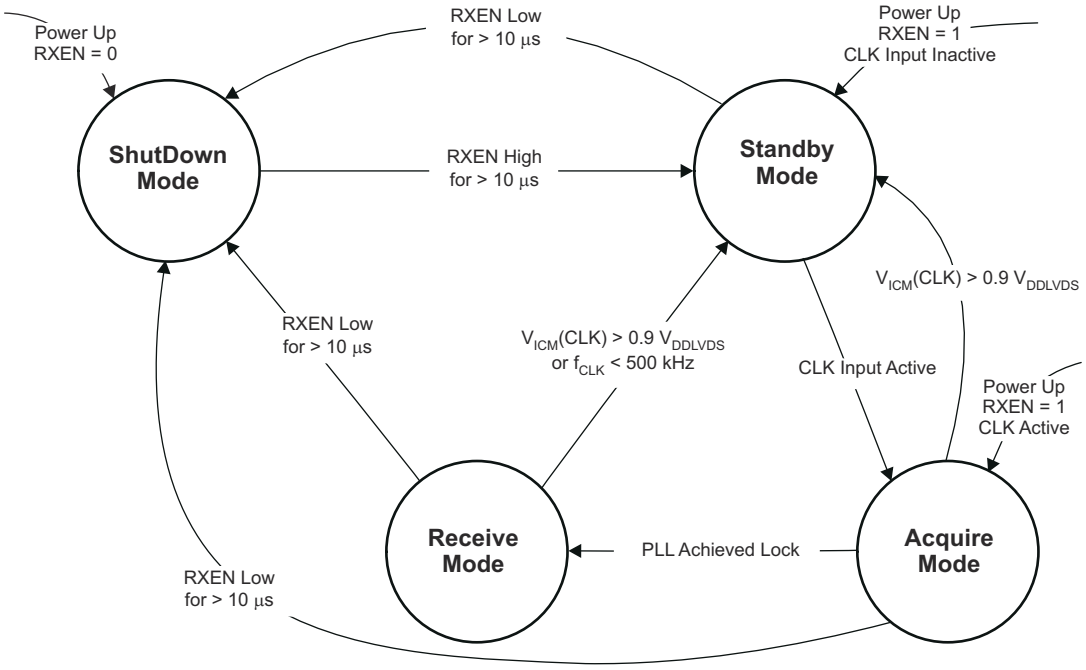


Figure 8-7. Operating Modes and State Machine Diagram

Table 8-2. Status Detect and Operating Modes Descriptions

MODE	CHARACTERISTICS	CONDITIONS
Shutdown Mode	Least amount of power consumption (most circuitry turned off); All outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high DE = PCLK = low;	RXEN is set low for longer than 10 µs(1) (2)
Standby Mode	Low power consumption (Standby monitor circuit active; PLL is shutdown to conserve power); All outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high DE = PCLK = low;	RXEN is high for longer than 10 µs, and both CLK input common-mode $V_{ICM(CLK)}$ above 0.9 × V_{DDLVDS}, or CLK input floating(2)
Acquire Mode	PLL pursues lock; All outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high DE = PCLK = low;	RXEN is high; CLK input monitor detected clock input common mode and woke up receiver out of Standby mode
Receive Mode	Data transfer (normal operation); receiver deserializes data and provides data on parallel output	RXEN is high and PLL is locked to incoming clock

(1) In Shutdown Mode, all SN65LVDS302 internal switching circuits (for example: PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.

(2) Leaving CMOS control inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All CMOS inputs must be tied to a valid logic level V_{IL} or V_{IH} during Shutdown or Standby Mode. Exceptions are the subLVDS inputs CLK and Dx, which can be left unconnected while not in use.

Table 8-3. Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → Standby	Drive RXEN high to enable receiver	1. RXEN high > 10 µs 2. Receiver enters standby mode a. R[0:7] = G[0:7] = B[0:7] = VS = HS remain high and DE = PCLK low b. Receiver activates clock input monitor
Standby → Acquire	Transmitter activity detected	1. CLK input monitor detects clock input activity 2. Outputs remain static 3. PLL circuit is enabled
Acquire → Receive	Link is ready to receive data	1. PLL is active and approaches lock 2. PLL achieves lock within t_{wakeup} 3. D1, D2, or D3 become active depending on LS0 and LS1 selection 4. First Data word was recovered 5. Parallel output bus turns on switching from static output pattern to output first valid data word
Receive → Standby	Transmitter requested to enter Standby mode by input common mode voltage V_{ICM} > 0.9 V_{DDLVDS} as when transmitter output clock stops or enters high-impedance state.	1. Receiver disables outputs within t_{sleep} 2. RX Input monitor detects V_{ICM} > 0.9 VDD_{LVDS} within t_{sleep} 3. R[0:7] = G[0:7] = B[0:7] = VS = HS transition to high and DE = PCLK to low on next falling PLL clock edge 4. PLL shuts down. Clock activity input monitor remains active
Receive and Standby → Shutdown	Turn off Receiver	1. RXEN pulled low for > t_{pwrdn} 2. R[0:7] = G[0:7] = B[0:7] = VS = HS remain static high or transition to static high and DE = PCLK remain or transition to static low 3. Most IC circuitry is shut down for least power consumption

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Application Information

General application guidelines and hints for LVDS drivers and receivers may be found in the LVDS application notes and design guides.

9.1.2 Preventing Increased Leakage Currents in Control Inputs

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. Do not leave any CMOS input unconnected or floating. Every input must be connected to a valid logic level V_{IH} or V_{OL} while power is supplied to V_{DD}. This also minimizes the power consumption of standby and power down mode.

9.1.3 Calculation Example: HVGA Display

The following calculation shows an example for a Half-VGA display with the following parameters:

Display Resolution:	480 × 320
Frame Refresh Rate:	58.4 Hz
Horizontal Visible Pixel:	480 columns
Horizontal Front Porch:	20 columns
Horizontal Sync:	5 columns
Horizontal Back Porch:	3 columns
Vertical Visible Pixel:	320 lines
Vertical Front Porch:	10 lines
Vertical Sync:	5 lines
Vertical Back Porch:	3 lines

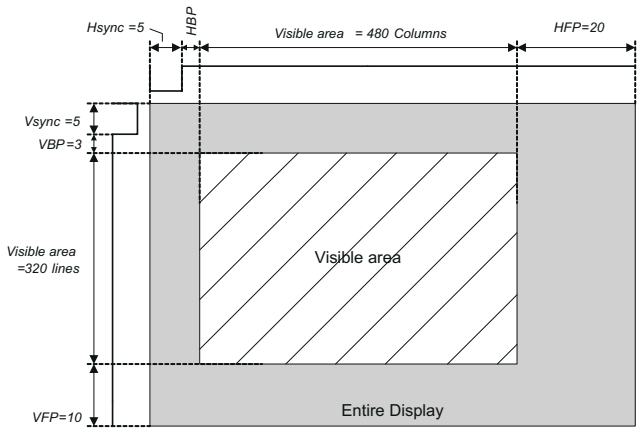


Figure 9-1. HVGA Display

Calculation of the total number of pixel and blanking overhead:

Visible Area Pixel Count:	480 × 320 = 153600 pixel
Total Frame Pixel Count:	(480 + 20 + 5 + 3) × (320 + 10 + 5 + 3) = 171704 pixel
Blanking Overhead:	(171704 – 153600) ÷ 153600 = 11.8%

The application requires the following serial-link parameters:

Pixel Clk Frequency:	171704 × 58.4 Hz = 10 MHz
Serial Data Rate:	1-channel mode: 10 MHz × 30 bit/channel = 300 Mbps 2-channel mode: 10 MHz × 15 bit/channel = 150 Mbps

9.1.4 How to Determine Interconnect Skew and Jitter Budget

Designing a reliable data link requires examining the interconnect skew and jitter budget. The sum of all transmitter, PCB, connector, FPC, and receiver uncertainties must be smaller than the available serial bit time. The highest pixel clock frequency defines the available serial bit time. The transmitter timing uncertainty is defined by t_{PPOS} in the transmitter data sheet. For a bit-error-rate target of ≤ 10^{-12}, the measurement duration for t_{PPOS} is ≥ 10^{12}. The SN65LVDS302 receiver can tolerate a maximum timing uncertainty defined by t_{RSKM}. The interconnect budget is calculated by Equation 1.

$$t_{interconnect} = t_{RSKM} - t_{PPOS} \quad (1)$$

Example:

f_{PCLK}(max)	23 MHz (VGA display resolution, 60 Hz)
Transmission mode: 2-ChM; t_{PPOS}(SN65LVDS301)	330 ps
Target bit error rate	10^{-12}
t_{RSKM}(SN65LVDS302)	1 / (2 × 15 × f_{PCLK}) – 480 ps = 969 ps

The interconnect budget for cable skew and ISI must be smaller than the output of Equation 2.

$$t_{interconnect} = t_{RSKM} - t_{PPOS} = 639ps \quad (2)$$

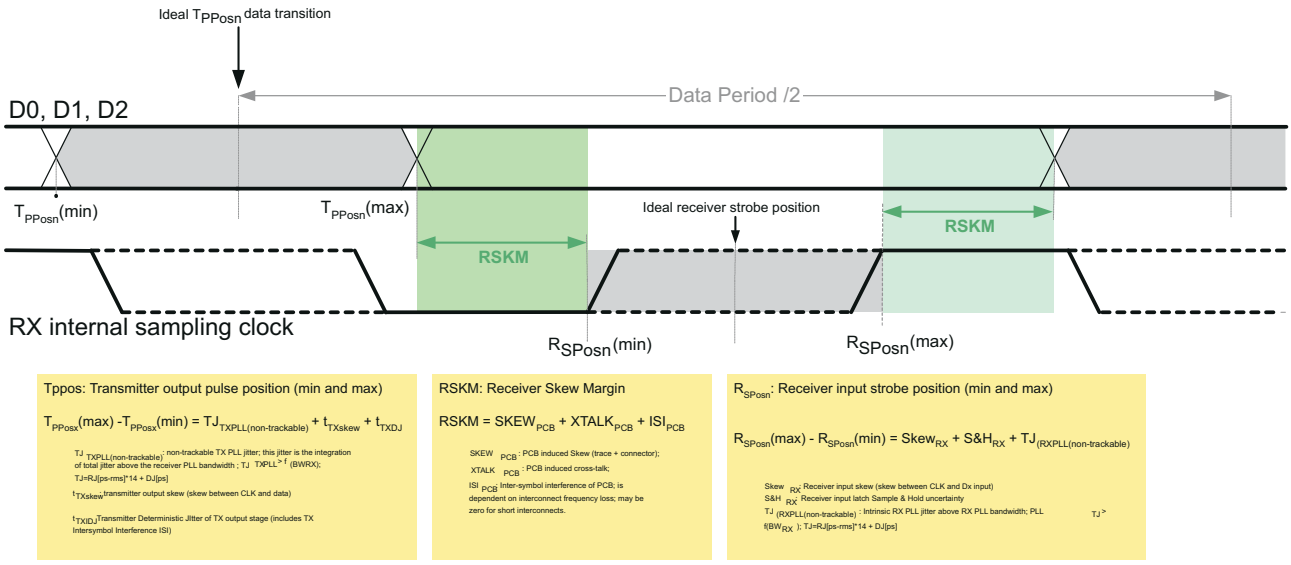


Figure 9-2. Jitter Budget

9.1.5 F/S Pin Setting and Connecting the SN65LVDS302 to an LCD Driver

Note

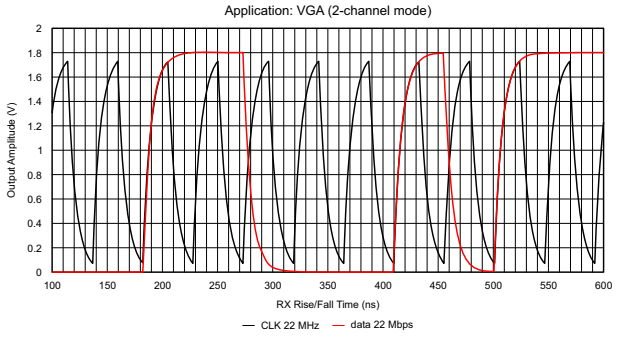
Receiver PLL tracking: To maximize the design margin for the interconnect, good RX PLL tracking of the TX PLL is important. FlatLink3G requires the RX PLL to have a bandwidth higher than the bandwidth of the TX PLL. The SN65LVDS302 PLL design is optimized to track the SN65LVDS0301 PLL particularly well, thus providing a very large receiver skew margin. A FlatLink3G-compliant link must provide at least ±225 ppm of receiver skew margin for the interconnect.

It is important to understand the tradeoff between power consumption, EMI, and maximum speed when selecting the F/S signal. It is beneficial to choose the slowest rise time possible to minimize EMI and power consumption. Unfortunately a slower rise time also reduces the timing margin left for the LCD driver. Hence it is necessary to calculate the timing margin to select the correct F/S pin setting.

The output rise time depends on the output driver strength and the output load. An LCD driver typical capacitive load is assumed with approximately 10 pF. As the capacitive load increases, the rise time also increases. Rise time of the SN65LVDS302 is measured as the time duration it takes the output voltage to rise from 20% of V_{DD} and 80% of V_{DD} and fall time is defined as the time for the output voltage to transition from 80% of V_{DD} down to 20%.

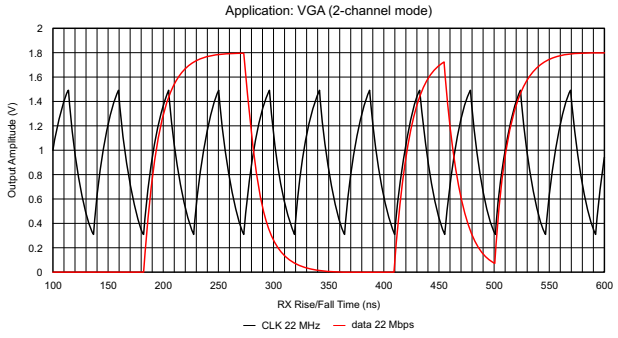
Within one mode of operation and one F/S pin setting, the rise time of the output stage is fixed and does not adjust to the pixel frequency. Due to the short bit time at very fast pixel clock speeds and the real capacitive load of the display driver, the output amplitude might not reach V_{DD} and GND saturation fully. To ensure sufficient signal swing and verify the design margin, it becomes necessary to determine that the output amplitude under any circumstance reaches the display driver's input stage logic threshold (usually 30% and 70% of V_{DD}).

Figure 9-3 shows a worst-case rise time simulation assuming a LCD driver load of 16 pF at VGA display resolution. PCLK is the fastest switching output. With F/S set to GND (Figure 9-4), the PCLK output voltage amplitude is significantly reduced. The voltage amplitude of the output data RGB[7:0], VS, HS, and DE shows less amplitude attenuation because these outputs carry random data pattern and toggle equal or less than half of the PCLK frequency. It is necessary to determine the timing margin between the LVDS302 output and LCD driver input.



F/S = V_{DD} CL = 16 pF

Figure 9-3. Output Amplitude vs Toggling Frequency (F/S = 1)



F/S = 0 CL = 16 pF

The data signal has a slower maximum switching frequency, and therefore drives a larger amplitude than the clock signal.

Figure 9-4. Output Amplitude vs Toggling Frequency (F/S = 0)

9.1.6 How to Determine the LCD Driver Timing Margin

To determine the timing margin, it is necessary to specify the frequency of operation, identify the set-up and hold time of the LCD driver, and specify the output load of the SN65LVDS302 as a combination of the LCD driver input parasitics plus any capacitance caused by the connecting PCB trace. Furthermore, the setting of pin F/S and the SN65LVDS302 output skew impact the margin. The total remaining design margin calculates as following:

$$t_{DM} = \frac{1}{2 \times f_{PCLK}} - t_{DUTP(max\_error)} - \frac{t_{rise(max)} \times C_{LOAD}}{10\ pF} - \left|t_{OSK}\right| \quad (3)$$

where

- t_{DM} is the design margin
- f_{PCLK} is the pixel clock frequency
- $t_{DUTP(max\_error)}$ is the maximum duty cycle error
- $t_{rise(max)}$ is the maximum rise or fall time; see $t_{R/F}$ under switching characteristics
- C_L is the parasitic capacitance (sum of LCD driver input parasitics + connecting PCB trace)
- t_{skew} is the clock to data output skew SN65LVDS302

Example:

At a pixel clock frequeny of 5.5 MHz (QVGA), and an assumed LCD driver load of 15 pF, the remaining timing margin is:

$$t_{DUTP(max\_error)} = \frac{\left|t_{DUTP}(max) - 50\right|}{100\%} \times t_{PCLK} = \frac{5\%}{100\%} \times \frac{1}{5.5\ MHz} = 9.1\ ns \quad (4)$$

$$t_{DM} = \frac{1}{2 \times 5.5\ MHz} - 9\ ns - \frac{16\ ns_{(F/S=GND)} \times 15\ pF}{10\ pF} - 500\ ps = 57.3\ ns \quad (5)$$

As long as the set-up and hold time of the LCD driver are each less than 57 ns, the timing budget is met sufficiently.

9.1.7 Typical Application Frequencies

The SN65LVDS302 supports pixel clock frequencies from 4 MHz to 65 MHz over 1, 2, or 3 data lanes. Table 9-1 provides a few typical display resolution examples and shows the number of data lanes necessary to connect the SN65LVDS302 with the display. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate. Furthermore, the examples in the table assumes a display frame refresh rate of 60 Hz. The actual refresh rate may differ depending on the application-processor clock implementation.

Table 9-1. Typical Application Data Rates and Serial Lane Usage

DISPLAY SCREEN RESOLUTION	VISIBLE PIXEL COUNT	BLANKING OVERHEAD	DISPLAY REFRESH RATE	PIXEL CLOCK FREQUENCY [MHz]	SERIAL DATA RATE PER LANE		
					1-ChM	2-ChM	3-ChM
176x220 (QCIF+)	38,720	20%	90 Hz	4.2 MHz	125 Mbps		
240x320 (QVGA)	76,800	20%	60 Hz	5.5 MHz	166 Mbps		
640x200	128,000	20%	60 Hz	9.2 MHz	276 Mbps	138 Mbps	
352x416 (CIF+)	146,432	20%	60 Hz	10.5 MHz	316 Mbps	158 Mbps	
352x440	154,880	20%	60 Hz	11.2 MHz	335 Mbps	167 Mbps	
320x480 (HVGA)	153,600	20%	60 Hz	11.1 MHz	332 Mbps	166 Mbps	
800x250	200,000	20%	60 Hz	14.4 MHz	432 Mbps	216 Mbps	
640x320	204,800	20%	60 Hz	14.7 MHz	442 Mbps	221 Mbps	
640x480 (VGA)	307,200	20%	60 Hz	22.1 MHz		332 Mbps	221 Mbps
1024x320	327,680	20%	60 Hz	23.6 MHz		354 Mbps	236 Mbps
854x480 (WVGA)	409,920	20%	60 Hz	29.5 MHz		443 Mbps	295 Mbps

Table 9-1. Typical Application Data Rates and Serial Lane Usage (continued)

DISPLAY SCREEN RESOLUTION	VISIBLE PIXEL COUNT	BLANKING OVERHEAD	DISPLAY REFRESH RATE	PIXEL CLOCK FREQUENCY [MHz]	SERIAL DATA RATE PER LANE		
					1-ChM	2-ChM	3-ChM
800x600 (SVGA)	480,000	20%	60 Hz	34.6 MHz			346 Mbps
1024x768 (XGA)	786,432	20%	60 Hz	56.6 MHz			566 Mbps

9.2 Typical Applications

9.2.1 VGA Application

Figure 9-5 shows a possible implementation of a standard 640x480 VGA display. The LVDS301 interfaces to the SN65LVDS302, which is the corresponding receiver device to deserialize the data and drive the display driver. The pixel clock rate of 22 MHz assumes approximately 10% blanking overhead and 60 Hz display refresh rate. The application assumes 24-bit color resolution. Also shown is how the application processor provides a powerdown (reset) signal for both serializer and the display driver. The signal count over the Flexible Printed Circuit board (FPC) could be further decreased by using the standby option on the SN65LVDS302 and pulling RXEN high with a 30 kΩ resistor to V_{DD}.

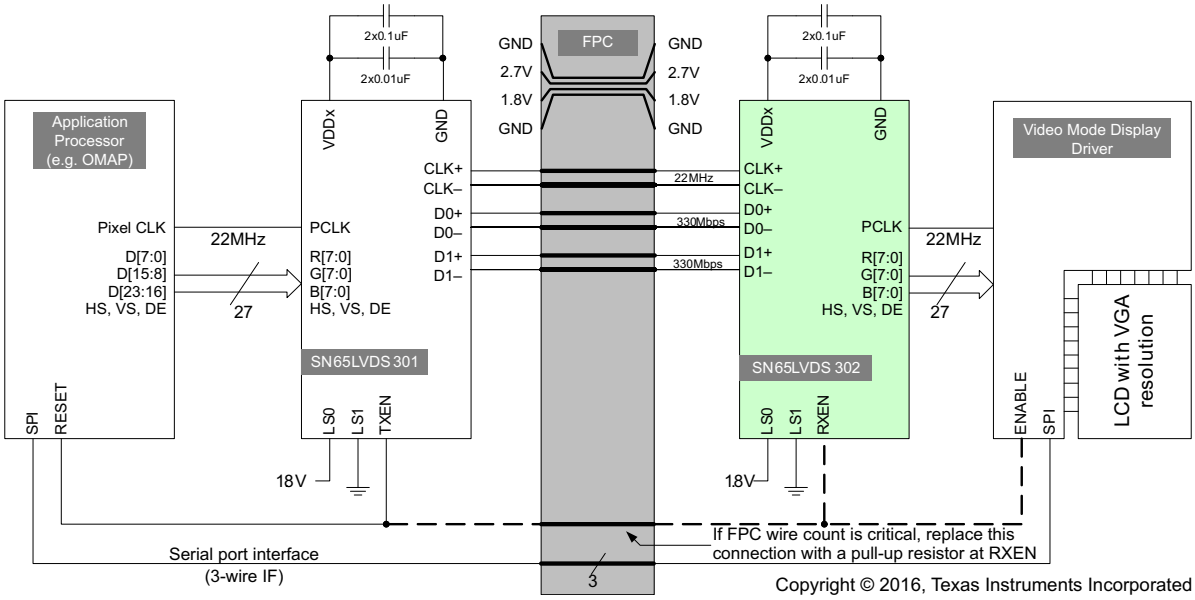


Figure 9-5. Typical VGA Display Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-2 as the input parameters.

Table 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Operating free-air temperature range	–40°C to 85°C
Supply voltages, V_{DD}, V_{DDLVDS}, V_{DDPLLA}, V_{DDPLLD}	1.65 V to 1.95 V
Magnitude of differential input voltage, V_{ID}	70 mV to 200 mV
Input voltage common mode range, V_{ICM}	0.6 V to 1.2 V
Receiver input skew, 2-channel mode	< 630 ps

9.2.1.2 Detailed Design Procedure

Configuration and Connection:

- Include a power supply capable of providing the power requirements of the whole system.
- Configure the Application Processor to transmit the RGB data at 22 MHz.
- Configure the transmitter and the SN65LVDS302 to work using two channels.
- Connect the SN65LVDS302 to the LCD display following the same color mapping. See *Section 8.3.1* for more information.

9.2.1.2.1 Power-Up and Power-Down Sequences

The SN65LVDS302 does not require a specific power up sequence for the voltage lines. However, TI recommends using the power-up and power-down sequences detailed below.

Power-up sequence (SN65LVDS301 RXEN input initially low):

1. Ramp up LCD power and SN65LVDS302 (approximately 0.5 ms to 10 ms) but keep the backlight turned off.
2. Wait for an additional 0 ms to 200 ms to ensure display noise does not occur.
3. Enable video source output; start sending black video data.
4. Toggle SN65LVDS301 TXEN = V_{IH}.
5. Toggle SN65LVDS302 RXEN = V_{IH}.
6. Send at least 1 ms of black video data. This allows the SN65LVDS301 to be phase locked, and the display to show black data first.
7. Start sending true image data.
8. Enable backlight.

Power-down sequence (SN65LVDS301 RXEN input initially high):

1. Disable LCD backlight and wait for the minimum time specified in the LCD datasheet for the backlight to go low.
2. Switch the video source output from active video data to black image data (all visible pixels turn black) for at least 2 frame times.
3. Set SN65LVDS301 TXEN = GND and wait for 250 ns.
4. Set SN65LVDS302 RXEN = GND and wait for 250 ns.
5. Disable the video output of the video source.
6. Remove power from the LCD panel for lowest system power.

9.2.1.3 Application Curves

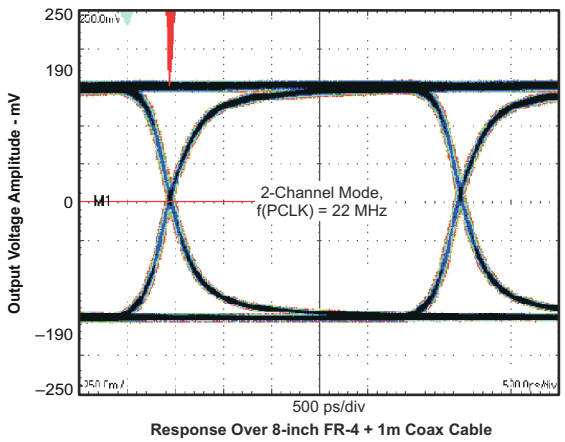


Figure 9-6. VGA 2-Channel Output Waveform

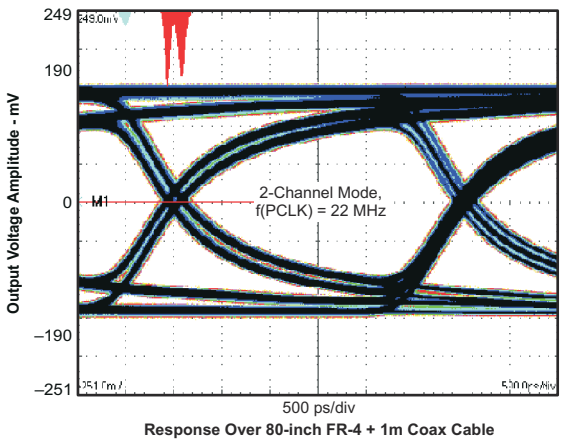


Figure 9-7. VGA 2-Channel Output Waveform

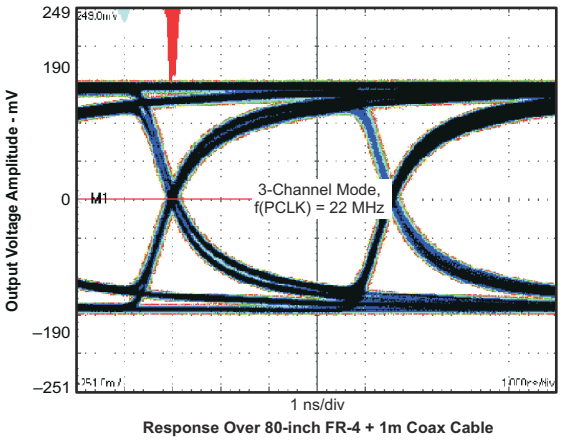


Figure 9-8. VGA3-Channel Output Waveform

9.2.2 Dual LCD-Display Application

The example in Figure 9-9 shows a possible application setup driving two video-mode displays from one application processor. The data rate of 330 Mbps at a pixel clock rate of 5.5 MHz corresponds to a 320x240 QVGA resolution at 60 Hz refresh rate and 10% blanking overhead.

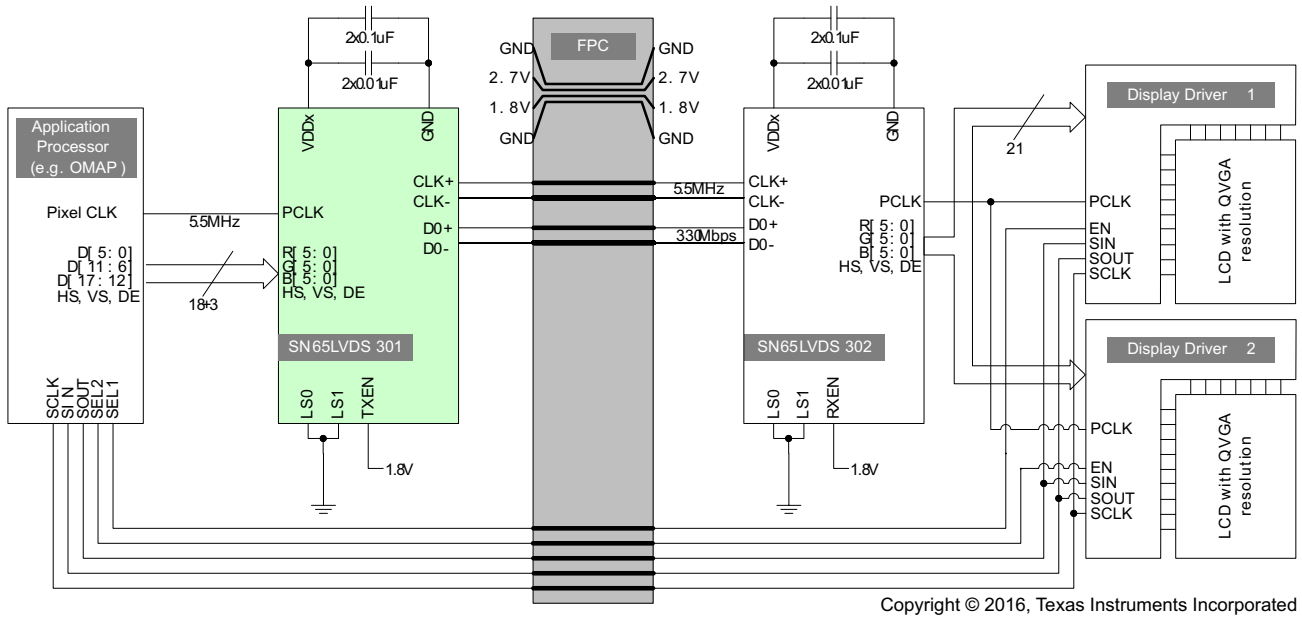


Figure 9-9. Example Dual-QVGA Display Application

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-3 as the input parameters.

Table 9-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Operating free-air temperature range	–40°C to 85°C
Supply voltages, V_{DD}, V_{DDLVDS}, V_{DDPLLA}, V_{DDPLLD}	1.65 V to 1.95 V
Magnitude of differential input voltage, V_{ID}	70 mV to 200 mV
Input voltage common mode range, V_{ICM}	0.6 V to 1.2 V
Receiver input skew, 1-channel mode	< 630 ps

9.2.2.2 Application Curve

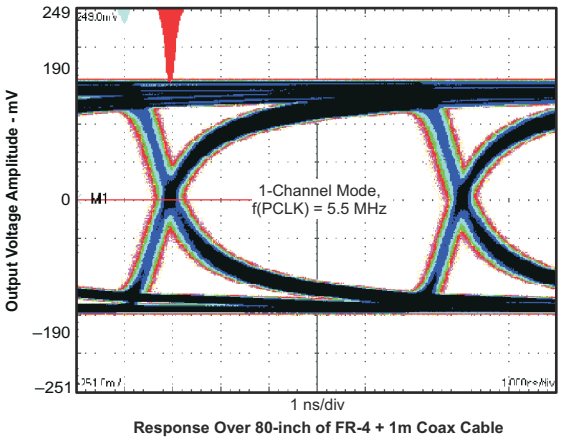


Figure 9-10. QVGA Output Waveform

10 Power Supply Recommendations

To minimize the power supply noise floor, provide good decoupling near the SN65LVDS302 power pins. TI recommends placing one 0.01-µF ceramic capacitor at each power pin, and two 0.1-µF ceramic capacitors on each power node. The distance between the SN65LVDS302 and capacitors must be minimized to reduce loop inductance and provide optimal noise filtering. Placing the capacitor underneath the SN65LVDS302 on the bottom of the PCB is often a good choice. A 100-pF ceramic capacitor can be put at each power pin to optimize the EMI performance.

11 Layout

11.1 Layout Guidelines

Use chamfered corners (45° bends) instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bend is seen as a smaller discontinuity.

When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.

Avoid metal layers and traces underneath or between the pads of the LVDS connectors for better impedance matching. Otherwise they cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.

Use solid power and ground planes for 100 Ω impedance control and minimum power noise.

For a multilayer PCB, TI recommends keeping one common GND layer underneath the device and connect all ground terminals directly to this plane. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.

Keep the trace length as short as possible to minimize attenuation.

Place bulk capacitors (10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.

12 Device and Documentation Support

12.1 Community Resource

12.2 Trademarks

FlatLink™ is a trademark of Texas Instruments.
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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS302ZXH	ACTIVE	NFBGA	ZXH	80	576	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS302	Samples
SN65LVDS302ZXHR	ACTIVE	NFBGA	ZXH	80	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS302	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

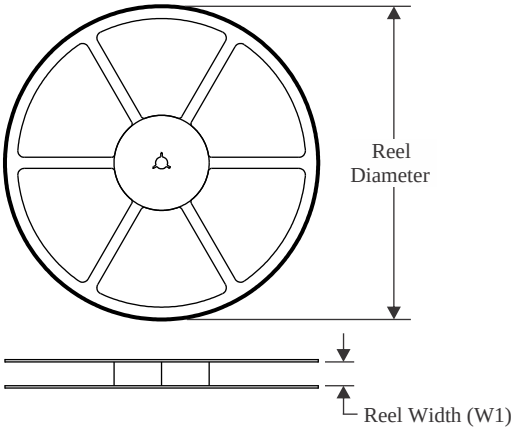
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

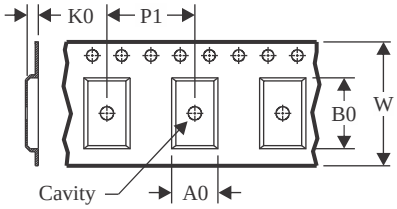
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

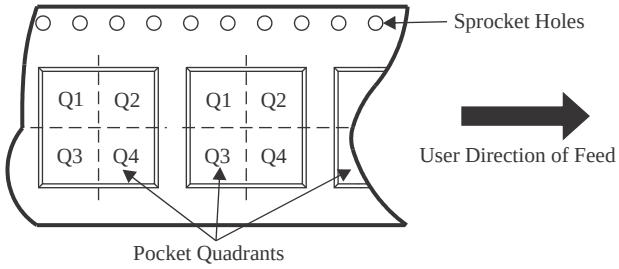


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

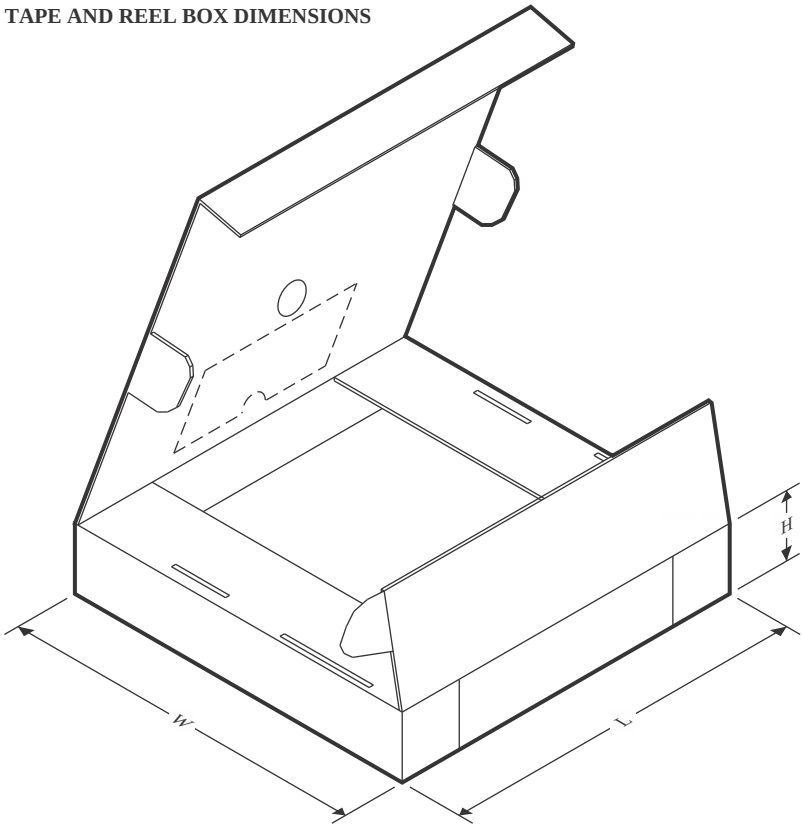
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS302ZXHR	NFBGA	ZXH	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

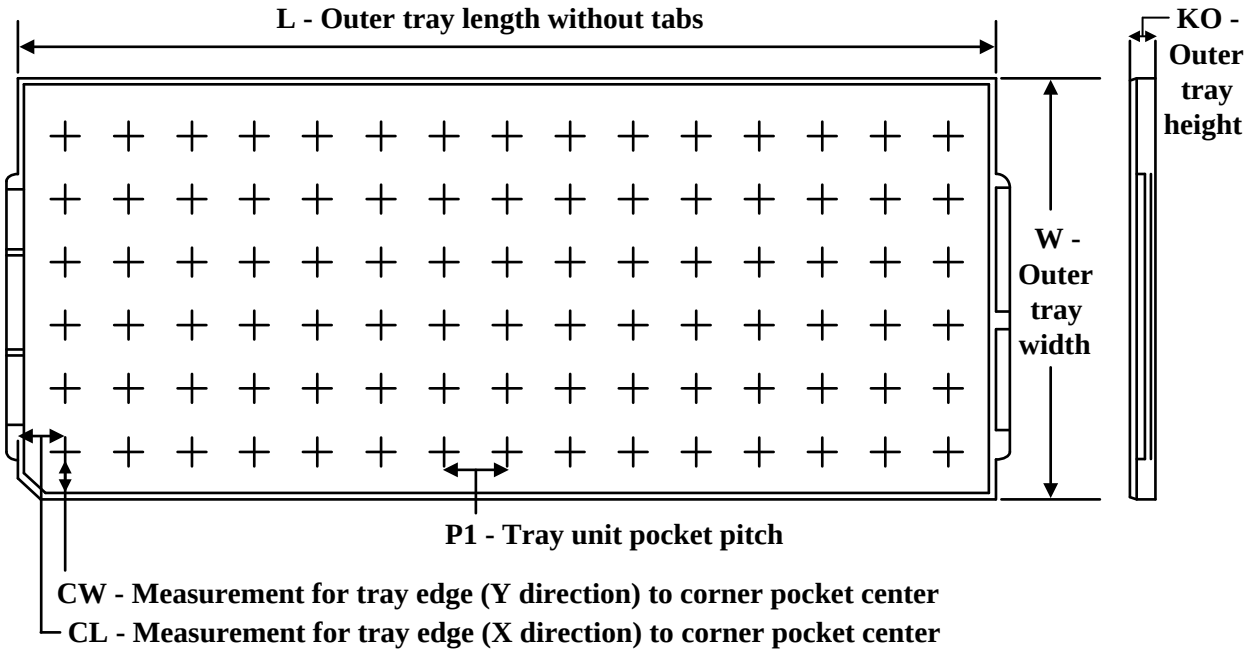
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS302ZXHR	NFBGA	ZXH	80	2500	336.6	336.6	31.8

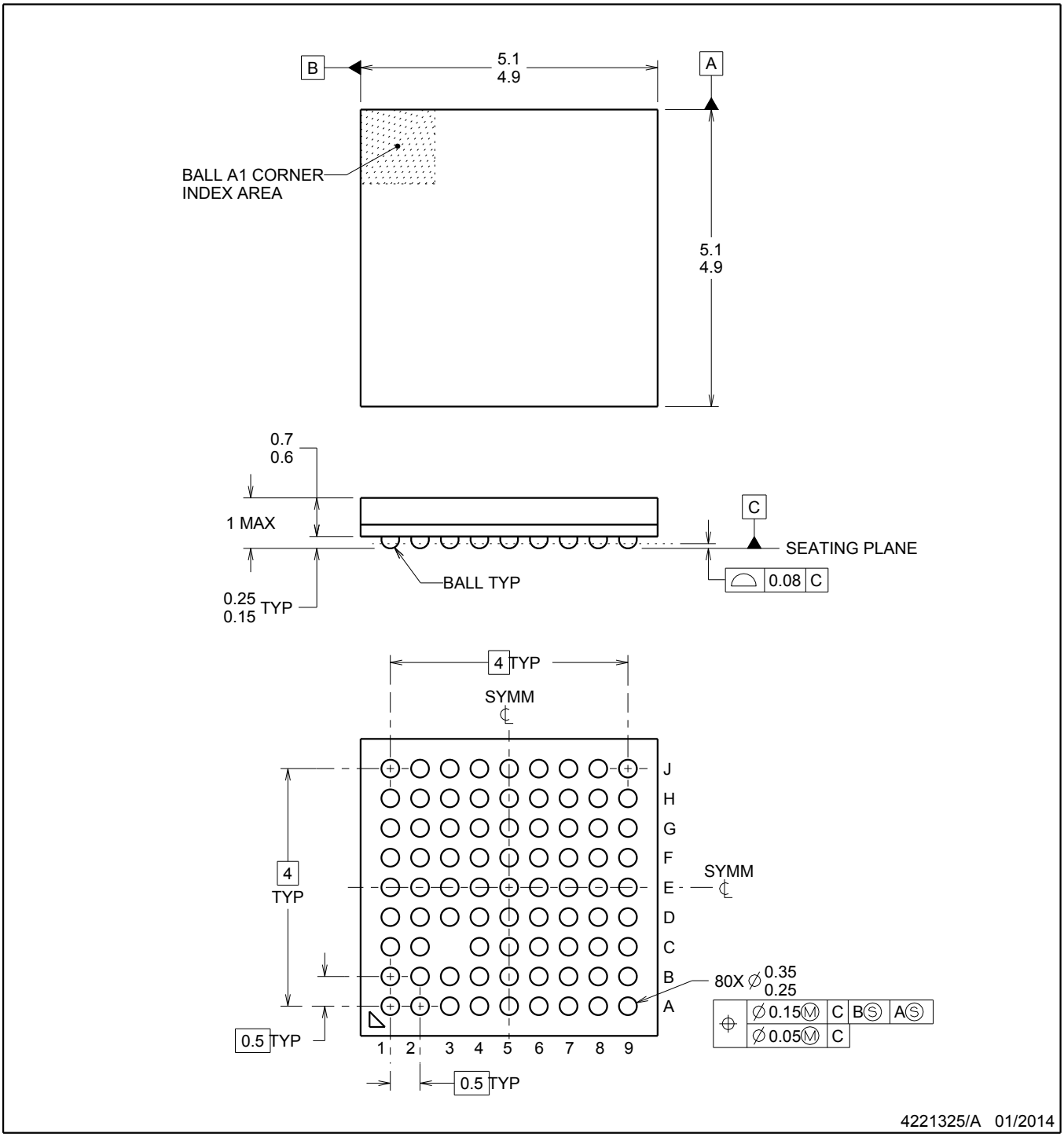
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

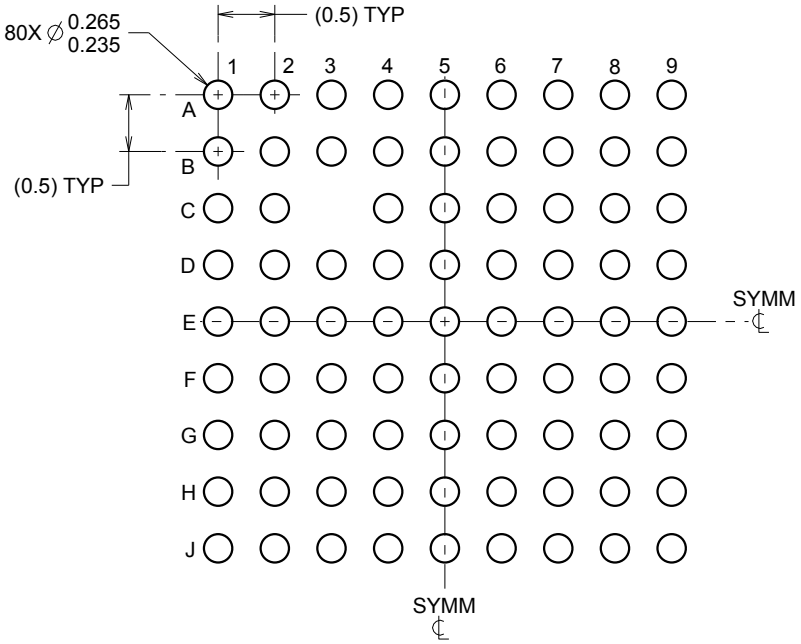
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN65LVDS302ZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7

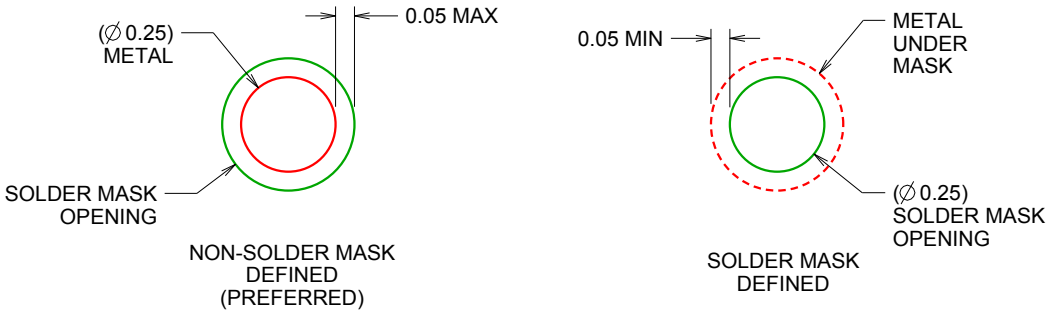


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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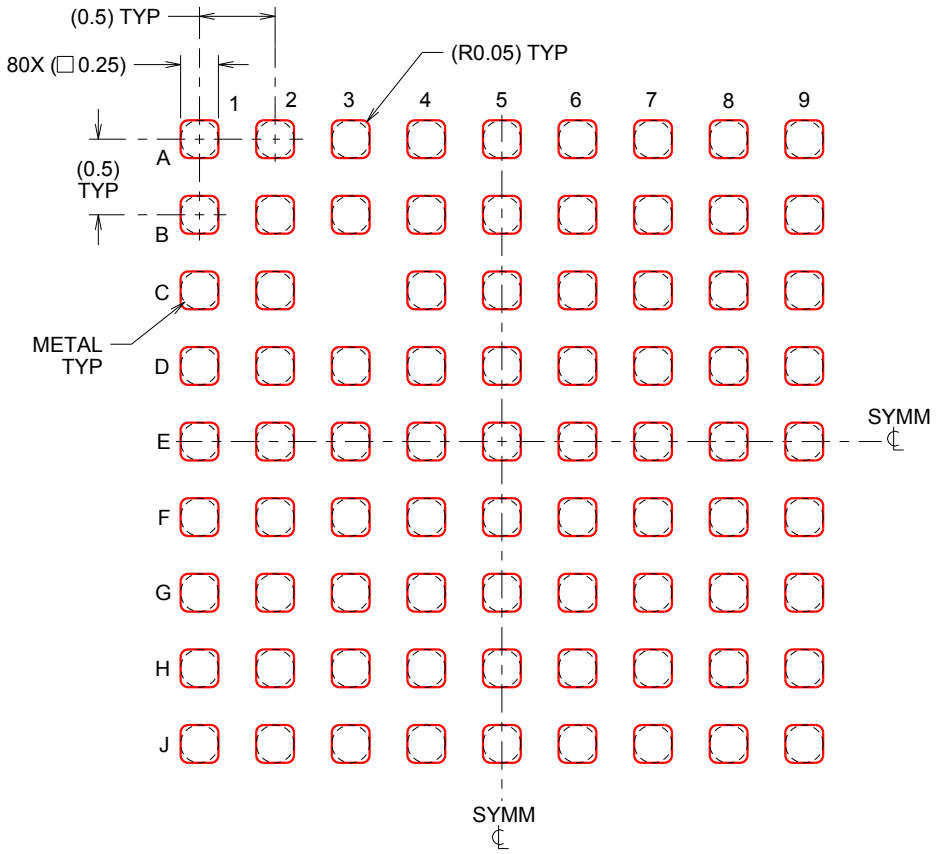
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221325/A 01/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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