

FEATURES

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- J and \bar{K} Inputs to First Stage
- Complementary Outputs From Last Stage
- Package Options: Plastic and Ceramic DIPS and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

DESCRIPTION/ORDERING INFORMATION

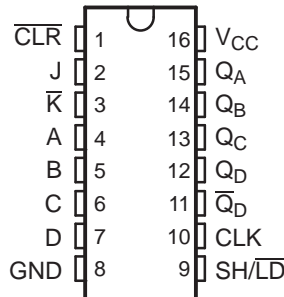
These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load, and shift (in the direction Q_A and Q_D).

Parallel loading is accomplished by applying the 4-bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

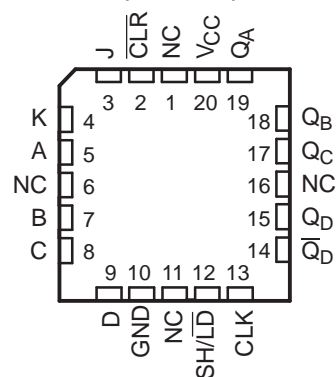
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs permit the first stage to perform as a J- \bar{K} , D, or T type flip-flop as shown in the function table.

The SN54HC195 is characterized for operation over the full military temperature range of -55°C to 125°C .

SN54HC195 . . . J PACKAGE
(TOP VIEW)

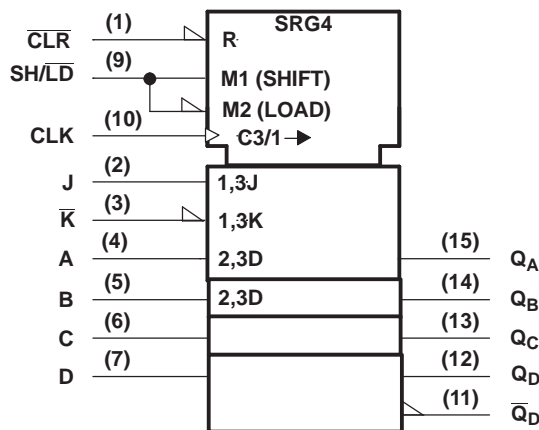


SN54HC195 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

LOGIC SYMBOL†



† This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617–12.

Pin numbers shown are for J package.

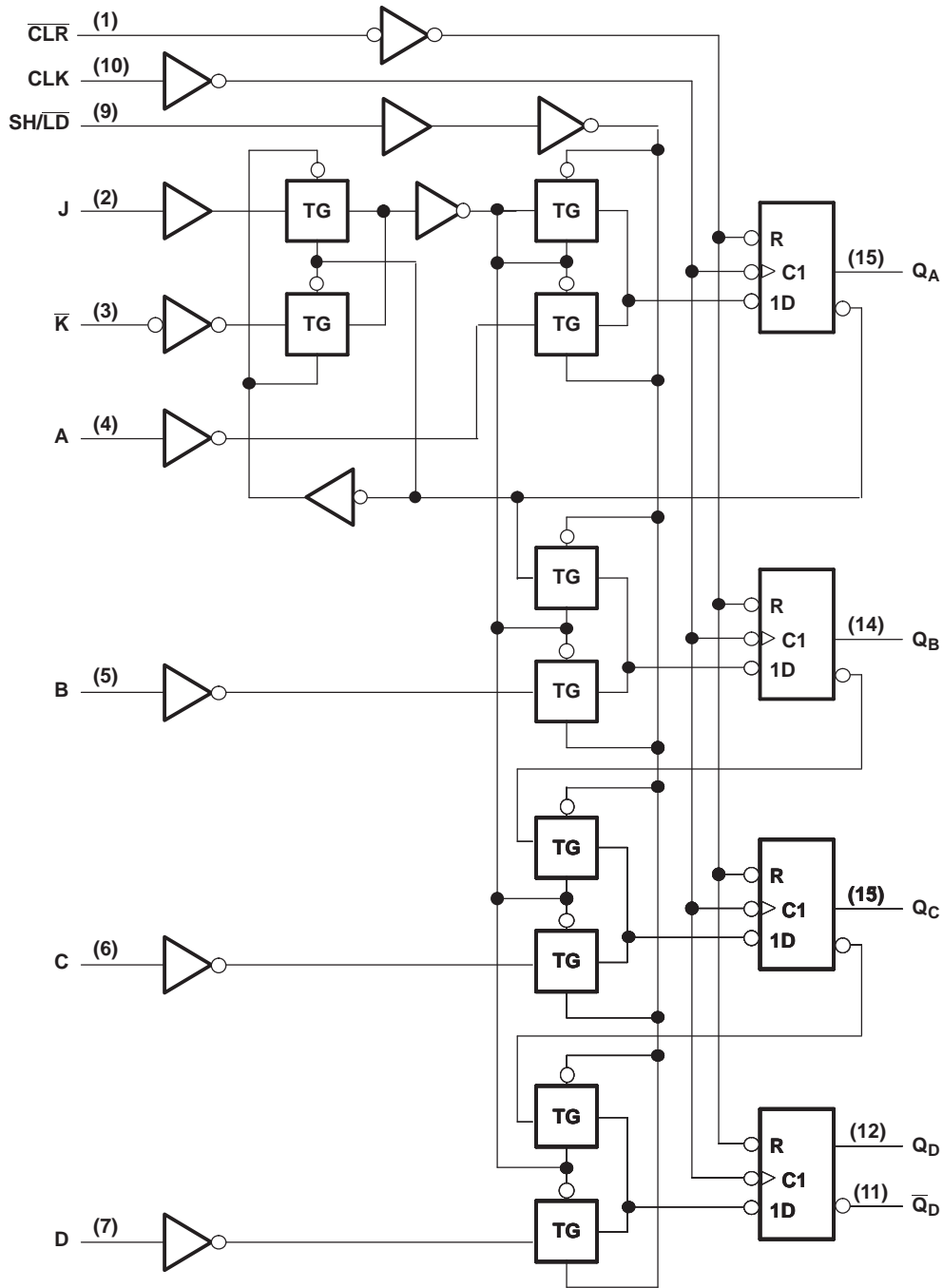


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54HC195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

SCLS124A—DECEMBER 1992—REVISED NOVEMBER 2007

LOGIC DIAGRAM (POSITIVE LOGIC)

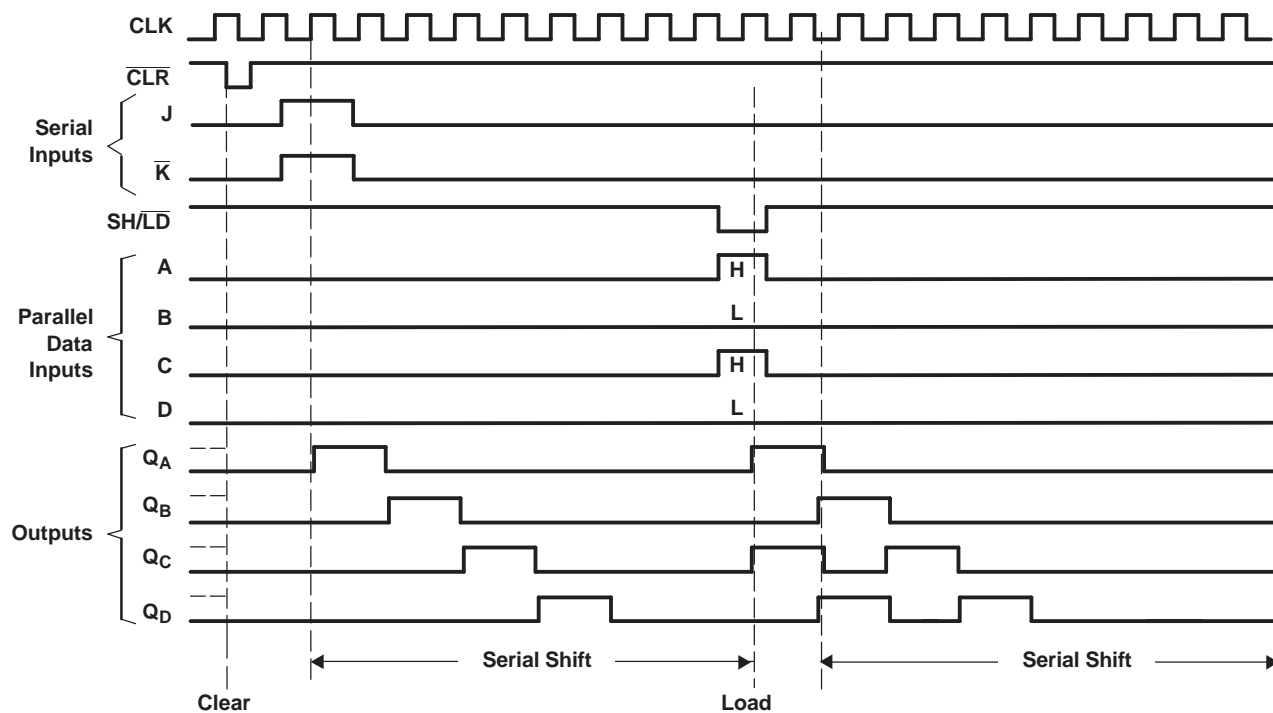


Pin numbers shown are for J package.

FUNCTION TABLE

CLR	SH/LD	CLK	INPUTS						OUTPUTS				
			SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D	Q̄ _D
			J	K̄	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d̄
H	H	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q̄ _{D0}
H	H	↑	L	H	X	X	X	X	Q _{A0}	Q _{A0}	Q _{Bn}	Q _{Cn}	Q̄ _{Cn}
H	H	↑	L	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q̄ _{Cn}
H	H	↑	H	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q̄ _{Cn}
H	H	↑	H	L	X	X	X	X	Q̄ _{An}	Q _{An}	Q _{Bn}	Q _{Cn}	Q̄ _{Cn}

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



SN54HC195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

SCLS124A–DECEMBER 1992–REVISED NOVEMBER 2007

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
I_{IK}	Input clamp current $V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I_{OK}	Output clamp current $V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current $V_O = 0$ to V_{CC}		25	mA
	Continuous current through V_{CC} or GND pins		50	mA
	Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package		300	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package		260	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT	
V_{CC}	Supply voltage	2	5	6	V	
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	V	
		$V_{CC} = 4.5$ V		3.15		
		$V_{CC} = 6$ V		4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	V	
		$V_{CC} = 4.5$ V		0		
		$V_{CC} = 6$ V		0		
V_I	Input voltage	0		V_{CC}	V	
V_O	Output voltage	0		V_{CC}	V	
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V		0	1000	ns
		$V_{CC} = 4.5$ V		0	500	
		$V_{CC} = 6$ V		0	400	
T_A	Operating free-air temperature	-55		125	°C	

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC195		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9	V	
		4.5 V	4.4	4.499		4.4		
		6 V	5.9	5.999		5.9		
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7		
		6 V	5.48	5.80		5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1	0.1	V	
		4.5 V		0.001	0.1	0.1		
		6 V		0.001	0.1	0.1		
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26	0.4		
		6 V		0.15	0.26	0.4		
I_I	$V_I = V_{CC}$ or 0	6 V		± 0.1	± 100	± 1000	nA	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8	160	μA	
C_I	$V_I = V_{CC}$ or GND	2 V to 6 V		3	10	10	pF	

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	$T_A = 25^\circ\text{C}$		SN54HC195		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.2	MHz
		4.5 V	0	31	0	21	
		6 V	0	36	0	25	
t_w	Pulse duration	CLK high or low		2 V	80	120	ns
				4.5 V	16	24	
				6 V	14	20	
	$\overline{\text{CLR}}$ low		2 V	80	120		
			4.5 V	16	24		
			6 V	14	20		
t_{su}	Setup time, before CLK \uparrow	SH/ $\overline{\text{LD}}$, or serial and parallel data, or CLR inactive		2 V	100	150	ns
				4.5 V	20	30	
				6 V	17	26	
t_h	Hold time, after CLK \uparrow	SH/ $\overline{\text{LD}}$, or serial and parallel data, or CLR inactive		2 V	0	0	ns
				4.5 V	0	0	
				6 V	0	0	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50 \text{ pF}^{(1)}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC195		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			2 V	6	12		4.2	MHz	
			4.5 V	31	50		21		
			6 V	36	60		25		
t_{pd}	CLK	Q_A thru Q_D or \overline{Q}_D	2 V		67	145		220	ns
			4.5 V		17	29		44	
			6 V		14	25		37	
t_{pd}	$\overline{\text{CLR}}$	Q_A thru Q_D or \overline{Q}_D	2 V		67	150		225	ns
			4.5 V		17	30		45	
			6 V		13	26		38	
t_t		Any	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	
C_{pd}	Power dissipation capacitance			No load, $T_A = 25^\circ\text{C}$				65 pF typ	

(1) Load circuit and voltage waveforms are shown in previous pages.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8682701EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8682701EA SNJ54HC195J	Samples
SN54HC195J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC195J	Samples
SNJ54HC195J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8682701EA SNJ54HC195J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated