SDAS069B - DECEMBER 1982 - REVISED DECEMBER 1994

- Two-Way Asynchronous Communication Between Data Buses
- pnp Inputs Reduce dc Loading
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

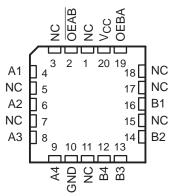
description

These quadruple bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEBA and OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneously enabling OEBA and OEAB. Each output reinforces its input in this transceiver configuration. When both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (eight in all) retain their states. The 4-bit codes appearing on the two sets of buses are identical.

SN54ALS243A J PACKAGE SN74ALS243A D OR N PACKAGE (TOP VIEW)									
OEAB [NC [A1 [A2 [A3 [A4 [GND [1 2 3 4 5 6 7	14 13 12 11 10 9 8	V _{CC} OEBA NC B1 B2 B3 B4						
	1	°	1 04						

SN54ALS243A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN54ALS243A is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74ALS243A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE										
INP	UTS									
OEAB	OEBA	FUNCTION								
L	L	A to B								
Н	Н	B to A								
Н	L	Isolation								
L	н	Latch A and B (A = B)								

FUNCTION TABLE

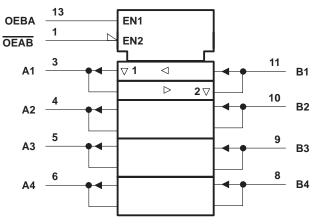
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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logic symbol[†]



 $\overline{OEAB} \xrightarrow{1} 0EBA$ $A1 \xrightarrow{3} 13 0EBA$ $A1 \xrightarrow{11} B1$ $A2 \xrightarrow{4} 10 B2$

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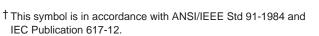
- B3

8 B4

logic diagram (positive logic)

A3 —

A4 _____



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC}		
Input voltage, VI: All inputs		
Operating free-air temperature range, T _A :	SN54ALS243A	 –55°C to 125°C
	SN74ALS243A	 0°C to 70°C
Storage temperature range		 –65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN	54ALS24	3A	SN74ALS243A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			-12			-15	mA
IOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

						3A	SN7				
	PARAMETER	TEST CO	NDITIONS				TYP [†]	MAX	UNIT		
VIK		V _{CC} = 4.5 V,	lj = – 18 mA			-1.2			-1.2	V	
		V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	V _{CC} -2	2		V _{CC} -2	2			
			$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V	
VOH		V _{CC} = 4.5 V	$I_{OH} = -12 \text{ mA}$	2						V	
			I _{OH} = – 15 mA				2				
			I _{OL} = 12 mA		0.25	0.4		0.25	0.4	v	
VOL		V _{CC} = 4.5 V	I _{OL} = 24 mA				0.35		0.5	v	
1.	Control inputs		$V_{I} = 7 V$			0.1			0.1		
Ιį	A or B ports	V _{CC} = 5.5 V	VI = 5.5 V			0.1			0.1	mA	
	Control inputs		V 07V			20			20		
ΊΗ	A or B ports‡	V _{CC} = 5.5 V,	V _I = 2.7 V		20				20 ^{µ/}	μA	
1	Control inputs		Nr. 0.4.V			-0.1			-0.1		
ΊL	A or B ports‡	V _{CC} = 5.5 V,	V _I = 0.4 V		-0.1				-0.1	mA	
ΙΟ§		$V_{CC} = 5.5 V,$	V _O = 2.25 V	-20		-112	-30		-112	mA	
			Outputs high		15	30		15	25		
ICC		$V_{CC} = 5.5 V$	Outputs low		20	35		20	30	mA	
			Outputs disabled		21	37		21	32		

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. [‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX¶					
			SN54AL	S243A	SN74AL	S243A			
			MIN	MAX	MIN	MAX			
^t PLH	A as D	Der	4	15	4	11	ns		
^t PHL	A or B	B or A	4	15	4	11			
^t PZH	0545	_	7	25	7	20			
^t PZL	OEAB	В	7	25	7	20	ns		
^t PHZ	0540			16	2	14			
^t PLZ	OEAB	В	3	27	3	22	ns		
^t PZH	0.55.4		7	25	7	20			
^t PZL	OEBA	А	7	25	7	20	ns		
^t PHZ		٨	2	16	2	14			
^t PLZ	OEBA	A	3	27	3	22	ns		

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES 7 V $R_{L} = R1 = R2$ Vcc Ç **S**1 ≶ RL **R1** From Output Test From Output Test From Output Test Point **Under Test Under Test** Point Point **Under Test** Cı 5 CL Rı **R2** CL (see Note A) (see Note A) (see Note A) LOAD CIRCUIT FOR LOAD CIRCUIT LOAD CIRCUIT **BI-STATE TOTEM-POLE OUTPUTS** FOR OPEN-COLLECTOR OUTPUTS FOR 3-STATE OUTPUTS 3.5 V 3.5 V Timing **High-Level** 1.3 V 1.3 V 1.3 V Input Pulse 0.3 V 0.3 V th t_{su} 3.5 V 3.5 V Data Low-Level 131 1.3 V 3 v .3 V Input Pulse 0.3 V 0.3 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PULSE DURATIONS SETUP AND HOLD TIMES 3.5 V Output Control 1.3 V 1.3 V (low-level , enabling) 0.3 V 3.5 V ^tPZL 1.3 V 1.3 V Input ^tPLZ 0.3 V ≈3.5 V Waveform 1 ^tPHL **t**PLH 1.3 \ S1 Closed VOH In-Phase (see Note B) 1.3 V 1.3 V VOL Output VOL 0.3 V tphz 🕩 ^tPLH tpzh 🔶 tPHL -VOH VOH Waveform 2 Out-of-Phase 1.3 V S1 Open 0.3 V 1.3 V 1.3 V Output VOL (see Note B) (see Note C) 0 V

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{f} = t_{f} = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
84013022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84013022A SNJ54ALS 243AFK	Samples
SNJ54ALS243AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84013022A SNJ54ALS 243AFK	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
84013022A	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54ALS243AFK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK 20

8.89 x 8.89, 1.27 mm pitch

GENERIC PACKAGE VIEW

LCCC - 2.03 mm max height

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





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