

SNx4AHC86 Quadruple 2-Input Exclusive-OR Gates

1 Features

- Operating range 2-V to 5.5-V V_{CC}
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22
 - 2000-V human-body model (A114-A)
 - 200-V machine model (A115-A)
 - 1000-V charged-device model (C101)

2 Applications

- [Detect phase differences in input signals](#)
- Create a selectable inverter or buffer

3 Description

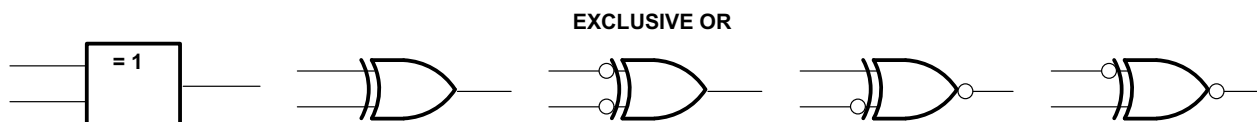
The SNx4AHC86 devices are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true or complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

Device Information

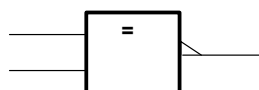
PART NUMBER	RATING	PACKAGE ⁽¹⁾
SN74AHC86	Commercial	BQA (WQFN, 14)
		D (SOIC, 14)
		DB (SSOP, 14)
		DGV (TVSOP, 14)
		N (PDIP, 14)
		NS (SOP, 14)
		PW (TSSOP, 14)
SN54AHC86	Military	RGY (VQFN, 14)
		J (CDIP, 14)
		W (CFP, 14)
		FK (LCCC, 20)

(1) For all available packages, see the orderable addendum at the end of the data sheet.



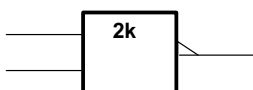
These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



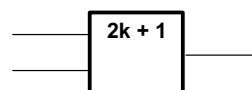
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

Exclusive-OR Logic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (May 2013) to Revision K (July 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added the <i>Device Information</i> table.....	1
• Added the <i>Device and Documentation Support</i> sections.....	9
• Added the <i>Mechanical, Packaging, and Orderable Information</i> sections.....	9

Changes from Revision I (July 2003) to Revision J (May 2013)	Page
• Changed document format from Quicksilver to DocZone.....	1
• Extended operating temperature range to 125°C.....	4

5 Pin Configuration and Functions

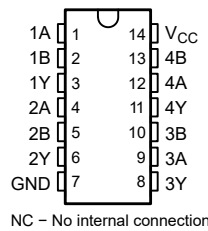


Figure 5-1. SN54AHC86 J or W Package, SN74AHC86 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)

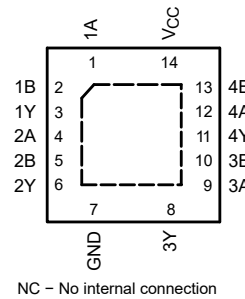


Figure 5-2. SN74AHC86 RGY Package, VQFN 14-Pin (Top View)

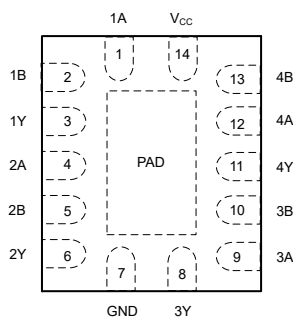


Figure 5-3. SN74AHC86 BQA Package, WQFN 14-Pin (Top View)

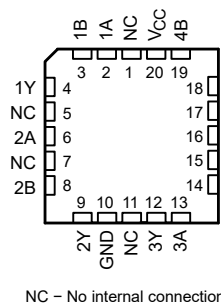


Figure 5-4. SN54AHC86 FK Package, LCCC 20-Pin (Top View)

Table 5-1. Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	D, DB, DGV, N, NS, PW, RGY, J, W, or BQA	FK		
1A	1	2	I	Channel 1, Input A
1B	2	3	I	Channel 1, Input B
1Y	3	4	O	Channel 1, Output Y
2A	4	6	I	Channel 2, Input A
2B	5	8	I	Channel 2, Input B
2Y	6	9	O	Channel 2, Output Y
GND	7	10	G	Ground
3Y	8	12	O	Channel 3, Output Y
3A	9	13	I	Channel 3, Input A
3B	10	14	I	Channel 3, Input B
4Y	11	16	O	Channel 4, Output Y
4A	12	18	I	Channel 4, Input A
4B	13	19	I	Channel 4, Input B
V _{CC}	14	20	P	Positive Supply
NC	—	1, 5, 7, 11, 15, 17	—	Not internally connected
Thermal pad ⁽²⁾			—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, G = ground, P = power.

(2) BQA package only

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	VALUE	UNIT
Supply voltage range, V_{CC}	-0.5 to 7	V
Input voltage range, V_I ⁽²⁾	-0.5 to 7	V
Output voltage range, V_O ⁽²⁾	-0.5 to $V_{CC} + 0.5$	V
Input clamp current, I_{IK} ($V_I < 0$)	-20	mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20	mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25	mA
Continuous current through V_{CC} or GND	± 50	mA
Storage temperature range, T_{stg}	-65 to 150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Recommended Operating Conditions

		SN54AHC86		SN74AHC86		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V
		$V_{CC} = 3\text{ V}$	2.1	2.1		
		$V_{CC} = 5.5\text{ V}$	3.85	3.85		
V_{IL}	Low-level Input voltage	$V_{CC} = 2\text{ V}$		0.5	0.5	V
		$V_{CC} = 3\text{ V}$		0.9	0.9	
		$V_{CC} = 5.5\text{ V}$		1.65	1.65	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	-4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	-8	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	20	
T_A	Operating free-air temperature	-55	125	-40	125	°C

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		D ⁽²⁾	DB ⁽²⁾	DGV ⁽²⁾	N ⁽²⁾	NS ⁽²⁾	PW ⁽²⁾	RGY ⁽³⁾	BQA	UNIT
		SOIC	SSOP	TVSOP	PDIP	SOP	TSSOP	VQFN	WQFN	
		14	14	14	14	14	14	14	14	
R _{θJA}	Junction-to-ambient thermal resistance	86	96	127	80	76	113	47	88.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.
- (3) The package thermal impedance is calculated in accordance with JESD 51-5

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
					SN54AHC86		SN74AHC86		SN74AHC86		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2	1.9		1.9		1.9		V
		3 V	2.9	3	2.9		2.9		2.9		
		4.5 V	4.4	4.5	4.4		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58		2.48		2.48		2.48		
		4.5 V	3.94		3.8		3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V		0.1		0.1		0.1		0.1	V
		3 V		0.1		0.1		0.1		0.1	
		4.5 V		0.1		0.1		0.1		0.1	
	I _{OH} = 4 mA	3 V		0.36		0.5		0.44		0.5	
		4.5 V		0.36		0.5		0.44		0.5	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V		±0.1		±1 ⁽¹⁾		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		2		20		20		20	μA
C _i	V _I = V _{CC} or GND	5 V		4	10			10			pF

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

6.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C		T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
						SN54AHC86		SN74AHC86		SN74AHC86		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	7 ⁽¹⁾	11 ⁽¹⁾	1 ⁽¹⁾	13 ⁽¹⁾	1	13	1	13	ns
t _{PHL}				7 ⁽¹⁾	11 ⁽¹⁾	1 ⁽¹⁾	13 ⁽¹⁾	1	13	1	13	
t _{PLH}	A or B	Y	C _L = 50 pF	9.5	14.5	1	16.5	1	16.5	1	16.5	ns
t _{PHL}				9.5	14.5	1	16.5	1	16.5	1	16.5	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
						SN54AHC86		SN74AHC86		Recommended		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$	4.8 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8	ns
t_{PHL}				4.8 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	6.3	8.8	1	10	1	10	1	10	ns
t_{PHL}				6.3	8.8	1	10	1	10	1	10	

6.7 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74AHC86			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.3		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

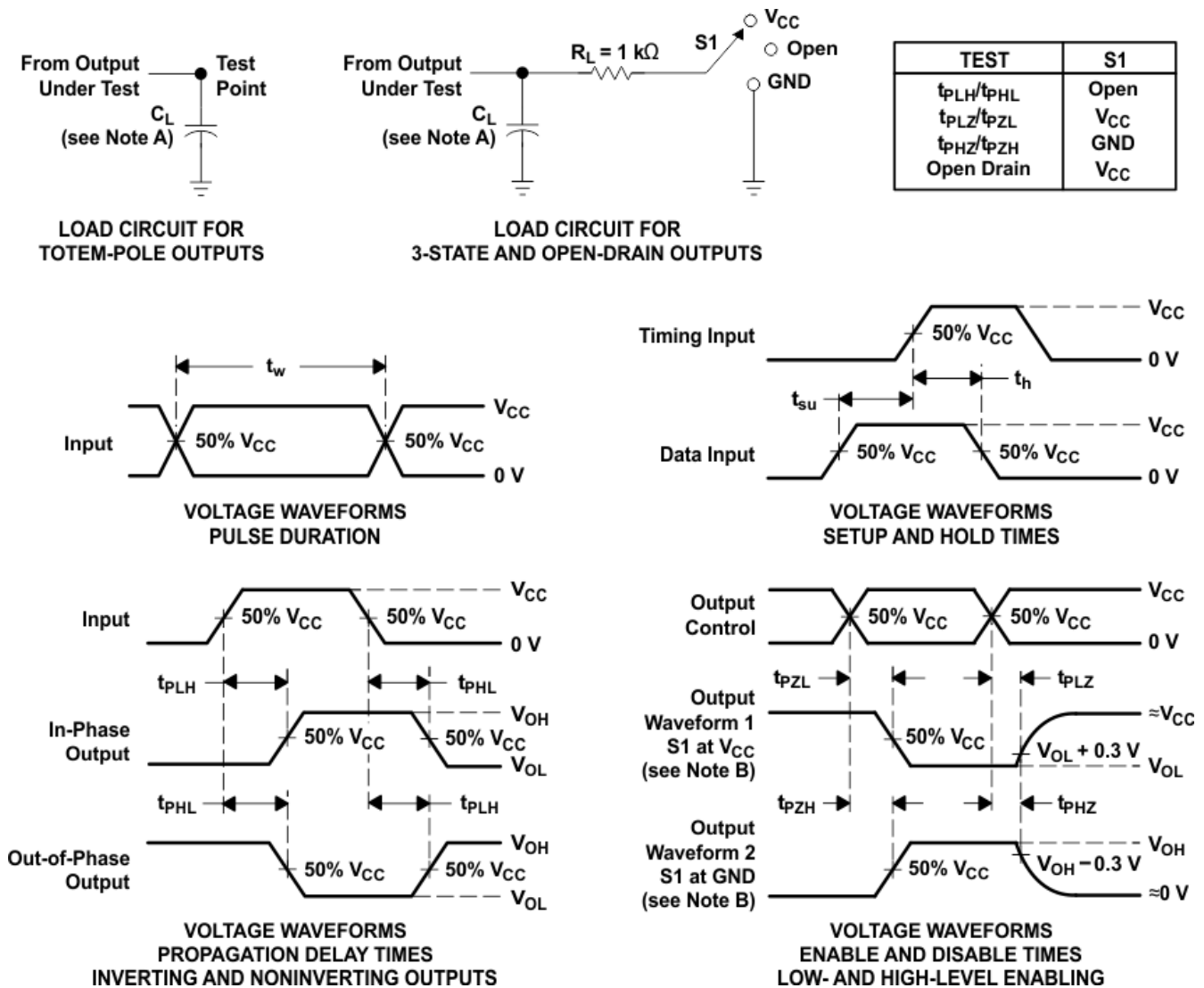
(1) Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	18	pF

7 Parameter Measurement Information



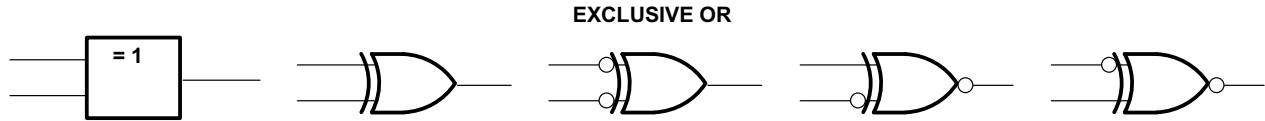
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

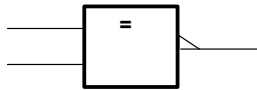
8.1 Functional Block Diagram

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



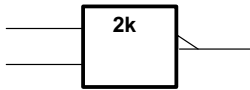
These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



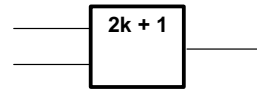
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

Figure 8-1. Exclusive-OR Logic

8.2 Device Functional Modes

**Table 8-1. Function Table
(Each Gate)**

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9681601Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9681601Q2A SNJ54AHC 86FK	Samples
5962-9681601QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681601QC A SNJ54AHC86J	Samples
5962-9681601QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681601QD A SNJ54AHC86W	Samples
SN74AHC86BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86	Samples
SN74AHC86DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86	Samples
SN74AHC86DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86	Samples
SN74AHC86DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86	Samples
SN74AHC86N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC86N	Samples
SN74AHC86NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86	Samples
SN74AHC86PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86	Samples
SN74AHC86PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86	Samples
SN74AHC86RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA86	Samples
SNJ54AHC86FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9681601Q2A SNJ54AHC 86FK	Samples
SNJ54AHC86J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681601QC A SNJ54AHC86J	Samples
SNJ54AHC86W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681601QD A SNJ54AHC86W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC86, SN74AHC86 :

● Catalog : [SN74AHC86](#)

● Military : [SN54AHC86](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC86BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC86DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC86DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC86NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC86RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC86BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC86DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC86DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC86DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC86NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC86PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC86RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

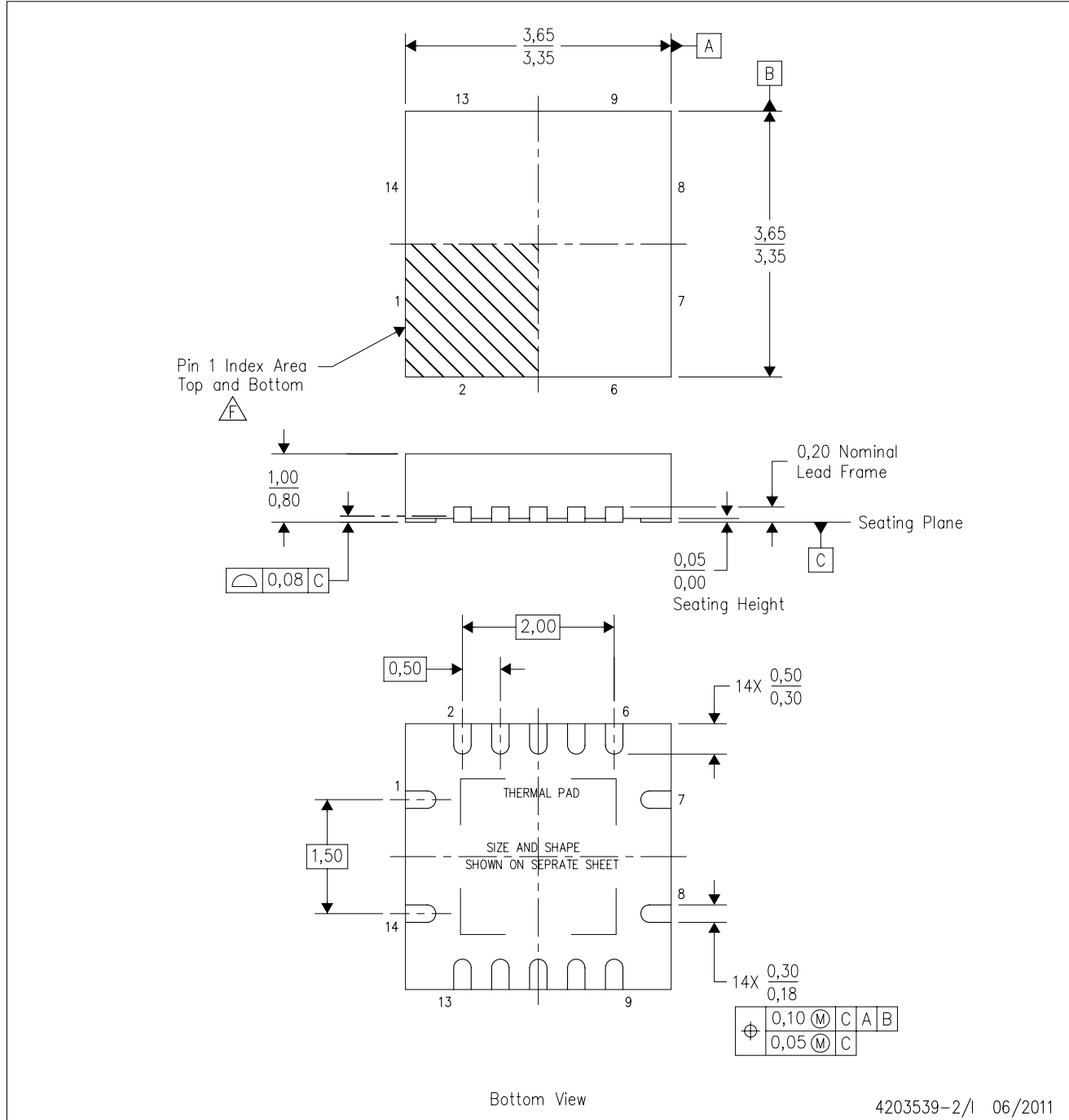
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9681601Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9681601QDA	W	CFP	14	1	506.98	26.16	6220	NA
SN74AHC86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC86N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC86FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54AHC86W	W	CFP	14	1	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

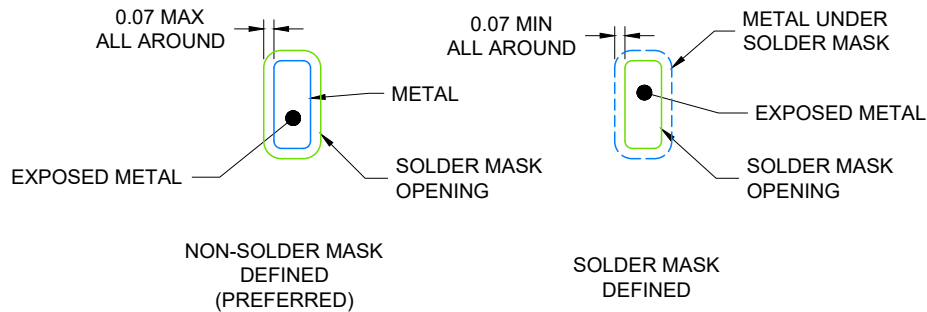
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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