SMx320VC33 Digital Signal Processor

1 Features

- High-Performance Floating-Point Digital Signal Processor (DSP)
  - SMx320VC33-150
    - 13-ns Instruction Cycle Time
    - 150 Million Floating-Point Operations per Second (MFLOPS)
    - 75 Million Instructions per Second (MIPS)
- 34K × 32-Bit (1.1-Mbit) On-Chip Words of Dual-Access Static Random-Access Memory (SRAM) Configured in 2 × 16K plus 2 × 1K Blocks to Improve Internal Performance
- x5 Phase-Locked Loop (PLL) Clock Generator
- Very-Low Power: <200 mW at 150 MFLOPS
- 32-Bit High-Performance CPU
- 16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations
- Four Internally Decoded Page Strobes to Simplify Interface to I/O and Memory Devices
- Boot-Program Loader
- EDGEMODE Selectable External Interrupts
- 32-Bit Instruction Word, 24-Bit Addresses
- Eight Extended-Precision Registers
- Fabricated Using the 0.18-µm (l_{eff} – Effective Gate Length) TImeline™ Technology by Texas Instruments
- On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1 (JTAG)
- On-Chip Memory-Mapped Peripherals:
  - One Serial Port
  - Two 32-Bit Timers
  - Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation
- 164-Pin Low-Profile Quad Flatpack (HFG Suffix)
- 144-Pin Non-Hermetic Ceramic Ball Grid Array (CBGA) (GNM Suffix)
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Two Low-Power Modes
- Two- and Three-Operand Instructions
- Parallel Arithmetic/Logic Unit (ALU) and Multiplier Execution in a Single Cycle
- Block-Repeat Capability
- Zero-Overhead Loops With Single-Cycle Branches
- Conditional Calls and Returns
- Interlocked Instructions for Multiprocessing Support
- Bus-Control Registers Configure Strobe-Control Wait-State Generation
- 1.8-V (Core) and 3.3-V (I/O) Supply Voltages

2 Description

The SMx320VC33 DSP is a 32-bit, floating-point processor manufactured in 0.18-µm four-level-metal CMOS (TImeline) technology. The SMx320VC33 is part of the SM320C3x™ generation of DSPs from Texas Instruments.

The SM320C3x internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 150 MFLOPS. The SMx320VC33 optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

The SMx320VC33 can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. These features result in high performance and ease of use. General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure.

The SM320C3x supports a wide variety of system applications from host processor to dedicated coprocessor. High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SM320VC33	CFP (164)	12.00 mm × 12.00 mm
SMJ320VC33	CFP (164)	29.09 mm × 29.09 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

1 **Features** ... 1
2 **Description** ... 1
3 **Revision History** ... 2
4 **Description (continued)** ... 3
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 7
- 6.1 Absolute Maximum Ratings ... 7
- 6.2 Recommended Operating Conditions ... 7
- 6.3 Electrical Characteristics ... 8
- 6.4 Phase-Locked Loop Characteristics Using EXTCLK or On-Chip Crystal Oscillator Timing Requirements ... 9
- 6.5 Circuit Parameters for On-Chip Crystal Oscillator Timing Requirements ... 9
- 6.6 Timing Requirements for EXTCLK, All Modes ... 10
- 6.7 Timing Requirements for Memory Read/Write for STRB ... 10
- 6.8 Timing Requirements for XF0 and XF1 when Executing LDFI or LDII ... 10
- 6.9 Timing Requirements for XF0 and XF1 when Executing SIGI ... 11
- 6.10 Timing Requirements for Changing XFx from Output to Input Mode ... 11
- 6.11 Timing Requirements for RESET ... 11
- 6.12 Timing Requirements for INT3 to INT0 Response ... 11
- 6.13 Timing Requirements for Serial Port ... 12
- 6.14 Timing Requirements for HOLD/HOLDA ... 13
- 6.15 Timing Requirements for Peripheral Pin General-Purpose I/O ... 13
- 6.16 Timing Requirements for Timer Pin ... 13
- 6.17 Timing Requirements for IEEE-1149.1 Test Access Port ... 13
- 6.18 Switching Characteristics for EXTCLK, All Modes ... 14
- 6.19 Switching Characteristics for Memory Read/Write for STRB ... 14
- 6.20 Switching Characteristics for XF0 and XF1 when Executing LDFI or LDII ... 14
- 6.21 Switching Characteristics for XF0 when Executing STFI or STII ... 14
- 6.22 Switching Characteristics for XF0 and XF1 when Executing SIGI ... 14
- 6.23 Switching Characteristics for Loading when XF is Configured as an Output ... 15
- 6.24 Switching Characteristics for Changing XFx from Output to Input Mode ... 15
- 6.25 Switching Characteristics for Changing XFx from an Input to an Output ... 15
- 6.26 Switching Characteristics for RESET ... 15
- 6.27 Switching Characteristics for IACK ... 15
- 6.28 Switching Characteristics for Serial Port ... 16
- 6.29 Switching Characteristics for HOLD/HOLDA ... 16
- 6.30 Switching Characteristics for Peripheral Pin General-Purpose I/O ... 16
- 6.31 Switching Characteristics for Timer Pin ... 16
- 6.32 Switching Characteristics for SHZ ... 17

7 **Parameter Measurement Information** ... 18
8 **Detailed Description** ... 29
- 8.1 Functional Block Diagram ... 29
- 8.2 Feature Description ... 30
- 8.3 Register Maps ... 41

9 **Power Supply Recommendations** ... 44
- 9.1 Power Sequencing Considerations ... 44

10 **Device and Documentation Support** ... 45
- 10.1 Third-Party Products Disclaimer ... 45
- 10.2 Device Support ... 45
- 10.3 Related Links ... 47
- 10.4 Community Resources ... 47
- 10.5 Trademarks ... 48
- 10.6 Electrostatic Discharge Caution ... 48
- 10.7 Glossary ... 48

11 **Mechanical, Packaging, and Orderable Information** ... 48

3 Revision History

Changes from Revision E (October 2002) to Revision F — **Page**

- Added to *Features* list and updated *Description* ... 1
- Added *Feature Description* section, *Power Supply Recommendations* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 30
- Corrected figure reference in *PLL Isolation* ... 32
- Added more detail to *Clock and PLL Considerations on Initialization* ... 33
- Updated note in *Interrupt-Acknowledge Timing* ... 39

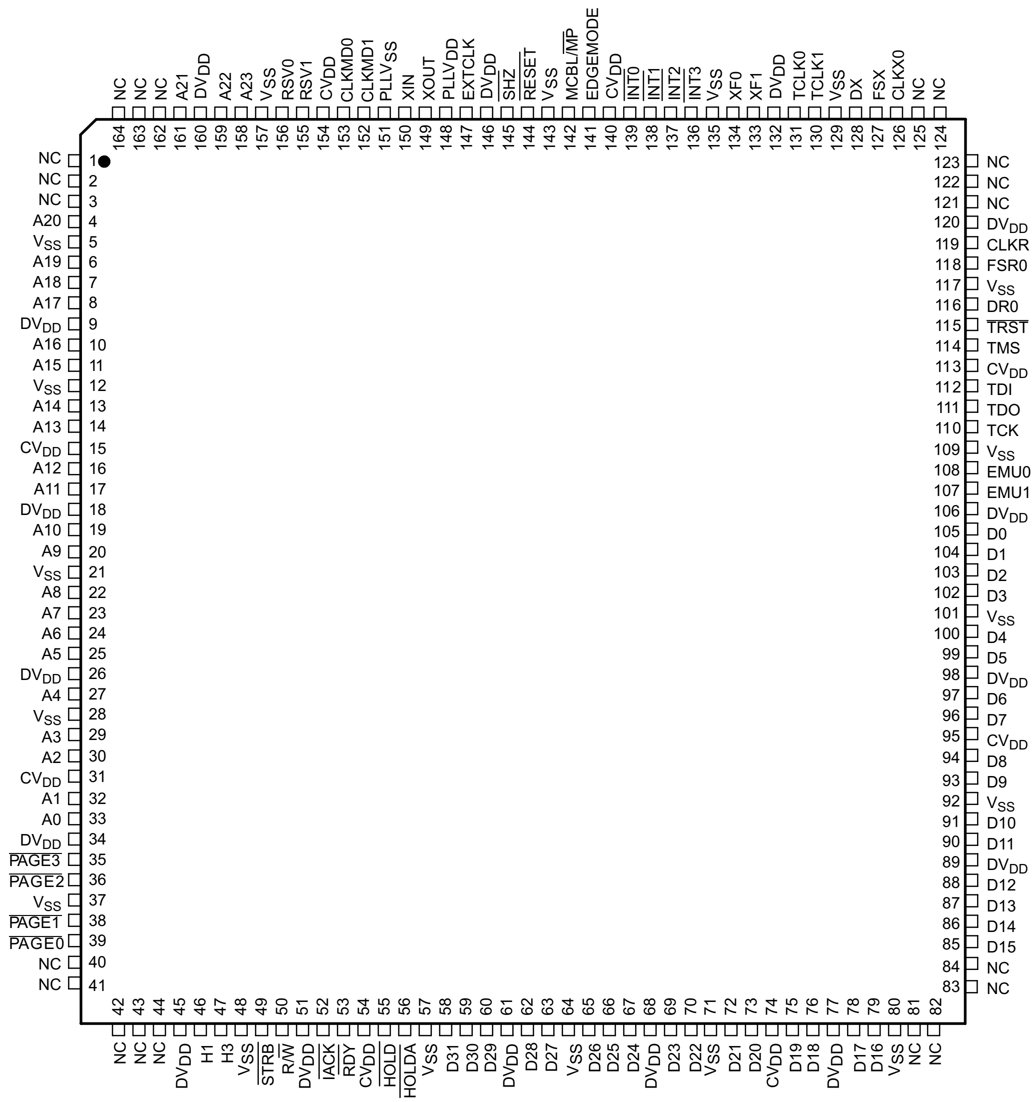
4 Description (continued)

The SM/SMJ320VC33 is a superset of the TMS320C31. Designers now have an additional 1Mb of on-chip SRAM, a maximum throughput of 150 MFLOPS, and several I/O enhancements that allow easy upgrades to current systems or creation of new baselines. This data sheet provides information required to fully use the new features of the SM/SMJ320VC33 device. For general TMS320C3x architecture and programming information, see the *TMS320C3x User's Guide* (SPRU031).

The SMx320VC33 device is packaged in 164-pin low-profile quad flatpacks (HFG suffix) and in 144-ball fine pitch ball grid arrays (GNL and GNM suffix).

5 Pin Configuration and Functions

HFG Package
164-Pin CFP
Top View



NC – No internal connection

NOTE: DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. VSS is the ground for both the I/O pins and the core CPU.

$PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

GNM Pin Assignments(1)

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
A0	J2	D0	G12	DV_{DD}	M1	$R/\overline{W}$	L4
A1	K2	D1	G10		N1	$\overline{RDY}$	M5
A2	K1	D2	F13		N4	$\overline{RESET}$	B7
A3	J4	D3	G11		N7	RSV0	B4
A4	H4	D4	H10		M8	RSV1	D5
A5	H3	D5	H13		N12	$\overline{SHZ}$	D7
A6	H1	D6	H12		L13	$\overline{STRB}$	M4
A7	G4	D7	J10		H11	TCK	F10
A8	G1	D8	J11		F11	TCLK0	C10
A9	G2	D9	J12		B12	TCLK1	A11
A10	F3	D10	K13		A10	TDI	E11
A11	F4	D11	K12		A6	TDO	D13
A12	F2	D12	K10		A1	TMS	E10
A13	E1	D13	M13	DX0	A12	$\overline{TRST}$	C13
A14	E2	D14	L11	EDGEMODE	A7	V_{SS}	B1
A15	E4	D15	L12	EMU0	F12		D1
A16	C1	D16	M12	EMU1	E12		G3
A17	C2	D17	L10	EXTCLK	C6		J1
A18	D3	D18	K9	FSR0	C12		L2
A19	C3	D19	N11	FSX	D10		M3
A20	B2	D20	M11	H1	L3		M6
A21	D4	D21	M10	H3	N2		L7
A22	A2	D22	K8	$\overline{HOLD}$	N5		N10
A23	B3	D23	N9	$\overline{HOLDA}$	K5		N13
CLKMD0	C5	D24	M9	$\overline{IACK}$	K4		K11
CLKMD1	B5	D25	L8	$\overline{INT0}$	C8		G13
CLKR0	B13	D26	N8	$\overline{INT1}$	B9		E13
CLKX0	B11	D27	M7	$\overline{INT2}$	D8		A13
CV_{DD}	E3	D28	K7	$\overline{INT3}$	A9		C11
	J3	D29	L6	$MCBL/\overline{MP}$	B8		C9
	L5	D30	N6	$\overline{PAGE0}$	M2		C7
	L9	D31	K6	$\overline{PAGE1}$	N3		C4
	J13	DR0	D11	$\overline{PAGE2}$	L1	XF0	B10
	D12	DV_{DD}	D2	$\overline{PAGE3}$	K3	XF1	D9
	A8		F1	$PLLV_{DD}$ (2)	A5	XIN	B6
	A3		H2	$PLLV_{SS}$ (2)	A4	XOUT	D6

(1) DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.
(2) $PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

Pin Functions

PIN NAME	PIN QTY	TYPE(1)	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE(2)
PRIMARY-BUS INTERFACE				
D31- D0	32	I/O/Z	32-bit data port	S H R
			Data port bus keepers. (See Figure 30)	S
A23- A0	24	O/Z	24-bit address port	S H R
R/W	1	O/Z	Read/write. R/W is high when a read is performed and low when a write is performed over the parallel interface.	S H R
STRB	1	O/Z	Strobe. For all external-accesses	S H
PAGE0 to PAGE3	1	O/Z	Page strobes. Four decoded page strobes for external access	S H R
RDY	1	I	Ready. RDY indicates that the external device is prepared for a transaction completion.	
HOLD	1	I	Hold. When HOLD is a logic low, any ongoing transaction is completed. A23 to A0, D31 to D0, STRB, and R/W are placed in the high-impedance state and all transactions over the primary-bus interface are held until HOLD becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.	
HOLDA	1	O/Z	Hold acknowledge. HOLDA is generated in response to a logic-low on HOLD. HOLDA indicates that A23 to A0, D31 to D0, STRB, and R/W are in the high-impedance state and that all transactions over the bus are held. HOLDA is high in response to a logic-high of HOLD or the NOHOLD bit of the primary-bus-control register is set.	S
CONTROL SIGNALS				
RESET	1	I	Reset. When RESET is a logic low, the device is in the reset condition. When RESET becomes a logic high, execution begins from the location specified by the reset vector.	
EDGEMODE	1	I	Edge mode. Enables interrupt edge mode detection.	
INT3 to INT0	4	I	External interrupts	
IACK	1	O/Z	Internal acknowledge. IACK is generated by the IACK instruction. IACK can be used to indicate when a section of code is being executed.	S
MCBL/MP	1	I	Microcomputer bootloader/microprocessor mode-select	
SHZ	1	I	Shutdown high impedance. When active, SHZ places all pins in the high-impedance state. SHZ can be used for board-level testing or to ensure that no dual-drive conditions occur. **CAUTION**: A low on SHZ corrupts the device memory and register contents. Reset the device with SHZ high to restore it to a known operating condition.	
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S R
SERIAL PORT 0 SIGNALS				
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S R
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S R
DR0	1	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S R
DX0	1	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S R
TIMER SIGNALS				
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S R

(1) I = input, O = output, Z = high-impedance state
(2) S = SHZ active, H = HOLD active, R = RESET active

Pin Functions (continued)

PIN NAME	PIN QTY	TYPE[1]	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE[2]	
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
SUPPLY AND OSCILLATOR SIGNALS					
H1	1	O/Z	External H1 clock	S	
H3	1	O/Z	External H3 clock	S	
CV_{DD}	8	I	+VDD. Dedicated 1.8-V power supply for the core CPU. All must be connected to a common supply plane.[3]		
DV_{DD}	16	I	+VDD. Dedicated 3.3-V power supply for the I/O pins. All must be connected to a common supply plane.[3]		
V_{SS}	18	I	Ground. All grounds must be connected to a common ground plane.		
$PLLV_{DD}$	1	I	Internally isolated PLL supply. Connect to CVDD (1.8 V)		
$PLLV_{SS}$	1	I	Internally isolated PLL ground. Connect to V_{SS}		
EXTCLK	1	I	External clock. Logic level compatible clock input. If the XIN/XOUT oscillator is used, tie this pin to ground.		
XOUT	1	O	Clock out. Output from the internal-crystal oscillator. If a crystal is not used, leave XOUT unconnected.		
XIN	1	I	Clock in. Internal-oscillator input from a crystal. If EXTCLK is used, tie this pin to ground.		
CLKMD0, CLKMD1	2	I	Clock mode select pins		
RSV0 to RSV1	2	I	Reserved. Use individual pullups to DV_{DD}.		
JTAG EMULATION					
EMU1 to EMU0	2	I/O	Emulation pins 0 and 1, use individual pullups to DV_{DD}		
TDI	1	I	Test data input		
TDO	1	O	Test data output		
TCK	1	I	Test clock		
TMS	1	I	Test mode select		
$\overline{TRST}$	1	I	Test reset		

(3) Recommended decoupling. Four 0.1 μF for CV_{DD} and eight 0.1 μF for DV_{DD}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
CV_{DD}	Supply voltage [2]	–0.3	2.4	V
DV_{DD}		–0.3	4	
V_I	Input voltage [3]	–1	4.6	
V_O	Output voltage	–0.3	4.6	
	Continuous power dissipation (worst case) [4]		500	mW
T_C	Operating case temperature	–55	125	°C
T_{stg}	Storage temperature	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.
(3) Absolute dc input level should not exceed the DV_{DD} or V_{SS} supply rails by more than 0.3 V. An instantaneous low current pulse of <2 ns, <10 mA, and <1 V amplitude is permissible.
(4) Actual operating power is much lower. This value was obtained under specially produced worst-case test conditions for the SMx320VC33, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external data and address buses at the maximum possible rate with a capacitive load of 30 pF. See normal (I_{CC}) current specification in *Electrical Characteristics* and also read *TMS320C3x General-Purpose Applications* (SPRU194).

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) [1][2][3]

		MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage for the core CPU [4]	1.71	1.8	1.89	V
DV_{DD}	Supply voltage for the I/O pins [5]	3.14	3.3	3.46	V
V_{SS}	Supply ground		0		V
V_{IH}	High-level input voltage	0.7 x DV_{DD}		DV_{DD} + 0.3 [6]	V
V_{IL}	Low-level input voltage	–0.3 [6]		0.3 x DV_{DD}	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current			4	mA
C_L	Capacitive load per output pin			30	pF
T_C	Operating case temperature	–55		125	°C

(1) All voltage values are with respect to V_{SS}.
(2) All inputs and I/O pins are configured as inputs.
(3) All input and I/O pins use a Schmidt hysteresis inputs except $\overline{SHZ}$ and D0 to D31. Hysteresis is approximately 10% of DV_{DD} and is centered at 0.5 × DV_{DD}.
(4) CV_{DD} should not exceed DV_{DD} by more than 0.7 V. (Use a Schottky clamp diode between these supplies.)
(5) DV_{DD} should not exceed CV_{DD} by more than 2.5 V.
(6) Absolute dc input level should not exceed the DV_{DD} or V_{SS} supply rails by more than 0.3 V. An instantaneous low current pulse of <2 ns, <10 mA, and <1 V amplitude is permissible.

6.3 Electrical Characteristics

over recommended ranges of supply voltage (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS[2]	MIN	TYP[3]	MAX	UNIT
V_{OH}	High-level output voltage	DV_{DD} = MIN, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	DV_{DD} = MIN, I_{OL} = MAX			0.4	V
I_Z	High-impedance current	T_C = 25°C, DV_{DD} = MAX	–5		5	µA
I_I	Input current	T_C = 25°C, V_I = V_{SS} to DV_{DD}	–5		5	µA
I_{IPU}	Input current (with internal pullup)	Inputs with internal pullups[4]	–600		10	µA
I_{IPD}	Input current (with internal pulldown)	Inputs with internal pulldowns[4]	600		10	µA
I_{BKU}	Input current (with bus keeper) pullup[5]	Bus keeper opposes until conditions match	–600		10	µA
I_{BKD}	Input current (with bus keeper) pulldown[5]	T_C = 25°C, f_x = 75 MHz	600		10	µA
I_{DDD}	Supply current, pins[6][7]	DV_{DD} = MAX		25	260	mA
I_{DDC}	Supply current, core CPU[6][7]	T_C = 25°C, f_x = 75 MHz, CV_{DD} = MAX		60	215	mA
I_{DD}	IDLE2, Supply current I_{DDD} plus I_{DDC}	PLL enabled, oscillator enabled		2		mA
		PLL disabled, oscillator enabled		500		µA
		PLL disabled, oscillator disabled, FCLK = 0		50		µA
C_i	Input capacitance	All inputs except XIN			10[8]	pF
		XIN			10[8]	pF
C_o	Output capacitance				10[8]	pF

(1) All voltage values are with respect to V_{SS}.
(2) For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in *Recommended Operating Conditions*.
(3) For VC33, all typical values are at DV_{DD} = 3.3, CV_{DD} = 1.8 V, T_C (case temperature) = 25°C.
(4) Pins with internal pullup devices: TDI, TCK, and TMS. Pin with internal pulldown device: $\overline{TRST}$.
(5) Pins D0 to D31 include internal bus keepers that maintain valid logic levels when the bus is not driven (see Figure 30).
(6) Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible. See *TMS320C3x General-Purpose Applications* (SPRU194).
(7) f_x is the PLL output clock frequency.
(8) Not production tested

6.4 Phase-Locked Loop Characteristics Using EXTCLK or On-Chip Crystal Oscillator Timing Requirements

see [1][2]

		MIN	MAX	UNIT
F_{pllin}	Frequency range, PLL input	5[3]	15[3]	MHz
F_{pllout}	Frequency range, PLL output	25[3]	75[3]	MHz
I_{pll}	PLL current, CVDD supply		2[3]	mA
P_{pll}	PLL power, CVDD supply		5[3]	mW
PLL_{dc}	PLL output duty cycle at H1	45%[3]	55%[3]	
PLLJ	PLL output jitter, F_{pllout} = 25 MHz		400[3]	ps
PLL_{LOCK}	PLL lock time in input cycles		1000	cycles

(1) Duty cycle is defined as 100 × t_1 / (t_1 + t_2)%
(2) To ensure clean internal clock references, the minimal low and high pulse durations must be maintained. At high frequencies, this may require a fast rise and fall time as well as a tightly controlled duty cycle. At lower frequencies, these requirements are less restrictive when in x1 and x0.5 modes. The PLL, however, must have an input duty cycle of between 40% and 60% for proper operation.
(3) Not production tested

6.5 Circuit Parameters for On-Chip Crystal Oscillator Timing Requirements

see Figure 2[1]

		MIN	TYP	MAX	UNIT
V_O	Oscillator internal supply voltage		CV_{DD}		V
F_O	Fundamental mode frequency range	1[2]		20[2]	MHz
V_{bias}	DC bias point (input threshold)	40[2]	50	60[2]	%VO
R_{fbk}	Feedback resistance	100[2]	300	500[2]	kΩ
R_{out}	Small signal ac output impedance	250[2]	500	1000[2]	Ω
V_{xoutac}	The ac output voltage with test crystal[3]		85		%VO
V_{xinac}	The ac input voltage with test crystal[3]		85		%VO
V_{xoutl}	$V_{xin} = V_{xinh}$, $I_{xout} = 0$, $F_O = 0$ (logic input)	V_{SS} – 0.1[2]		V_{SS} + 0.3[2]	V
V_{xouth}	$V_{xin} = V_{xinl}$, $I_{xout} = 0$, $F_O = 0$ (logic input)	CV_{DD} – 0.3[2]		CV_{DD} + 0.1[2]	V
V_{inl}	When used for logic level input, oscillator enabled	–0.3[2]		0.2 × V_O[2]	V
V_{inh}	When used for logic level input, oscillator enabled	0.8 × V_O[2]		DV_{DD} + 0.3[2]	V
V_{xinh}	When used for logic level input, oscillator disabled	0.7 × DV_{DD}		DV_{DD} + 0.3	V
C_{xout}	XOUT internal load capacitance	2[2]	3	5[2]	pF
C_{xin}	XIN internal load capacitance	2[2]	3	5[2]	pF
$t_{d(XIN-H1)}$	Delay time, XIN to H1 x1 and x0.5 modes	2	5.5	8	ns
I_{inl}	Input current, feedback enabled, $V_{il} = 0$			50[2]	μA
I_{inh}	Input current, feedback enabled, $V_{il} = V_{ih}$			–50[2]	μA

(1) This circuit is intended for series resonant fundamental mode operation.
(2) Not production tested
(3) Signal amplitude is dependent on the crystal and load used.

6.6 Timing Requirements for EXTCLK, All Modes

see Figure 3 and Figure 4

			MIN	MAX	UNIT
$t_{r(EXTCLK)}$	Rise time, EXTCLK	F = F_{max}, x0.5 and x1 modes	1 (1)		ns
		F < F_{max}	4 (1)		
$t_{f(EXTCLK)}$	Fall time, EXTCLK	F = F_{max}, x0.5 and x1 modes	1 (1)		ns
		F < F_{max}	4 (1)		
$t_{w(EXTCLKL)}$	Pulse duration, EXTCLK low	x5 mode	21 (1)		ns
		x1 mode	6 (1)		
		x0.5 mode	4 (1)		
$t_{w(EXTCLKH)}$	Pulse duration, EXTCLK high	x5 mode	21 (1)		ns
		x1 mode	5 (1)		
		x0.5 mode	4 (1)		
$t_{dc(EXTCLK)}$	Duty cycle, EXTCLK [$t_{w(EXTCLKH)}$ / $t_{c(H)}$]	x5 PLL mode	40% (1)	60% (1)	
		x1 and x0.5 modes, F = max	45%	55%	
		x1 and x0.5 modes, F = 0 Hz	0% (1)	100% (1)	
$t_{c(EXTCLK)}$	Cycle time, EXTCLK	x5 mode	66.7 (1)	200 (1)	ns
		x1 mode	13.3		
		x0.5 mode	10 (1)		
F_{ext}	Frequency range, 1 / $t_{c(EXTCLK)}$	x5 mode	5 (1)	15 (1)	MHz
		x1 mode	0	75	
		x0.5 mode	0 (1)	100 (1)	

(1) Not production tested

6.7 Timing Requirements for Memory Read/Write for $\overline{STRB}$

see Figure 5 through Figure 7 (1)

			MIN	MAX	UNIT
$t_{su(D-H1L)R}$	Setup time, data before H1 low (read)		5 (2)		ns
$t_{h(H1L-D)R}$	Hold time, data after H1 low (read)		–1 (2)		
$t_{su(RDY-H1H)}$	Setup time, $\overline{RDY}$ before H1 high		5		
$t_{h(H1H-RDY)}$	Hold time, $\overline{RDY}$ after H1 high		–1 (2)		
$t_{d(A-RDY)}$	Delay time, address valid to $\overline{RDY}$			P – 6 (2)(3)	
$t_{v(A-D)}$	Valid time, data valid after address PAGEx, or STRB valid	0 wait state, CL = 30 pF		6 (2)	
		1 wait state		tc(H) + 6 (2)	

(1) These timings assume a similar loading of 30 pF on all pins.
(2) Not production tested
(3) P = $t_{c(H)}$ / 2 (when duty cycle equals 50%).

6.8 Timing Requirements for XF0 and XF1 when Executing LDFI or LDII

see Figure 8

		MIN	MAX	UNIT
$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	4 (1)		ns
$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0 (1)		

(1) Not production tested

6.9 Timing Requirements for XF0 and XF1 when Executing SIGI

see Figure 10

		MIN	MAX	UNIT
$t_{su(XF1\text{-}H1L)}$	Setup time, XF1 before H1 low	4 (1)		ns
$t_{h(H1L\text{-}XF1)}$	Hold time, XF1 after H1 low	0 (1)		

(1) Not production tested

6.10 Timing Requirements for Changing XFx from Output to Input Mode

see Figure 12

		MIN	MAX	UNIT
$t_{su(XF\text{-}H1L)}$	Setup time, XFx before H1 low	4		ns
$t_{h(H1L\text{-}XF)}$	Hold time, XFx after H1 low	0		

6.11 Timing Requirements for $\overline{\text{RESET}}$

		MIN	MAX	UNIT
$t_{su(RESET\text{-}EXTCLKL)}$	Setup time, $\overline{\text{RESET}}$ before EXTCLK low	5 (1)	P – 7 (1)(2)	ns
$t_{su(RESETH\text{-}H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	5		

(1) Not production tested
(2) $P = t_{c(EXTCLK)}$

6.12 Timing Requirements for $\overline{\text{INT3}}$ to $\overline{\text{INT0}}$ Response

see Figure 15

		MIN	NOM	MAX	UNIT
$t_{su(INT\text{-}H1L)}$	Setup time, $\overline{\text{INT3}}$ to $\overline{\text{INT0}}$ before H1 low	4 (1)			ns
$t_{h(H1L\text{-}INT)}$	Hold time, $\overline{\text{INT3}}$ to $\overline{\text{INT0}}$ after H1 low			0	
$t_{w(INT)}$	Pulse duration, interrupt to ensure only one interrupt	P + 5 (1)(2)	1.5P	2P - 5 (1)(2)	

(1) Not production tested
(2) $P = t_{c(H)}$

6.13 Timing Requirements for Serial Port

see Figure 34 and Figure 35

			MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$ x 2.6 (1)		ns
		CLKX/R int	$t_{c(H)}$ x 4 (1)(2)	$t_{c(H)}$ × 216 (1)	
$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$ + 5		
		CLKX/R int	[$t_{c(SCK)}$ / 2] - 4 (1)	[$t_{c(SCK)}$ / 2] + 4 (1)	
$t_{r(SCK)}$	Rise time, CLKX/R			3 (1)	
$t_{f(SCK)}$	Fall time, CLKX/R			3 (1)	
$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	4 (1)		
		CLKR int	5 (1)		
$t_{h(CLKRL-DR)}$	Hold time, DR after CLKR low	CLKR ext	3 (1)		
		CLKR int	0 (1)		
$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	4 (1)		
		CLKR int	5 (1)		
$t_{h(SCKL-FS)}$	Hold time, FSX/R input after CLKX/R low	CLKX/R ext	3 (1)		
		CLKX/R int	0 (1)		
$t_{su(FSX-CLKX)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$ – 6] (1)	[$t_{c(SCK)}$ / 2] - 6	
		CLKX int	–[$t_{c(H)}$ - 10] (1)	$t_{c(SCK)}$ / 2 (1)	

(1) Not production tested
(2) A cycle time of $t_{c(H)}$ × 2 is possible when the device is operated at lower CPU frequencies. See the *TMS320VC33 Silicon Update* (SPRZ176) for further details.

6.14 Timing Requirements for $\overline{HOLD}$/$\overline{HOLDA}$

see Figure 17 and Figure 18

		MIN	MAX	UNIT
$t_{su(HOLD-H1L)}$	Setup time, $\overline{HOLD}$ before H1 low	3		ns
$t_{w(HOLD)}$	Pulse duration, $\overline{HOLD}$ low	$3t_{c(H)}$ (1)		

(1) Not production tested.

6.15 Timing Requirements for Peripheral Pin General-Purpose I/O

see Figure 19 and Figure 20 (1)

		MIN	MAX	UNIT
$t_{su(GPIO-H1L)}$	Setup time, general-purpose input before H1 low	3 (2)		ns
$t_{h(H1L-GPIO)}$	Hold time, general-purpose input after H1 low	0 (2)		

(1) Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.
(2) Not production tested

6.16 Timing Requirements for Timer Pin

see Figure 21 and Figure 22 (1)

		MIN	MAX	UNIT
$t_{su(TCLK-H1L)}$ (2)	Setup time, TCLK external before H1 low	3 (3)		ns
$t_{h(H1L-TCLK)}$ (2)	Hold time, TCLK external after H1 low	0		

(1) Valid logic-level periods and polarity are specified by the contents of the internal control registers.
(2) These requirements are applicable for a synchronous input clock.
(3) Not production tested

6.17 Timing Requirements for IEEE-1149.1 Test Access Port

see Figure 24

		MIN	MAX	UNIT
$t_{su(TMS-TCKH)}$	Setup time, TMS/TDI to TCK high	5 (1)		ns
$t_{h(TCKH-TMS)}$	Hold time, TMS/TDI from TCK high	5 (1)		ns
$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0 (1)	10 (1)	ns
$t_{r\ (TCK)}$	Rise time, TCK		3 (1)	ns
$t_{f\ (TCK)}$	Fall time, TCK		3 (1)	ns

(1) Not production tested

6.18 Switching Characteristics for EXTCLK, All Modes

over recommended operating conditions, all modes (see Figure 3 and Figure 4)

PARAMETER			MIN	TYP	MAX	UNIT
V_{mid}	Midlevel, used to measure duty cycle			0.5 × DV_{DD}		V
$t_{d(EXTCLK-H)}$	Delay time, EXTCLK to H1 and H3	x1 mode	2[1]	4.5	7[1]	ns
		x0.5 mode	2[1]	4.5	7[1]	
$t_{r(H)}$	Rise time, H1 and H3				3[1]	ns
$t_{f(H)}$	Fall time, H1 and H3				3[1]	ns
$t_{d(HL-HH)}$	Delay time, from H1 low to H3 high or from H3 low to H1 high		–1.5[1]		2[1]	ns
$t_{c(H)}$	Cycle time, H1 and H3	x5 PLL mode		$1 / (5 \times f_{ext})$		ns
		x1 mode		$1 / f_{ext}$		
		x0.5 mode		$2 / f_{ext}$		

(1) Not production tested

6.19 Switching Characteristics for Memory Read/Write for $\overline{\text{STRB}}$

over recommended operating conditions for memory read/write[1] (see Figure 5 through Figure 7)

PARAMETER		MIN	MAX	UNIT
$t_{d(H1L-SL)}$	Delay time, H1 low to $\overline{\text{STRB}}$ low	–1[2]	3	ns
$t_{d(H1L-SH)}$	Delay time, H1 low to $\overline{\text{STRB}}$ high	–1[2]	3	
$t_{d(H1H-RWL)W}$	Delay time, H1 high to R/$\overline{\text{W}}$ low (write)	–1[2]	3	
$t_{d(H1L-A)}$	Delay time, H1 low to address valid	–1[2]	3	
$t_{d(H1H-RWH)W}$	Delay time, H1 high to R/W high (write)	–1[2]	3	
$t_{d(H1H-A)W}$	Delay time, H1 high to address valid on back-to-back write cycles (write)	–1[2]	3[2]	
$t_{v(H1L-D)W}$	Valid time, data after H1 low (write)		5	
$t_{h(H1H-D)W}$	Hold time, data after H1 high (write)	0[2]	5	

(1) These timings assume a similar loading of 30 pF on all pins.
(2) Not production tested

6.20 Switching Characteristics for XF0 and XF1 when Executing LDFI or LDII

over recommended operating conditions for XF0 and XF1 when executing LDFI or LDII (see Figure 8)

PARAMETER		MIN	MAX	UNIT
$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		3	ns

6.21 Switching Characteristics for XF0 when Executing STFI or STII

over recommended operating conditions for XF0 when executing STFI or STII (see Figure 9)

PARAMETER		MIN	MAX	UNIT
$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high[1]		3	ns

(1) XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

6.22 Switching Characteristics for XF0 and XF1 when Executing SIGI

over recommended operating conditions for XF0 and XF1 when executing SIGI (see Figure 10)

PARAMETER		MIN	MAX	UNIT
$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		3	ns
$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		3	

6.23 Switching Characteristics for Loading when XF is Configured as an Output

over recommended operating conditions for loading the XF register when configured as an output pin (see Figure 11)

		MIN	MAX	UNIT
$t_{v(H3H\text{-}XF)}$	Valid time, XFx after H3 high		3	ns

6.24 Switching Characteristics for Changing XFx from Output to Input Mode

over recommended operating conditions for changing XFx from output to input mode (see Figure 12)

PARAMETER		MIN	MAX	UNIT
$t_{dis(H3H\text{-}XF)}$	Disable time, XFx after H3 high		5 (1)	ns

(1) Not production tested

6.25 Switching Characteristics for Changing XFx from an Input to an Output

over recommended operating conditions for changing XFx from input to output mode (see Figure 13)

PARAMETER		MIN	MAX	UNIT
$t_{d(H3H\text{-}XF)}$	Delay time, H3 high to XFx switching from input to output		3	ns

6.26 Switching Characteristics for $\overline{\text{RESET}}$

over recommended operating conditions for $\overline{\text{RESET}}$ (see Figure 14)

PARAMETER		MIN (1)	MAX (1)	UNIT
$t_{d(EXTCLKH\text{-}H1H)}$	Delay time, EXTCLK high to H1 high	2	7	ns
$t_{d(EXTCLKH\text{-}H1L)}$	Delay time, EXTCLK high to H1 low	2	7	
$t_{d(EXTCLKH\text{-}H3L)}$	Delay time, EXTCLK high to H3 low	2	7	
$t_{d(EXTCLKH\text{-}H3H)}$	Delay time, EXTCLK high to H3 high	2	7	
$t_{dis(H1H\text{-}DZ)}$	Disable time, data (high impedance) from H1 high (2)		6	
$t_{dis(H3H\text{-}AZ)}$	Disable time, address (high impedance) from H3 high		6	
$t_{d(H3H\text{-}CONTROLH)}$	Delay time, H3 high to control signals high		3	
$t_{d(H1H\text{-}RWH)}$	Delay time, H1 high to R/$\overline{\text{W}}$ high		3	
$t_{d(H1H\text{-}IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		3	
$t_{dis(RESETL\text{-}ASYNCH)}$	Disable time, asynchronous reset signals disabled (high impedance) from $\overline{\text{RESET}}$ low (3)		6	

(1) Not production tested
(2) High impedance for Dbus is limited to nominal bus keeper Z_{OUT} = 15 kΩ.
(3) Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

6.27 Switching Characteristics for $\overline{\text{IACK}}$

over recommended operating conditions for $\overline{\text{IACK}}$ (see Figure 16)

PARAMETER		MIN	MAX	UNIT
$t_{d(H1H\text{-}IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low	–1 (1)	3	ns
$t_{d(H1H\text{-}IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high	–1 (1)	3	

(1) Not production tested

6.28 Switching Characteristics for Serial Port

over recommended operating conditions (see Figure 34 and Figure 35)

PARAMETER			MIN	MAX	UNIT
$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			4 (1)	ns
$t_{d(CLKX-DX)}$	Delay time, CLKX to DX valid	CLKX ext		6	
		CLKX int		5 (1)	
$t_{d(CLKX-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		5	
		CLKX int		4 (1)	
$t_{d(CLKX-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		4	
		CLKX int		5 (1)	
$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			6	
$t_{dis(CLKX-DXZ)}$	Disable time, DX high impedance following last data bit from CLKX high			6	

(1) Not production tested

6.29 Switching Characteristics for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$

over recommended operating conditions for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ (see Figure 17 and Figure 18)

PARAMETER		MIN	MAX	UNIT
$t_{v(H1L-HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ after H1 low	–1 (1)	3 (1)	ns
$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low	$2t_{c(H)} - 4$ (1)		
$t_{d(H1L-SH)H}$	Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	–1	3	
$t_{dis(H1L-S)}$	Disable time, $\overline{\text{STRB}}$ to the high-impedance state from H1 low		4	
$t_{en(H1L-S)}$	Enable time, $\overline{\text{STRB}}$ enabled (active) from H1 low		4	
$t_{dis(H1L-RW)}$	Disable time, R/$\overline{\text{W}}$ to the high-impedance state from H1 low		5 (1)	
$t_{en(H1L-RW)}$	Enable time, R/$\overline{\text{W}}$ enabled (active) from H1 low		4	
$t_{dis(H1L-A)}$	Disable time, address to the high-impedance state from H1 low		4 (1)	
$t_{en(H1L-A)}$	Enable time, address enabled (valid) from H1 low		5	
$t_{dis(H1H-D)}$	Disable time, data to the high-impedance state from H1 high		4 (1)	

(1) Not production tested.

6.30 Switching Characteristics for Peripheral Pin General-Purpose I/O

over recommended operating conditions for peripheral pin general-purpose I/O (see Figure 19 and Figure 20) (1)

PARAMETER		MIN	MAX	UNIT
$t_{d(H1H-GPIO)}$	Delay time, H1 high to general-purpose output		4	ns
$t_{dis(H1H)}$	Disable time, general-purpose output from H1 high		5	

(1) Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.

6.31 Switching Characteristics for Timer Pin

over recommended operating conditions for timer pin (see Figure 21 and Figure 22)

PARAMETER			MIN	MAX	UNIT
$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK internal valid			3	ns
$t_{c(TCLK)}$ (1)	Cycle time, TCLK	TCLK ext		$t_{c(H)} \times 2.6$ (2)	
		TCLK int	$t_{c(H)} \times 2$ (2)	$t_{c(H)} \times 232$ (2)	
$t_{w(TCLK)}$ (1)	Pulse duration, TCLK	TCLK ext		$t_{c(H)} + 5$ (2)	
		TCLK int	$[t_{c(TCLK)} / 2] - 4$ (2)	$[t_{c(TCLK)} / 2] + 4$ (2)	

(1) These parameters are applicable for an asynchronous input clock.
(2) Not production tested

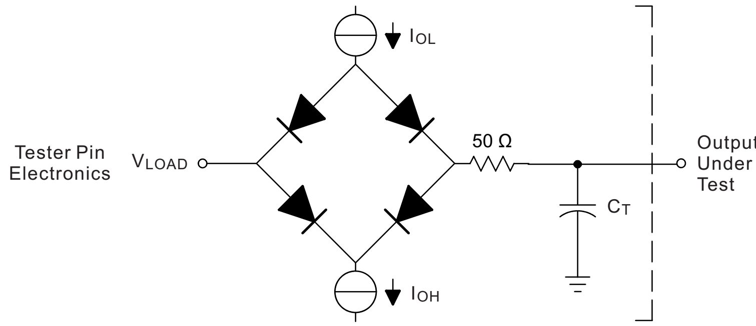
6.32 Switching Characteristics for $\overline{SHZ}$

over recommended operating conditions for $\overline{SHZ}$ (see Figure 23)

PARAMETER		MIN	MAX	UNIT
$t_{dis(SHZ)}$	Disable time, $\overline{SHZ}$ low to all outputs, I/O pins disabled (high impedance)	0[(1)]	8[(1)]	ns

(1) Not production tested

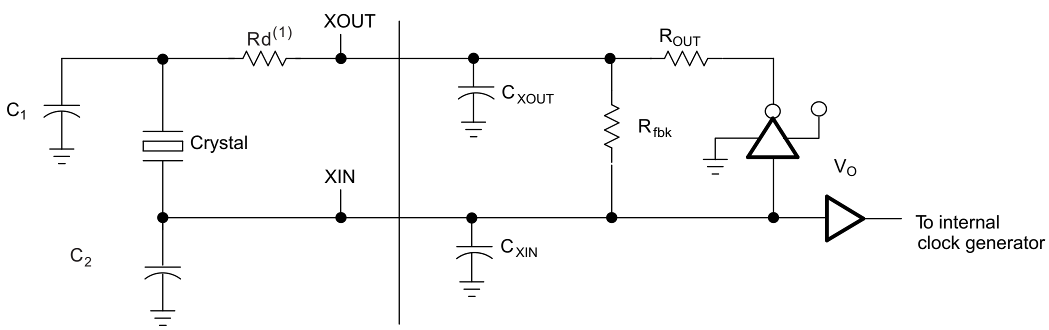
7 Parameter Measurement Information



where:

- I_{OL} = 4 mA (all outputs) for dc levels test.
- I_O and I_{OH} are adjusted during ac timing analysis to achieve an ac termination of 50 Ω
- $V_{LOAD} = DV_{DD} / 2$
- C_T = 40-pF typical load-circuit capacitance

Figure 1. Test Load Circuit



(1) See Table 3 for value of Rd.

Figure 2. On-Chip Oscillator Circuit

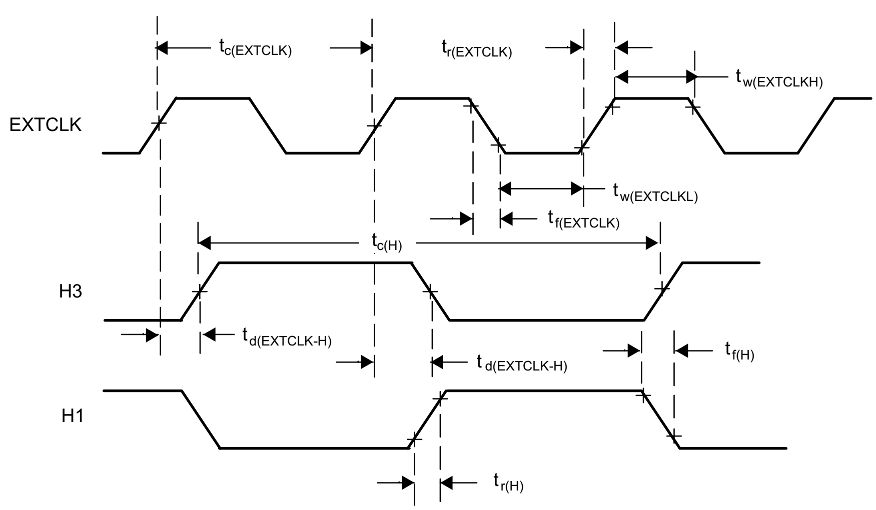
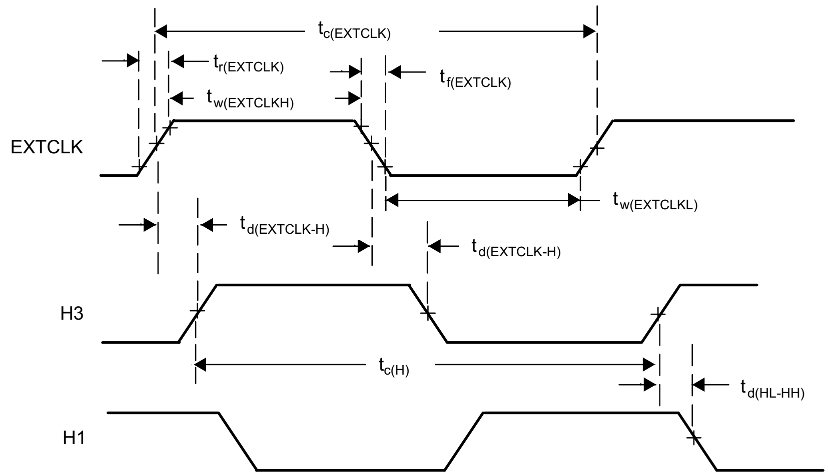


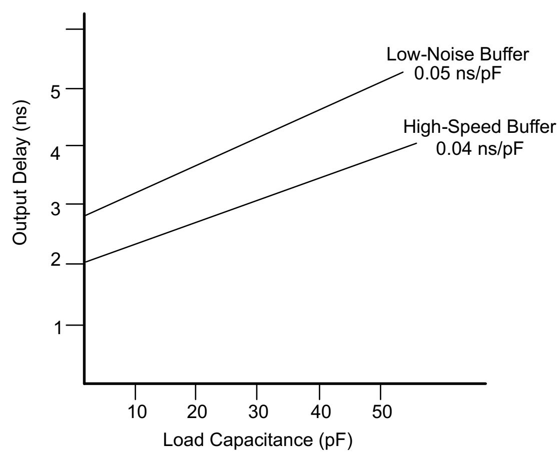
Figure 3. Divide-by-Two Mode

Parameter Measurement Information (continued)



EXTCLK is held low.

Figure 4. Divide-by-One Mode



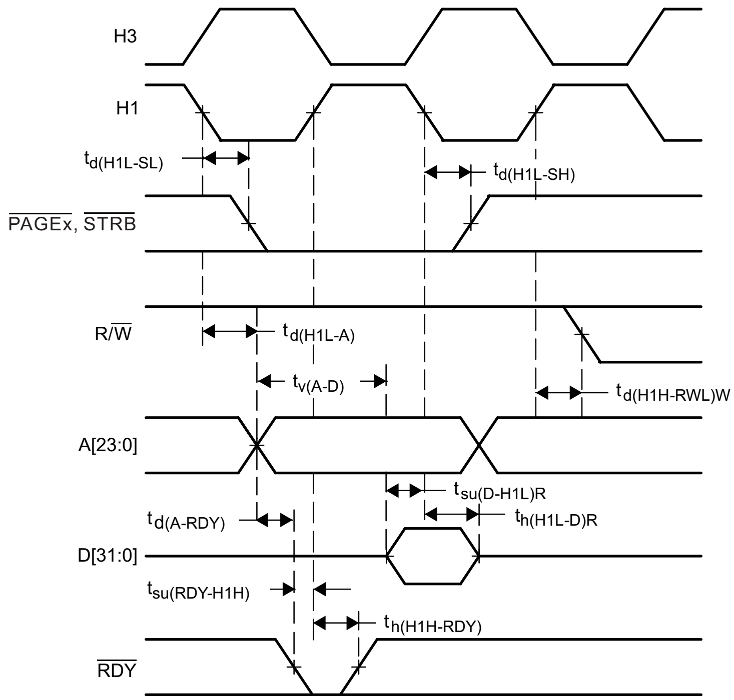
LOAD	HIGH SPEED	LOW NOISE
0 pF	2.0	2.8
15 pF	2.6	3.4
30 pF	3.2	4.4
50 pF	4.0	5.25

This figure shows output load characteristics for high-speed and low-speed (low-noise) output buffers. High-speed buffers are used on A0 to A23, $\overline{\text{PAGE0}}$ to $\overline{\text{PAGE3}}$, H1, H3, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$. All other outputs use the low-speed, (low-noise) output buffer.

C_{Lmax} = 30 pF

Figure 5. Output Load Characteristics, Buffer Only

Parameter Measurement Information (continued)



$\overline{STRB}$ remains low during back-to-back read operations.

Figure 6. Timing for Memory ($\overline{STRB}$ = 0 and $\overline{PAGEx}$ = 0) Read

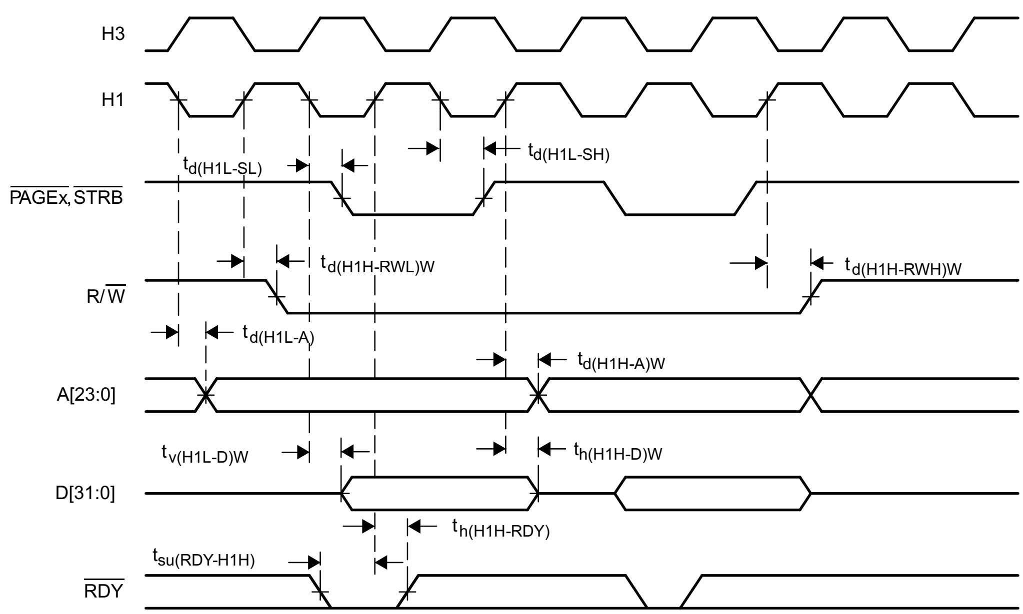


Figure 7. Timing for Memory ($\overline{STRB}$ = 0 and $\overline{PAGEx}$ = 0) Write

Parameter Measurement Information (continued)

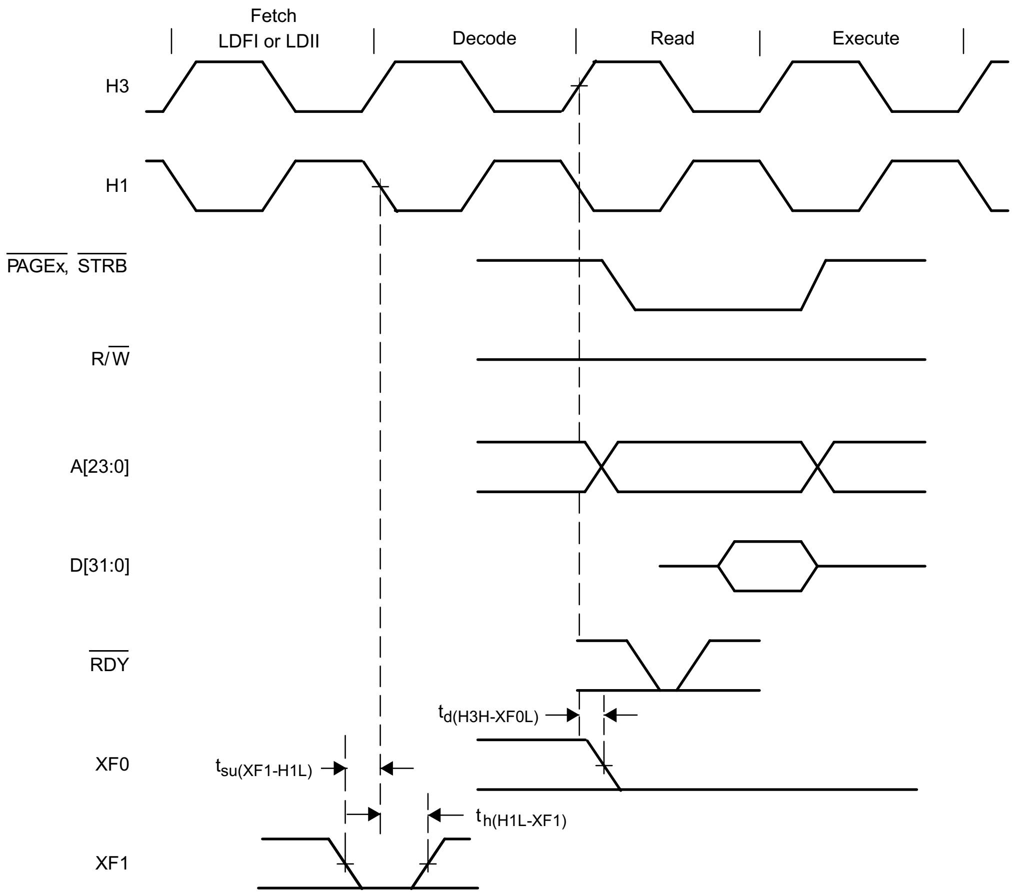


Figure 8. Timing for XF0 and XF1 When Executing LDFI or LDII

Parameter Measurement Information (continued)

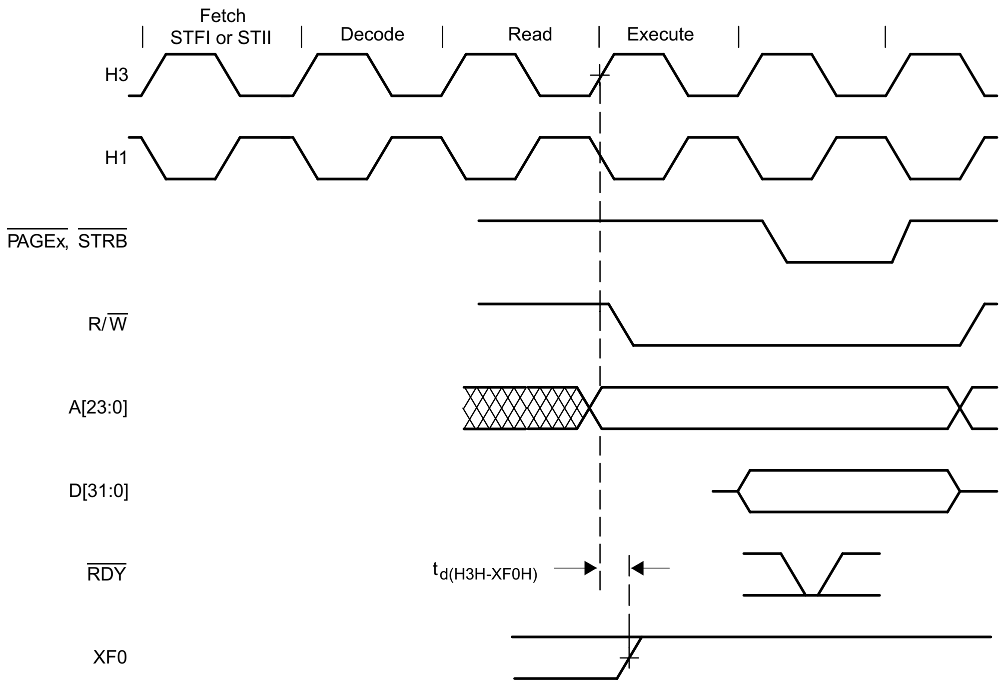


Figure 9. Timing for XF0 When Executing an STFI or STII

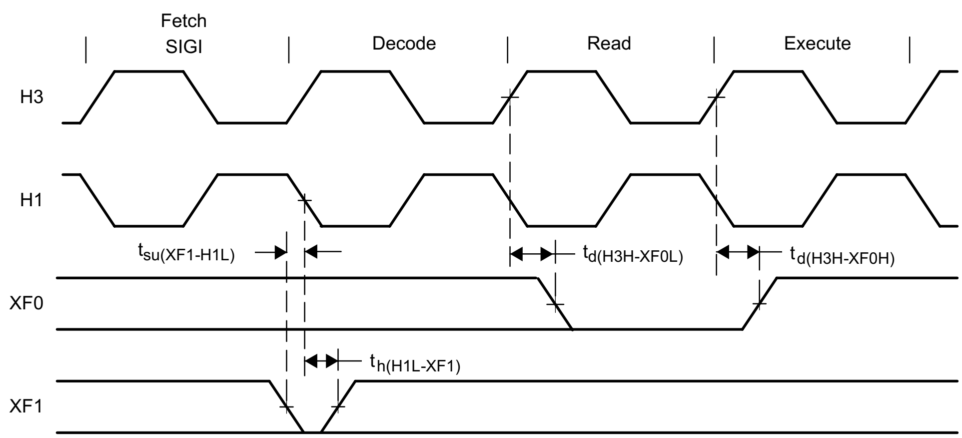
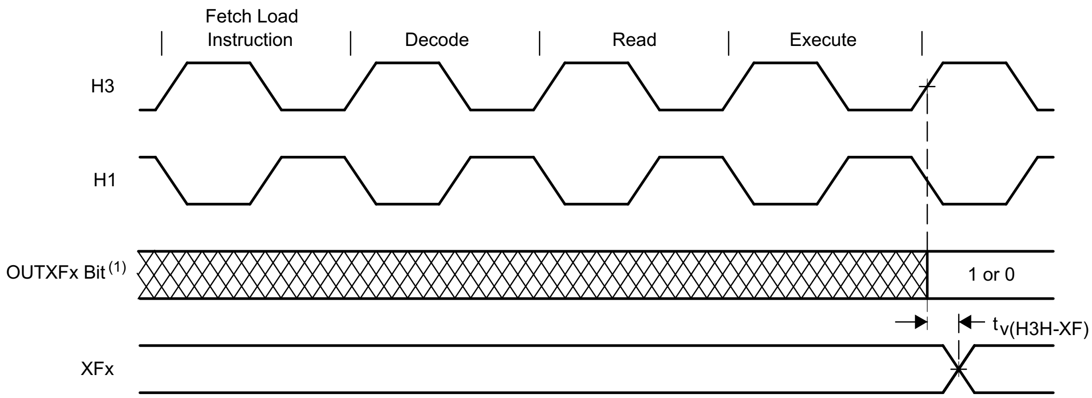


Figure 10. Timing for XF0 and XF1 When Executing SIGI

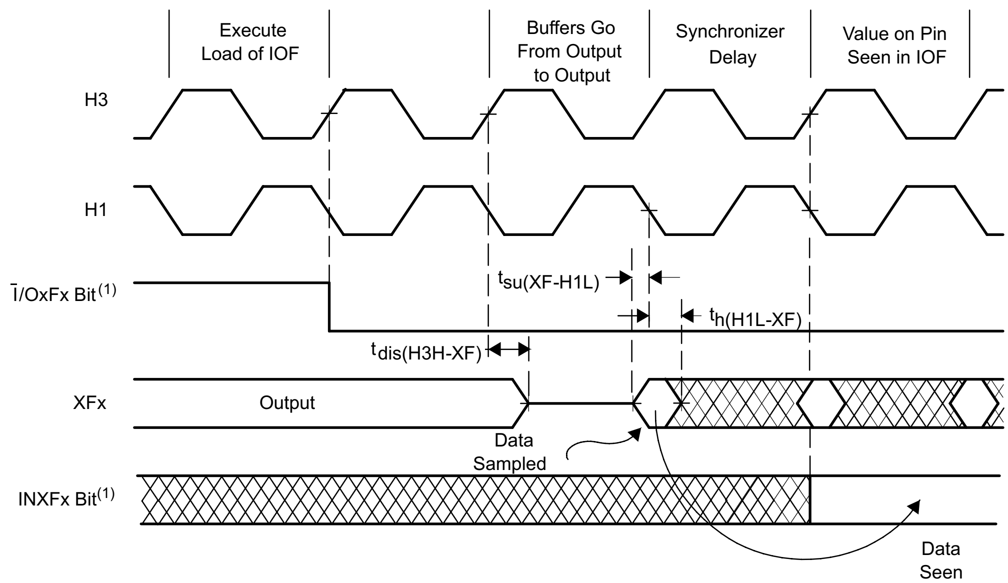
Parameter Measurement Information (continued)



1. OUTXFx represents either bit 2 or 6 of the IOF register

.

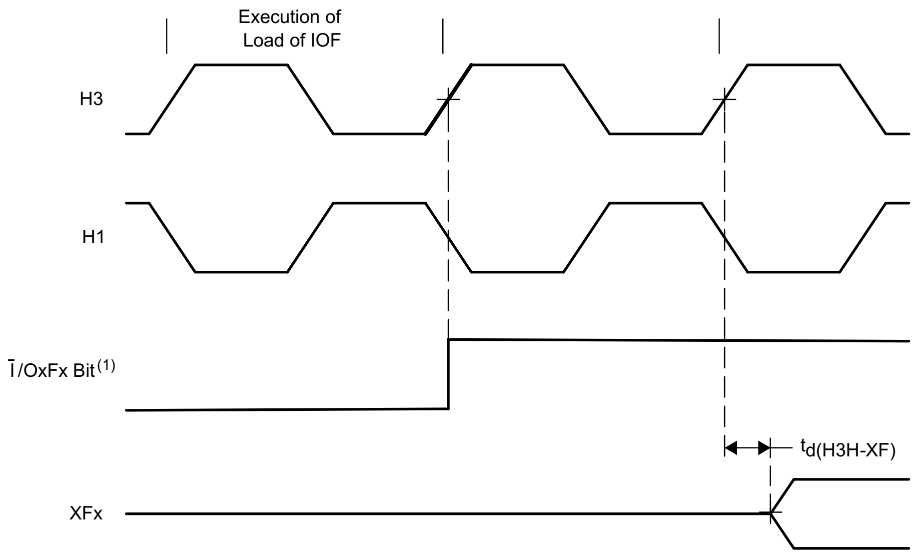
Figure 11. Timing for Loading XF Register When Configured as an Output Pin



1. I/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

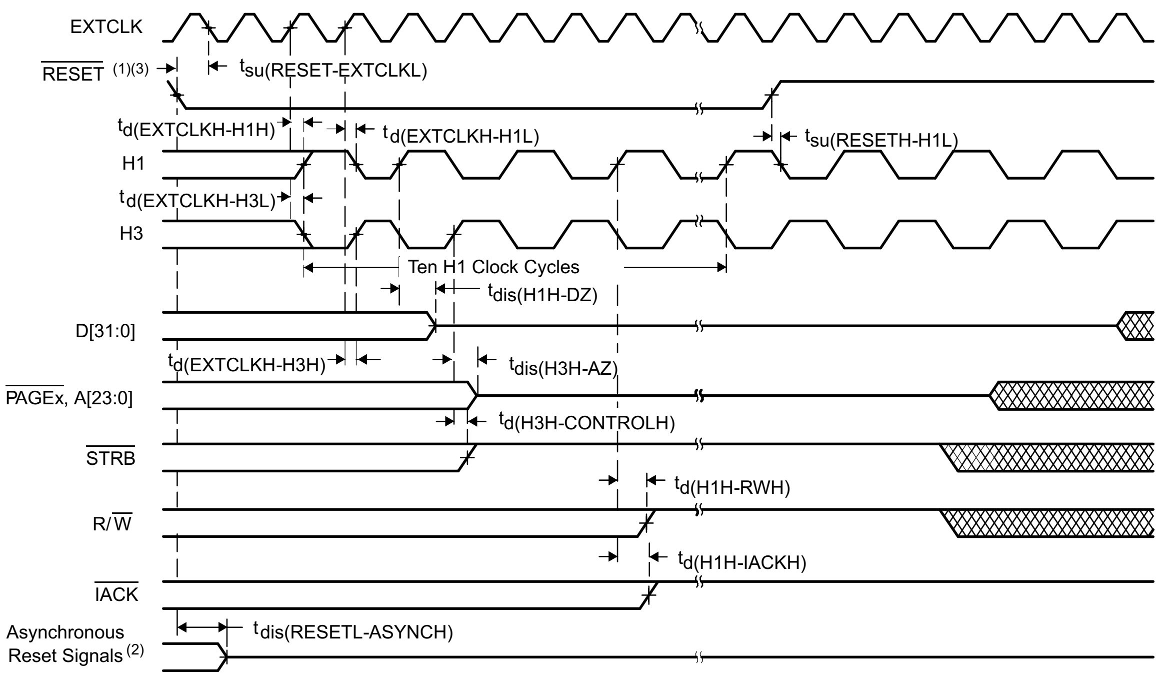
Figure 12. Timing for Changing XFx from Output to Input Mode

Parameter Measurement Information (continued)



1. I/OxFx represents either bit 1 or bit 5 of the IOF register.

Figure 13. Timing for Changing XFx from Input to Output Mode



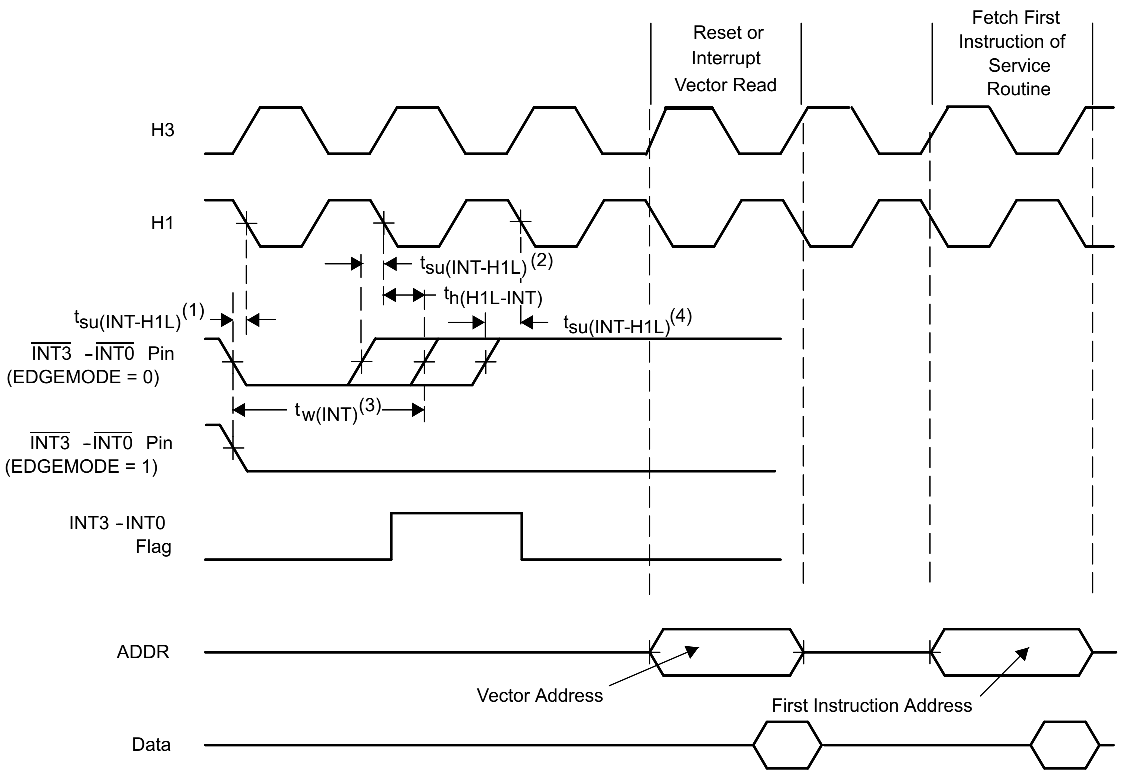
1. Clock circuit is configured in C31-compatible divide-by-2 mode. If configured for x1 mode, EXTCLK directly drives H3.
2. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
3. RESET is a synchronous input that can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.

In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.

The address and PAGE3 to PAGE0 outputs are placed in a high-impedance state during reset requiring a nominal 10- to 22-kΩ pullup. If not, undesirable spurious reads can occur when these outputs are not driven.

Figure 14. RESET Timing

Parameter Measurement Information (continued)



1. Falling edge of H1 just detects $\overline{\text{INTx}}$ falling edge.
2. Falling edge of H1 detects second $\overline{\text{INTx}}$ low, however flag clear takes precedence.
3. Nominal width
4. Falling edge of H1 misses previous $\overline{\text{INTx}}$ low as $\overline{\text{INTx}}$ rises.

Figure 15. $\overline{\text{INT3}}$ to $\overline{\text{INT0}}$ Response Timing

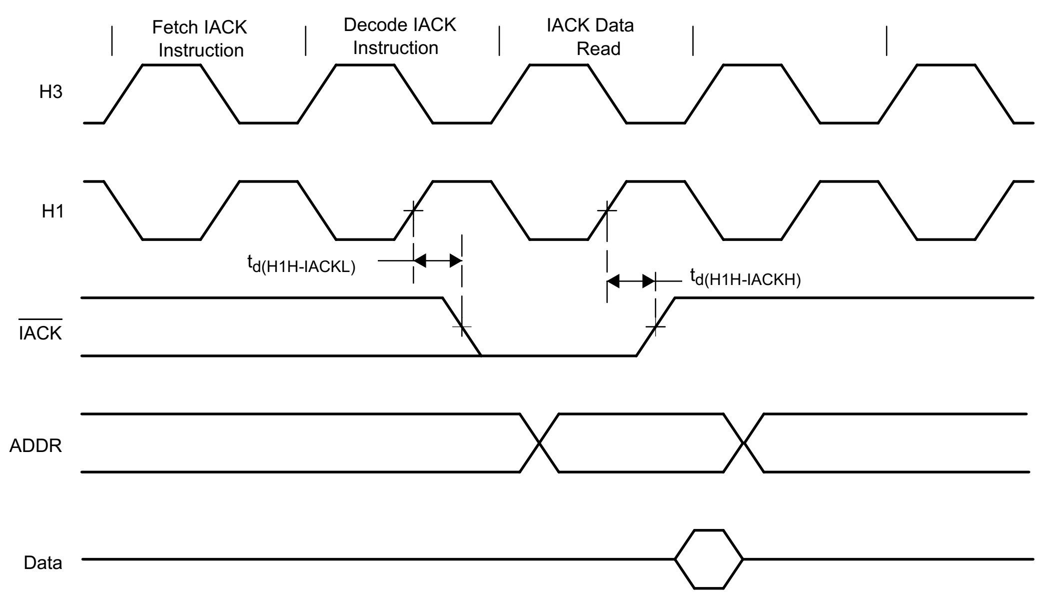
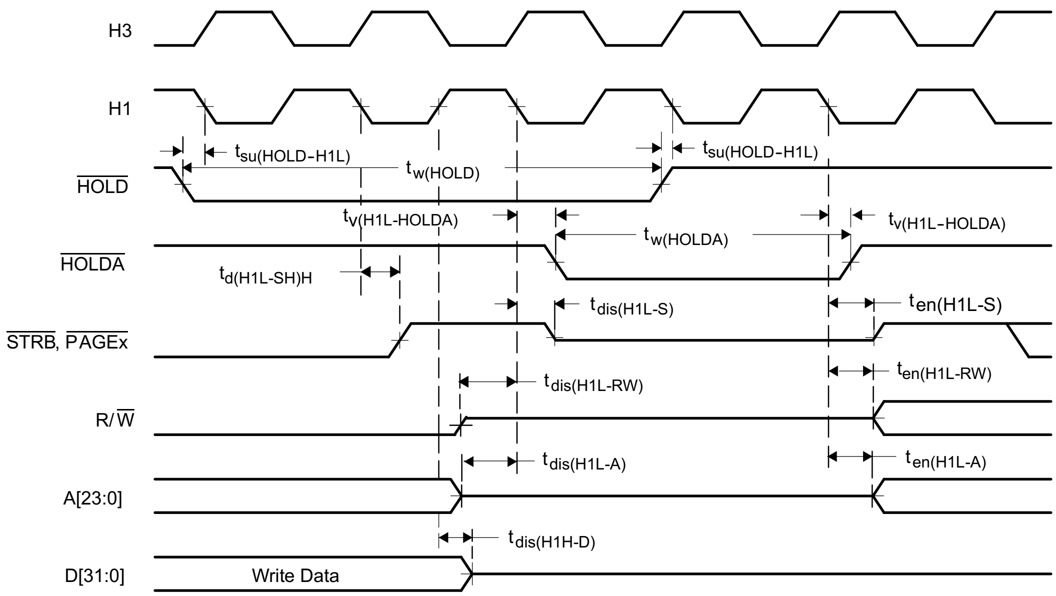


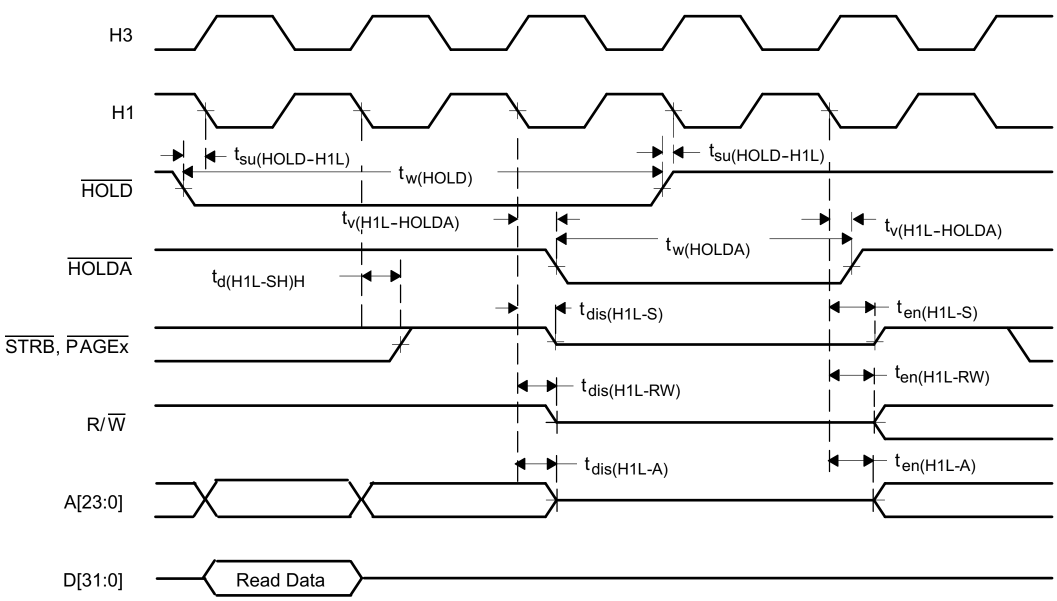
Figure 16. Interrupt Acknowledge ($\overline{\text{IACK}}$) Timing

Parameter Measurement Information (continued)



HOLDA goes low in response to HOLD going low and continues to remain low until one H1 cycle after HOLD goes back high.

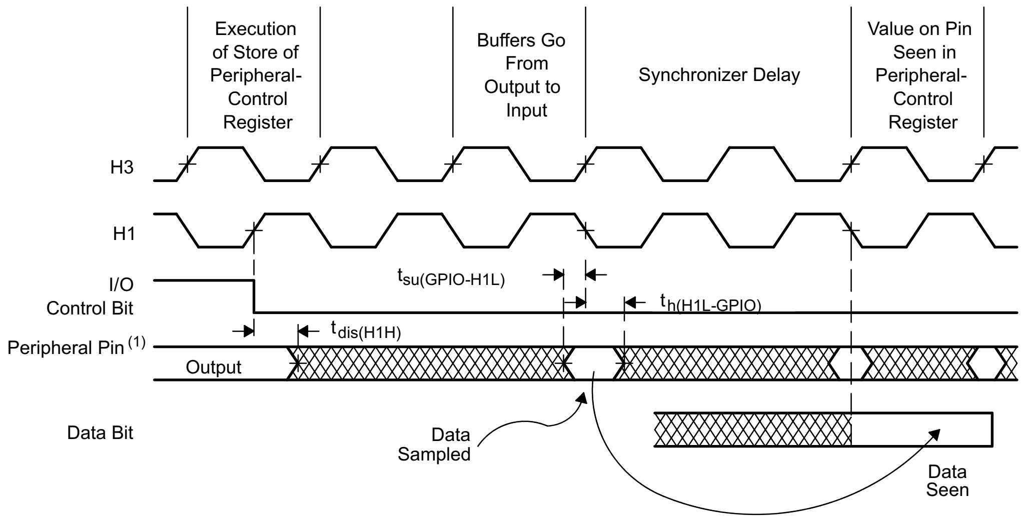
Figure 17. Timing for HOLD/HOLDA (After Write)



HOLDA goes low in response to HOLD going low and continues to remain low until one H1 cycle after HOLD goes back high.

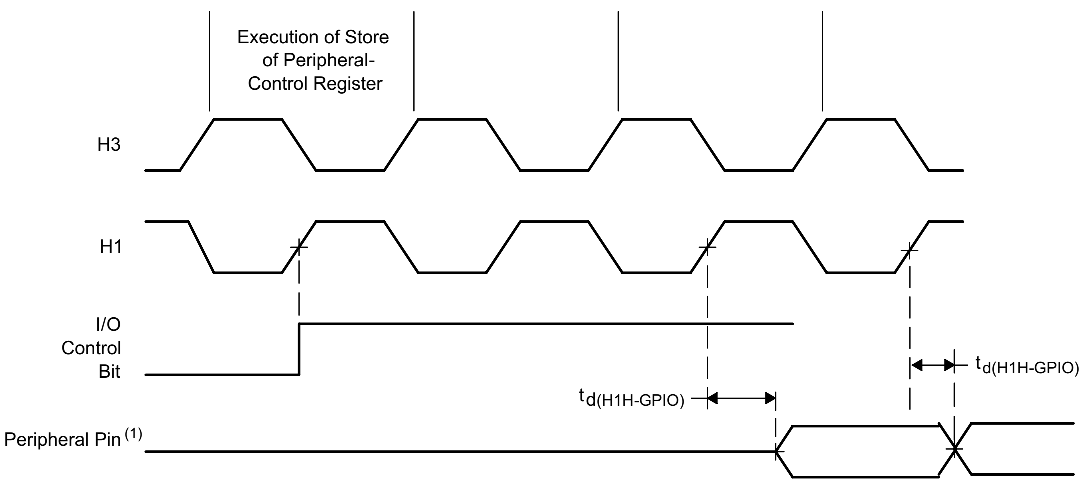
Figure 18. Timing for HOLD/HOLDA (After Read)

Parameter Measurement Information (continued)



1. Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 19. Change of Peripheral Pin from General-Purpose Output to Input Mode Timing



1. Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 20. Change of Peripheral Pin from General-Purpose Input to Output Mode Timing

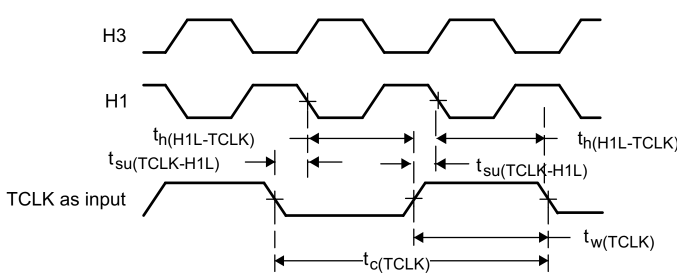


Figure 21. Timer Pin Timing, Input

Parameter Measurement Information (continued)

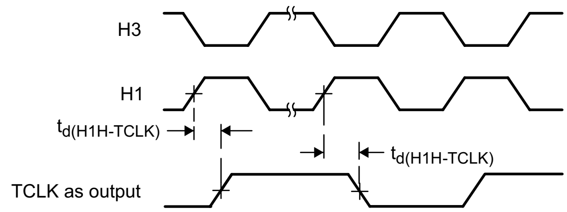
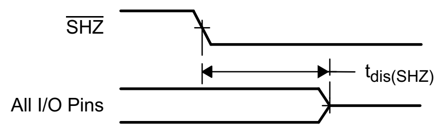


Figure 22. Timer Pin Timing, Output



Enabling $\overline{SHZ}$ destroys SMx320VC33 register and memory contents. Assert $\overline{SHZ}$ = 1 and reset the SMx320VC33 to restore it to a known condition.

Figure 23. Timing for $\overline{SHZ}$

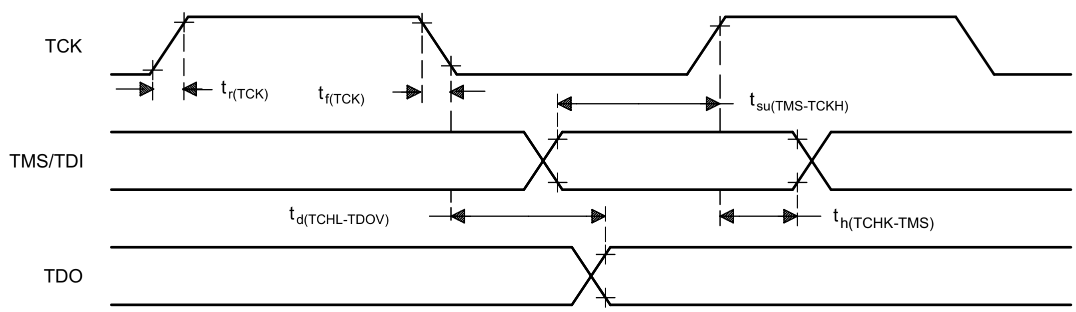
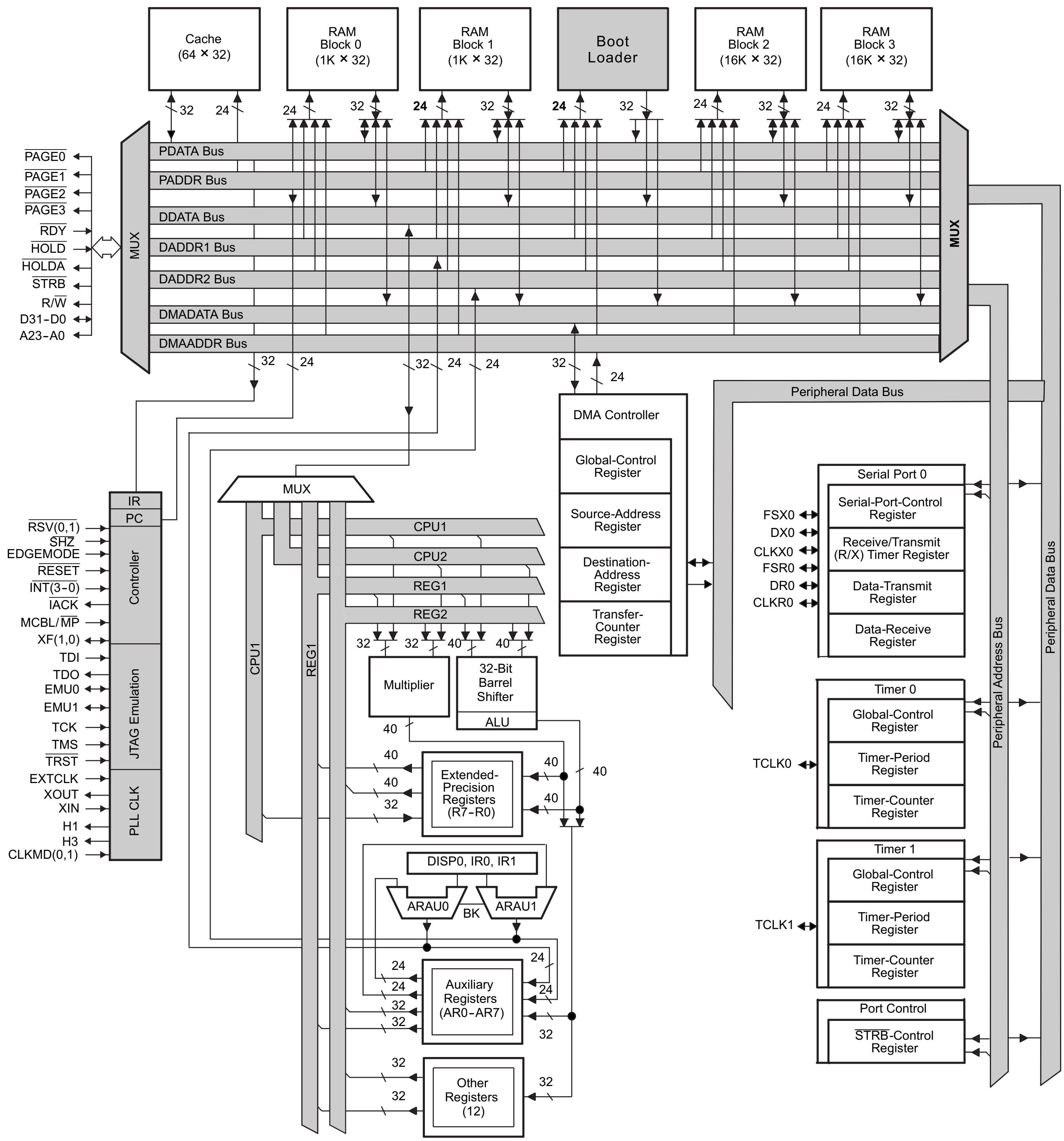


Figure 24. IEEE-1149.1 Test Access Port Timings

8 Detailed Description

8.1 Functional Block Diagram



8.2 Feature Description

8.2.1 JTAG Scan-Based Emulation Logic

The 320VC33 contains a JTAG port for CPU emulation within a chain of any number of other JTAG devices. The JTAG port on this device does not include a pin-by-pin boundary scan for point-to-point board level test. The Boundary Scan tap input and output is internally connected with a single dummy register allowing loop back tests to be performed through that JTAG domain.

The JTAG emulation port of this device also includes two additional pins, EMU0 and EMU1, for global control of multiple processors conforming to the TI emulation standard. These pins are open collector-type outputs which are wire ORed and tied high with a pullup. Non-TI emulation devices should not be connected to these pins.

The VC33 instruction register is 8 bits long. Table 1 shows the instructions code. The uses of SAMPLE and HIGHZ opcodes, though defined, have no meaning for the SMx320VC33, which has no boundary scan. For example, HIGHZ affects only the dummy cell (no meaning) and does not put the device pins in a high-impedance state.

Table 1. Boundary-Scan Instruction Code

INSTRUCTION NAME	INSTRUCTION CODE
EXTEST	00000000
BYPASS	11111111
SAMPLE	00000010 (1)
HIGHZ	00000110 (1)
PRIVATE1 (2)	00000011
PRIVATE2 (2)	00100000
PRIVATE3 (2)	00100001
PRIVATE4 (2)	00100010
PRIVATE5 (2)	00100011
PRIVATE6 (2)	00100100
PRIVATE7 (2)	00100101
PRIVATE8 (2)	00100110
PRIVATE9 (2)	00100111
PRIVATE10 (2)	00101000
PRIVATE11 (2)	00101001

(1) Boundary is only one dummy cell.
(2) Use of private opcodes could cause the device to operate in an unexpected manner.

8.2.2 Clock Generator

The clock generator provides clocks to the VC33 device and consists of an internal oscillator and a PLL circuit. The clock generator requires a reference clock input, which can be provided by using a crystal resonator with the internal oscillator, or from an external clock source. The PLL circuit generates the device clock by multiplying the reference clock frequency by a x5 scale factor, allowing use of a clock source with a lower frequency than that of the CPU. The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

8.2.3 PLL and Clock Oscillator Control

The clock mode control pins are decoded into four operational modes as shown in Figure 25. These modes control clock divide ratios, oscillator, and PLL power (see Table 2).

When an external clock input or crystal is connected, the opposite unused input is simply grounded. An XOR gate then passes one of the two signal sources to the PLL stage. This allows the direct injection of a clock reference into EXTCLK, or 1- to 20-MHz crystals and ceramic resonators with the oscillator circuit. The two clock sources include:

- A crystal oscillator circuit, where a crystal or ceramic resonator is connected across the XOUT and XIN pins and EXTCLK is grounded.
- An external clock input, where an external clock source is directly connected to the EXTCLK pin, and XOUT

is left unconnected and XIN is grounded.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. When the PLL is locked, it continues to track and maintain synchronization with the input signal. The PLL is a simple ×5 reference multiplier with bypass and power control.

The clock divider, under CPU control, reduces the clock reference by 1 (MAXSPEED), 1/16 (LOWPOWER), or clock stop (IDLE2). Wake-up from the IDLE2 state is accomplished by a RESET or interrupt pin logic-low state.

A divide-by-two TMS320C31 equivalent mode of operation is also provided. In this case, the clock output reference is further divided by two with clock synchronization being determined by the timing of RESET falling relative to the present H1/H3 state.

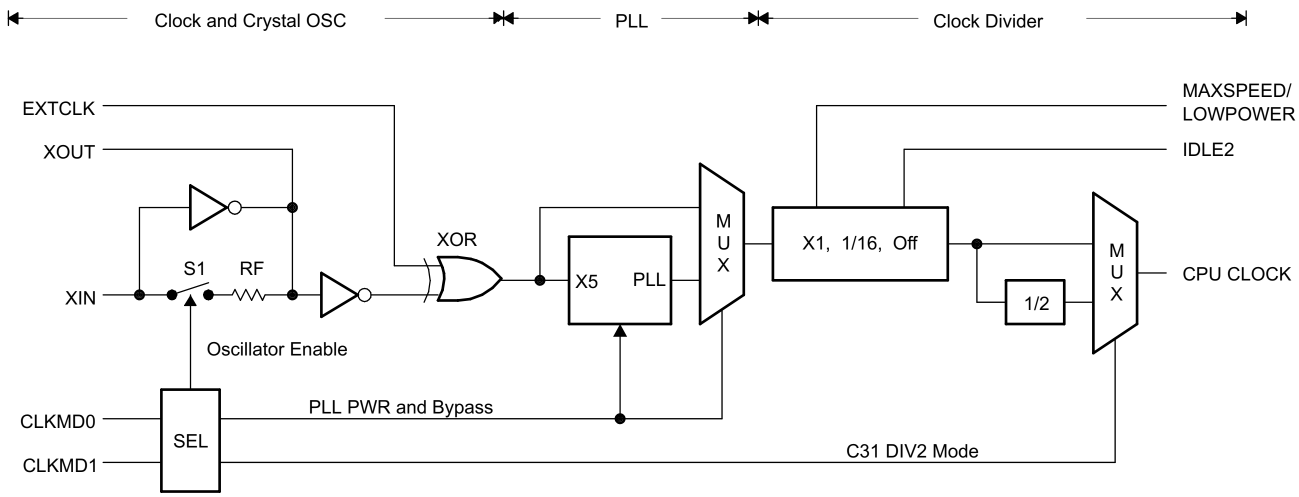


Figure 25. Clock Generation

Table 2. Clock Mode Select Pins

CLKMD0	CLKMD1	FEEDBACK	PLLPWR	RATIO	NOTES
0	0	Off	Off	1	Fully static, very-low power
0	1	On	Off	1/2	Oscillator enabled
1	0	On	Off	1	Oscillator enabled
1	1	On	On	5	2 mA at 60 MHz, 1.8-V PLL power. Oscillator enabled

Typical crystals in the 8- to 30-MHz range have a series resistance of 25 Ω, which increases below 8 MHz. To maintain proper filtering and phase relationships, R_d and Z_{out} of the oscillator circuit should be 10x to 40x that of the crystal. TI recommends a series compensation resistor (R_d), shown in Figure 26, when using lower frequency crystals. The XOUT output, the square wave inverse of XIN, is then filtered by the XOUT output impedance, C1 load capacitor, and R_d (if present). The crystal and C2 input load capacitor then refilters this signal, resulting in a XIN signal that is 75% to 85% of the oscillator supply voltage.

NOTE

Some ceramic resonators are available in a low-cost, three-pin package that includes C1 and C2 internally. Typically, ceramic resonators do not provide the frequency accuracy of crystals.

Better PLL stability can be achieved using the optional power supply isolation circuit shown in Figure 26. A similar filter can be used to isolate the $PLLV_{SS}$, as shown in Figure 27. $PLLV_{DD}$ can also be directly connected to CV_{DD}.

Table 3. Typical Crystal Circuit Loading

FREQUENCY (MHz)	R_d (Ω)	C1 (pF)	C2 (pF)	CL(1) (pF)	RL(1) (Ω)
2	4.7k	18	18	12	200
5	2.2k	18	18	12	60
10	470	15	15	12	30
15	0	15	12	12	25
20	0	9	9	10	25

(1) CL and RL are typical internal series load capacitance and resistance of the crystal.

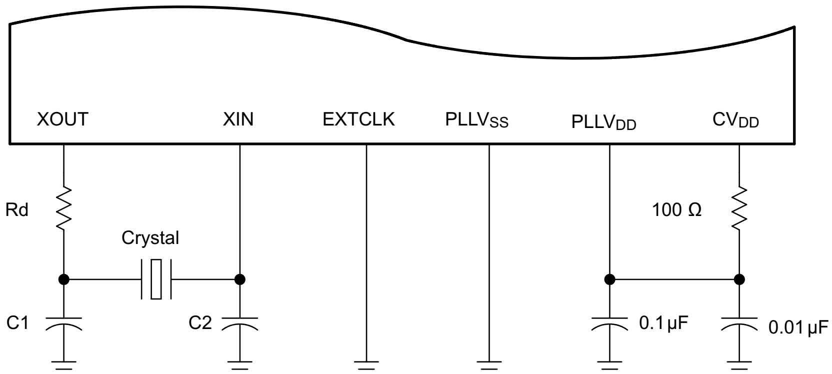


Figure 26. Self-Oscillation Mode

8.2.4 PLL Isolation

The internal PLL supplies can be directly connected to CVDD and VSS (0-Ω case), partially isolated as shown in Figure 26, or fully isolated as shown in Figure 27. The RC network prevents the PLL supplies from turning high-frequency noise in the CVDD and VSS supplies into jitter.

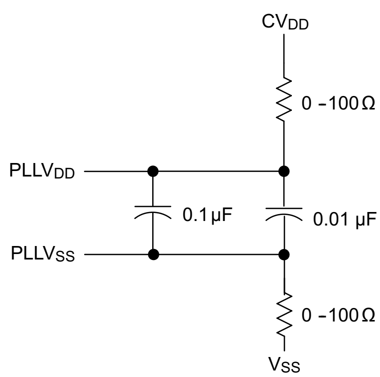


Figure 27. PLL Isolation Circuit Diagram

8.2.5 Clock and PLL Considerations on Initialization

On power up, the CPU clock divide mode can be in MAXSPEED, LOPOWER, or IDLE2, or the PLL could be in an undefined mode. RESET falling in the presence of a valid CPU clock is used to clear this state, after which the device will synchronously terminate any external activity.

The 5× Fclkin PLL of the 320VC33 contains an 8-bit PLL–LOCK counter that causes the PLL to output a frequency of Fclkin / 2 during the initial ramp. However, this counter does not increment while RESET is low or in the absence of an input clock. A minimum of 256 input clocks are required before the first falling edge of reset for the PLL to output to clear this counter. The following describes the setup and behavior that is observed. Power is applied to the DSP with RESET low and the input clock high or low. A clock is applied (RESET is still low) and the PLL appears to lock onto the input clock, producing the expected ×5 output frequency. RESET is driven high and the PLL output immediately drops to Fclkin / 2 for up to 256 input cycles or 128 of the Fclkin / 2 output cycles. The PLL/CPU clock then switches to ×5 mode.

The switch over is synchronous and does not create a clock glitch, so the only effect is that the CPU runs slow for up to the first 128 cycles after reset goes high. After the PLL has stabilized, the counter remains cleared and subsequent resets do not exhibit this condition.

Systems that are not using the crystal oscillator may be required to supply a current of 250 mA per DSP if full power is applied with no clock source. This extra current condition is a result of uninitialized internal logic within the DSP core and is corrected when the CPU sees a minimum of four internal clocks. The crystal oscillator is typically immune to this condition since the oscilator and core circuitry become semi-functional at CVDD = 1 V where the fault current is considerably lower. An alternate clock pulse can also be applied to either the EXTCLK or XIN clock input pins.

8.2.6 EDGEMODE

When EDGEMODE = 1, a sampled digital delay line is decoded to generate a pulse on the falling edge of the interrupt pin. To ensure interrupt recognition, input signal logic-high and logic-low states must be held longer than the synchronizer delay of one CPU clock cycle. Holding these inputs to no less than two cycles in both the logic-low and logic-high states is sufficient.

When EDGEMODE = 0, a logic-low interrupt pin continually sets the corresponding interrupt flag. The CPU or DMA can clear this flag within two cycles of it being set. This is the maximum interrupt width that can be applied if only one interrupt is to be recognized. The CPU can manually clear IF bits within an interrupt service routine (ISR), effectively lengthening the maximum ISR width.

After reset, EDGEMODE is temporarily disabled, allowing logic-low INT pins to be detected for bootload operation.

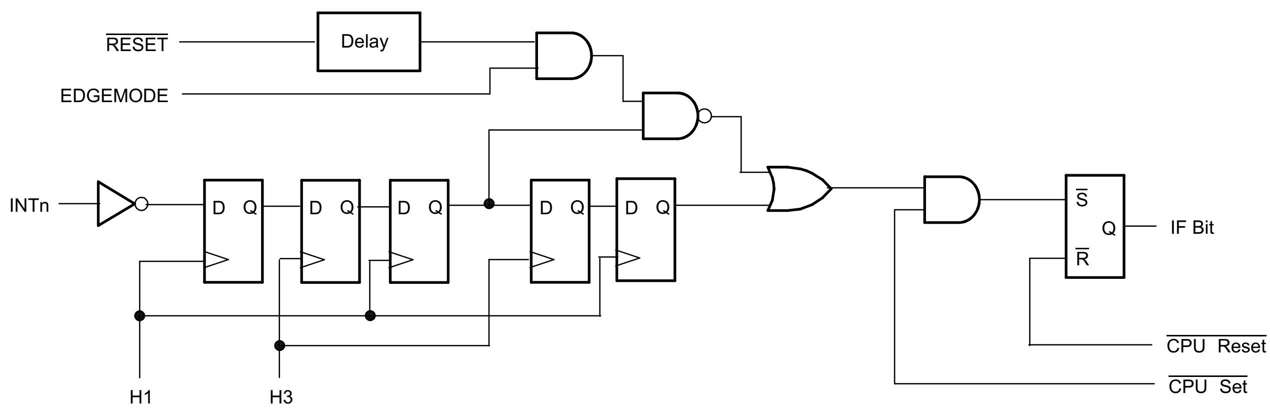


Figure 28. EDGEMODE and Interrupt Flag Circuit

8.2.7 Reset Operation

When RESET is applied, the CPU attempts to safely exit any pending read or write operations that may be in progress. This can take as much as 10 CPU cycles, after which, the address, data, and control pins are in an inactive or high-impedance state.

When both RESET and SHZ are applied, the device immediately enters the reset state with the pins held in high-impedance mode. SHZ should then be disabled at least 10 CPU cycles before RESET is set high. SHZ can be used during power-up sequencing to prevent undefined address, data, and control pins, avoiding system conflicts.

8.2.8 PAGE0 to PAGE3 Select Lines

To facilitate simpler and higher-speed connection to external devices, the SMx320VC33 includes four predecoded select pins that have the same timings as STRB.These pins are decoded from A22, A23, and STRB and are active only during external accesses over the ranges shown in Table 4. A single bus control register controls all external bus accesses.

Table 4. PAGE0 to PAGE3 Ranges

	START	END
PAGE0	0x000000	0x3FFFFF
PAGE1	0x400000	0x7FFFFF
PAGE2	0x800000	0xBFFFFF
PAGE3	0xC00000	0xFFFFFF

8.2.9 Using External Logic With the READY Pin

The key to designing external wait-state logic is the internal bus control register and associated internal logic that logically combines the external READY pin with the much faster on-chip bus control logic. This essentially allows slow external logic to interact with the bus while easily meeting the READY input timings. Note that the combined ready signals are sampled on the rising edge of the internal H1 clock. Refer to Figure 29 for the following examples.

Example 1: A simple 0 or WTCNT wait-state decoder can be created by simply tying an address line back to the READY pin and selecting the AND option. When the tied back address is low, the bus runs with 0 wait states. When the tied back address is high, the bus is controlled by the internal wait-state counter.

By enabling the bank compare logic, proper operation is further ensured by inserting a null cycle before a read on the next bank is performed (writes are not pre-extended). This extra time can also be used by external logic to affect the feedback path.

Example 2: An N–WTCNT minimum wait-state decoder can also be created by tying back an address line to READY and logically ORing it with the internal bank compare and wait count signals. When the address pin is low, bus timing is determined by the internal WTCNT and BNKCMP settings. When the address line is high, the bus can run no faster than the WTCNT counter and is extended as long as READY is held high.

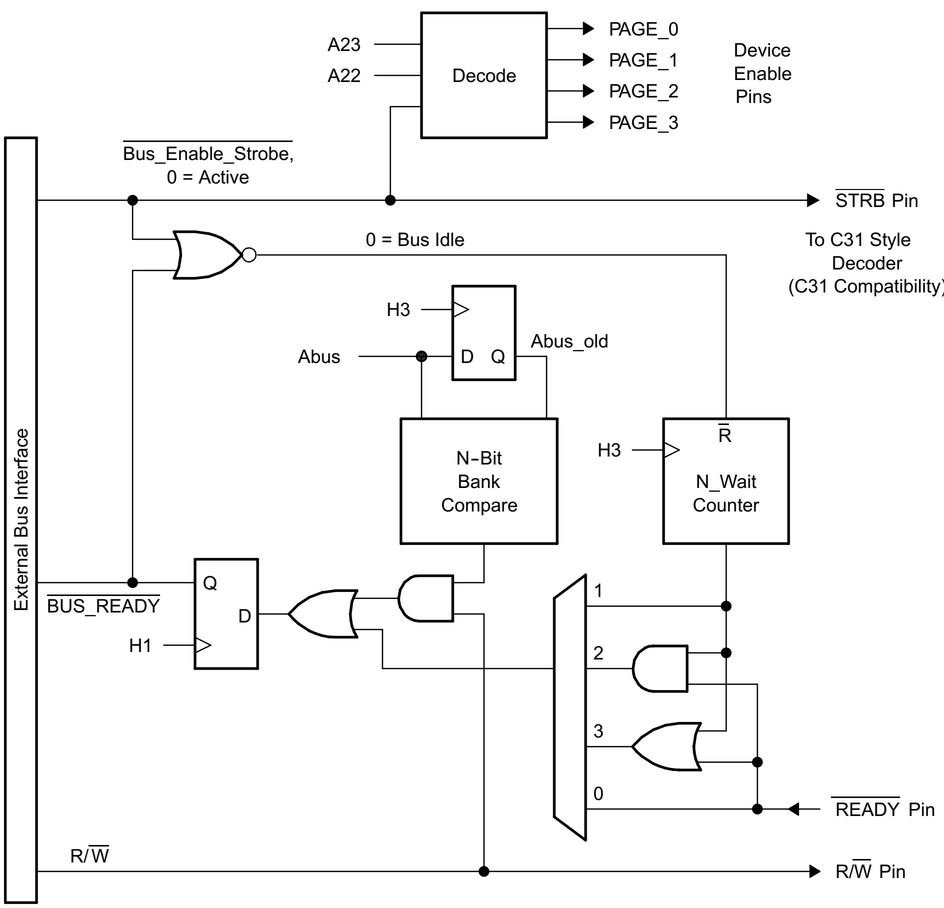


Figure 29. Internal Ready Logic, Simplified Diagram

Table 5. MUX Select (Bus Control Register Bits 4 and 3)

BIT 4	BIT 3	RESULTS
0	0	Ignore internal wait counter and use only external $\overline{\text{READY}}$
0	1	Use only internal wait counter and ignore ready pin
1	0	Logical AND internal wait counter with ready pin
1	1	Logical OR internal wait counter with ready pin (reset default)

8.2.10 Posted Writes

External writes are effectively “posted” to the bus, which then acts like an output latch until the write completes. Therefore, if the application code is executing internally, it can perform a very-slow external write with no penalty because the bus acts like it has a one-level-deep write FIFO.

8.2.11 Data Bus I/O Buffer

The circuit shown in Figure 30 is incorporated into each data pin to lightly “hold” the last driven value on the data bus pins when the DSP or an external device is not actively driving the bus. Each bus keeper is built from a three-state driver with nominal 15-kΩ output resistance which is fed back to the input in a positive feedback configuration. The resistance-isolated driver then pulls the output in one direction or the other keeping the last driven value. This circuit is enabled in all functional modes and is only disabled when $\overline{\text{SHZ}}$ is pulled low.

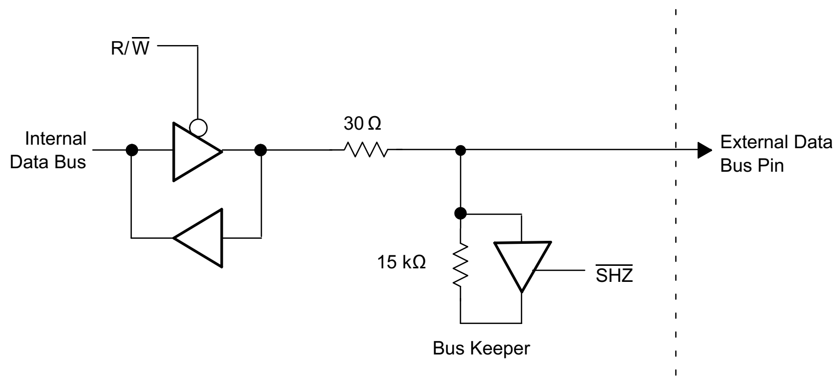


Figure 30. Bus Keeper Circuit

For an external device to change the state of these pins, it must be able to drive a small dc current until the driver threshold is crossed. At the crossover point, the driver changes state, agreeing with the external driver and assisting the change. The voltage threshold of the bus keeper is approximately at 50% of the DV_{DD} supply voltage. The typical output impedance of 30 Ω for all SMx320VC33 I/O pins is easily capable of meeting this requirement.

8.2.12 Bootloader Operation

When MCBL/$\overline{\text{MP}}$ = 1, an internal ROM is decoded into the address range of 0x000000 to 0x000FFF. Therefore, when reset occurs, execution begins within the internal ROM program and vector space. No external activity is evident until one of the boot options is enabled. These options are enabled by pulling an external interrupt pin low, which the boot-load software then detects, causing a particular routine to be executed (see Table 6).

Table 6. $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ Sources

ACTIVE INTERRUPT	ADDRESS/SOURCE WHERE BOOT DATA IS READ FROM	DATA FORMAT
INT0	0x001000	8-, 16-, or 32-bit width
INT1	0x400000	8-, 16-, or 32-bit width
INT2	0xFFF000	8-, 16-, or 32-bit width
INT3	Serial port	32-bit, external clock, and frame synch

When MCBL/$\overline{MP}$ = 1, the reset and interrupt vectors are hard-coded within the internal ROM. Because this is a read-only device, these vectors cannot be modified. To enable user-defined interrupt routines, the internal vectors contain fixed values that point to an internal section of SRAM beginning at 0x809FC1. Code execution begins at these locations, so it is important to place branch instructions (to the interrupt routine) at these locations and not vectors.

The bootloader program requires a small stack space for calls and returns. Two SRAM locations at 0x809800 and 0x809801 are used for this stack. Do not boot load data into these locations because it will corrupt the bootloader program runtime stack. After the boot-load operation is complete, a program can reclaim these locations. The simplest solution is to begin a program stack or uninitialized data section at 0x809800.

For additional details on bootloader operation including the bootloader source code, see the *TMS320C3x User's Guide* (SPRU031).

A bit I/O line or external logic can be used to safely disable the MCBL mode after bootloading is complete. However, to ensure proper operation, the CPU should not be currently executing code or using external data as the change takes place. In the following example, the XF0 pin is tri-state on reset, which allows the pullup resistor to place the DSP in MCBL mode. The following code, placed at the beginning of an application then causes the XF0 pin to become an active-logic-low output, changing the DSP mode to MP. The cache-enable and RPTS instructions are used because they cause the LDI instruction to be executed multiple times even though it has been fetched only once (before the mode change). In other words, the RPTS instruction acts as a one-level-deep program cache for externally executed code. If the application code is to be executed from internal RAM, no special provisions are needed.

```
LDI     8000h,ST ; Enable the cache
RPTS    4        ; RPTS will fetch the following opcode 1 time
LDI     2h, IOF  ; Drive MCBL/MP=0 for several cycles allowing
                 ; the pipeline to clear
```

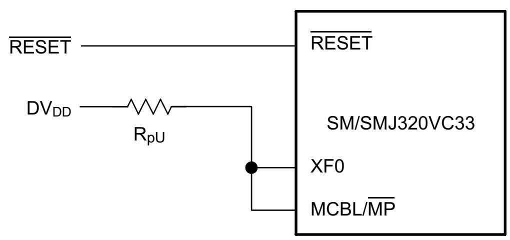


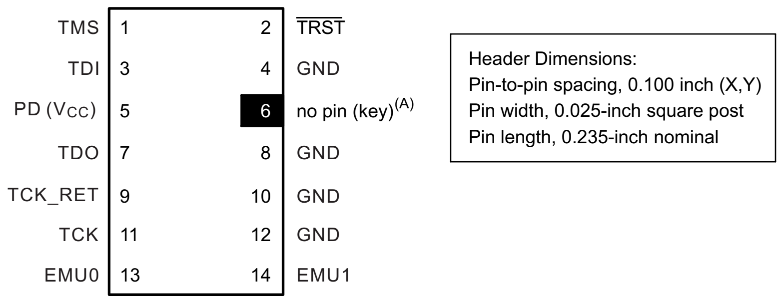
Figure 31. Changing Bootload Select Pin

8.2.13 JTAG Emulation

Though the 320VC33 contains a JTAG debug port which allows multiple JTAG enabled chips to be daisy-chained, boundary scan of the pins is not supported. If the pin scan path is selected, it will be routed through a null register with a length of one. For additional information concerning the emulation interface, see *JTAG/MPSD Emulation Technical Reference* (SPDU079).

8.2.14 Designing a Target System Emulator Connector (14-Pin Header)

JTAG target devices support emulation through a dedicated emulation port. This port is a superset of the test access port standard and is accessed by the emulator. To communicate with the emulator, the target system must have a 14-pin header (two rows of seven pins) with the connections that are shown in Figure 32. Table 7 describes the emulation signals.



A. While the corresponding female position on the cable connector is plugged to prevent improper connection, the cable lead for pin 6 is present in the cable and is grounded, as shown in the schematics and wiring diagrams in this data sheet.

Figure 32. 14-Pin Header Signals and Header Dimensions

Table 7. 14-Pin Header Signal Descriptions

SIGNAL	DESCRIPTION	EMULATOR(1) STATE	TARGET(1) STATE
TMS(2)	Test mode select	O	I
TDI	Test data input	O	I
TDO	Test data output	I	O
TCK	Test clock. TCK is a 10.368-MHz clock source from the emulation cable pod. This signal can be used to drive the system test clock	O	I
$\overline{\text{TRST}}$(3)	Test reset	O	I
EMU0(2)(4)	Emulation pin 0	I	I/O
EMU1(2)(4)	Emulation pin 1	I	I/O
PD(V_{CC})	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to V_{CC} in the target system.	I	O
TCK_RET	Test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	I	O
GND	Ground	—	—

(1) I = Input; O = Output
(2) Use 1- to 50-kΩ pullups for TMS, EMU0, and EMU1.
(3) Use 1- to 50-kΩ pulldown for $\overline{\text{TRST}}$. Do not use pullup resistors on $\overline{\text{TRST}}$: it has an internal pulldown device. In a low-noise environment, $\overline{\text{TRST}}$ can be left floating. In a high-noise environment, an additional pulldown resistor may be needed. (The size of this resistor should be based on electrical current considerations.)
(4) EMU0 and EMU1 are I/O drivers configured as open-drain (open-collector) drivers. They are used as bidirectional signals for emulation global start and stop.

Although other headers can be used, recommended parts include: straight header, unshrouded DuPont™ connector systems part numbers:

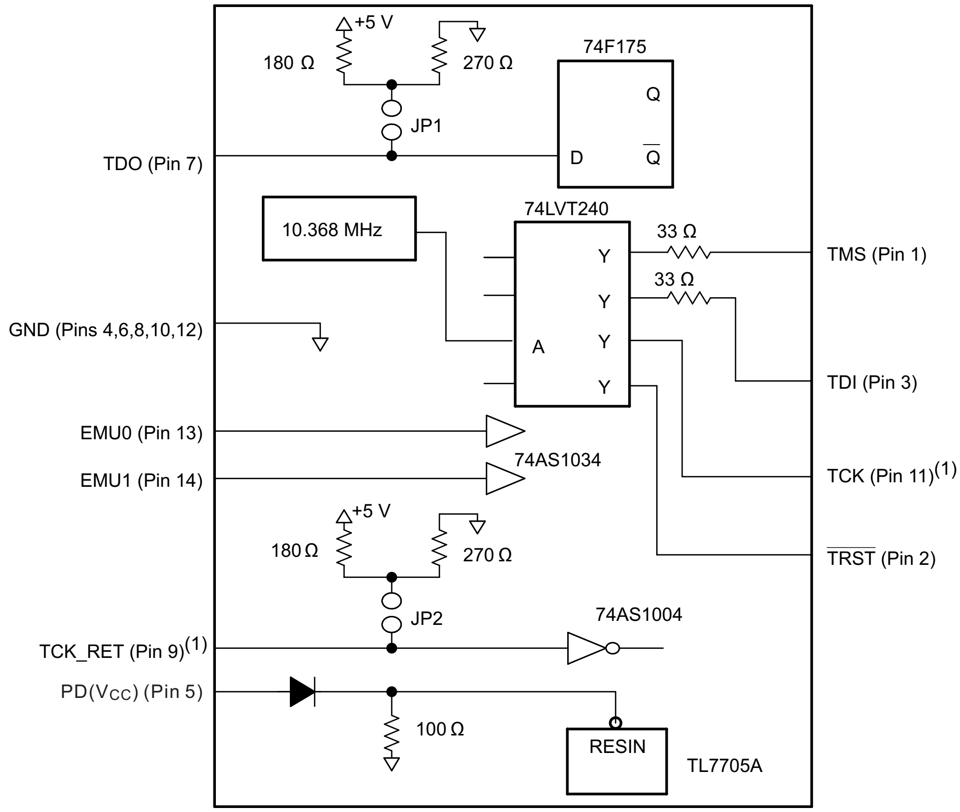
- 65610–114
- 65611–114
- 67996–114
- 67997–114

8.2.15 JTAG Emulator Cable Pod Logic

Figure 33 shows a portion of the emulator cable pod. The functional features of the pod are as follows:

- Signals TDO and TCK_RET can be parallel-terminated inside the pod if required by the application. By default, these signals are not terminated.
- Signal TCK is driven with a 74LVT240 device. Because of the high-current drive (32 mA I_{OL}/I_{OH}), this signal can be parallel-terminated. If TCK is tied to TCK_RET, the parallel terminator in the pod can be used.
- Signals TMS and TDI can be generated from the falling edge of TCK_RET, according to the bus slave device timing rules.
- Signals TMS and TDI are series-terminated to reduce signal reflections.

- A 10.368-MHz test clock source is provided. Another test clock can be used for greater flexibility.



1. The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.

Figure 33. JTAG Emulator Cable Pod Interface

8.2.16 Reset Timing

RESET is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 14 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

Resetting the device initializes the bus control register to seven software wait states and therefore results in slow external accesses until these registers are initialized.

HOLD is a synchronous input that can be asserted during reset. It can take nine CPU cycles before HOLDA is granted.

Timing Requirements for RESET defines the timing parameters for the RESET signal.

8.2.17 Interrupt Response TIming

The interrupt (INTx) pins are synchronized inputs that can be asserted at any time during a clock cycle. The TMS320C3x interrupts are selectable as level- or edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of the internal H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt when level mode is selected, an interrupt pulse must be set up and held such that a logic-low condition occurs for:

- A minimum of one H1 falling edge
- No more than two H1 falling edges
- Interrupt sources whose edges cannot be specified to meet the H1 falling edge setup and hold times must be

further restricted in pulse width as defined by $t_{w(INT)}$ in *Timing Requirements for $\overline{INT3}$ to $\overline{INT0}$ Response*.

When EDGEMODE = 1, the falling edge of the $\overline{INT0}$ to $\overline{INT3}$ pins are detected using synchronous logic (see Figure 28). The pulse low and high time should be two CPU clocks or greater.

The TMS320C3x can set the interrupt flag from the same source as quickly as two H1 clock cycles after it has been cleared.

If the specified timings are met, the exact sequence shown in Figure 15 occurs; otherwise, an additional delay of one clock cycle is possible.

8.2.18 Interrupt-Acknowledge Timing

The $\overline{IACK}$ output goes active on the first half-cycle (HI rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (HI rising) of the read phase of the IACK instruction.

Switching Characteristics for $\overline{IACK}$ defines the timing parameters for the $\overline{IACK}$ signal.

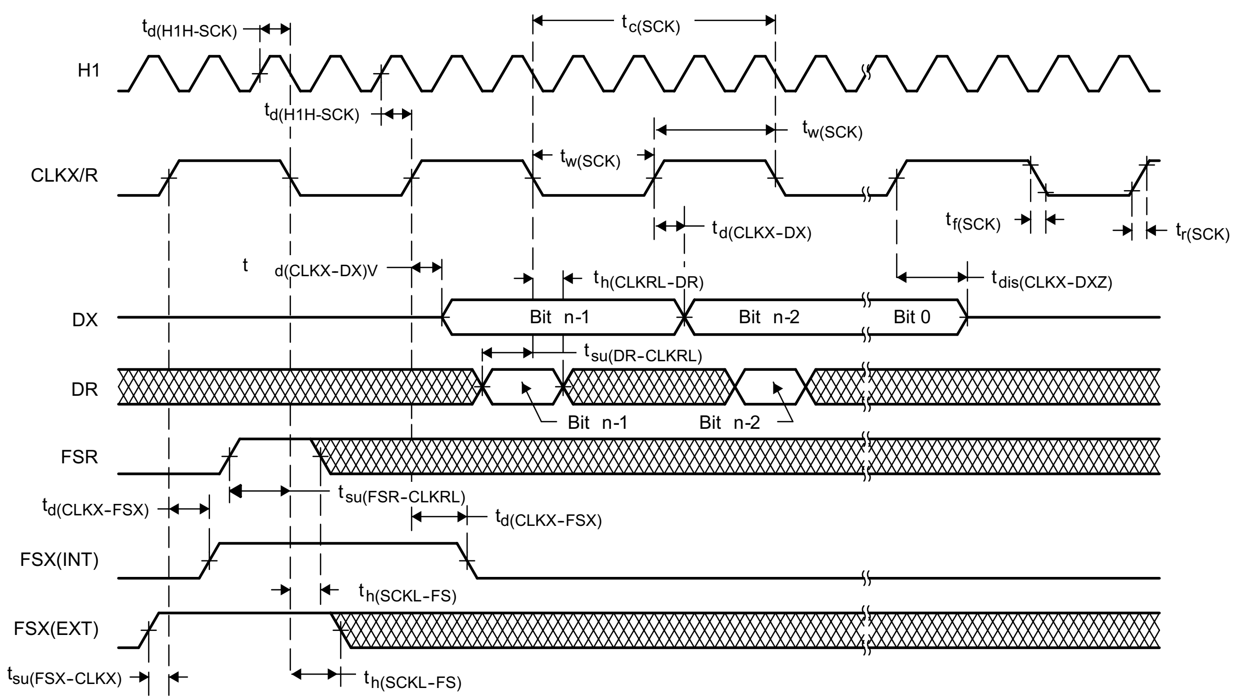
NOTE

The $\overline{IACK}$ instruction can be executed at anytime to signal an event. It is most often used within an interrupt routine to signal which interrupt has occurred. The IACK instruction must be executed to generate the IACK pulse.

8.2.19 Data-Rate Timing Modes

Unless otherwise indicated, the data-rate timings shown in Figure 34 and Figure 35 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation, see the *TMS320C3x User's Guide* (SPRU031).

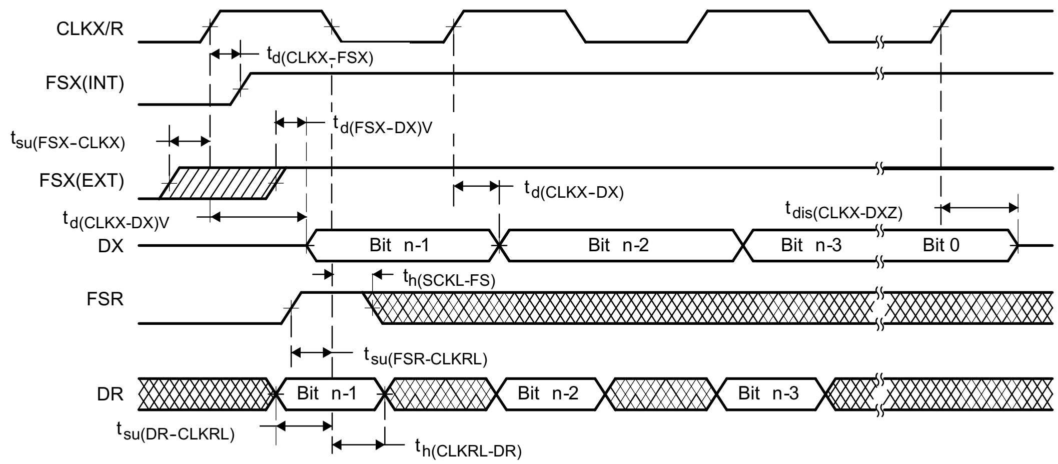
The serial-port timing parameters are defined in *Timing Requirements for Serial Port*.



Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.

Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 34. Fixed Data-Rate Mode Timing



Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.

Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 35. Variable Data-Rate Mode Timing

8.2.20 HOLD Timing

HOLD is a synchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 17 and Figure 18 occurs; otherwise, an additional delay of one clock cycle is possible.

Timing Requirements for HOLD/HOLDA defines the timing parameters for the HOLD and HOLDA signals.

The NOHOLD bit of the primary-bus control register overrides the HOLD signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

Asserting HOLD prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue (internally) until a second external write is encountered.

Figure 17, Figure 18, and the accompanying timings are for a zero wait-state bus configuration. Because HOLD is internally captured by the CPU on the H1 falling edge one cycle before the present cycle is terminated, the minimum HOLD width for any bus configuration is, therefore, WTCNT + 3. Also, do not deassert HOLD before HOLDA has been active for at least one cycle.

8.2.21 General-Purpose I/O Timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

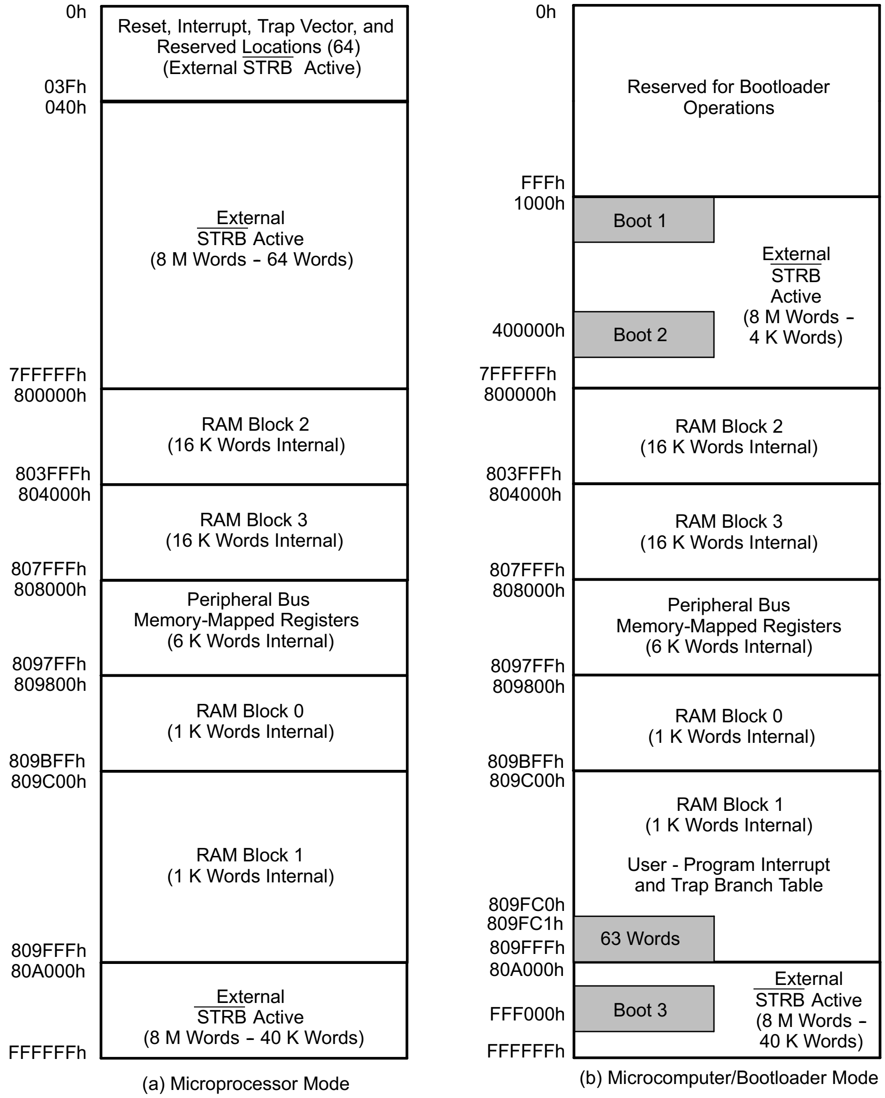
8.2.22 Peripheral Pin I/O Timing

Timing Requirements for Peripheral Pin General-Purpose I/O shows the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa.

8.2.23 Timer Pin Timing

Valid logic-level periods and polarity are specified by the contents of the internal control registers.

8.3 Register Maps



NOTE: STRB is active over all external memory ranges. PAGE0 to PAGE3 are configured as external bus strobes. These are simple decoded strobes that have no configuration registers and are active only during external bus activity over the following ranges:

Figure 36. SMx320VC33 Memory Maps

Table 8. SMx320VC33 Memory Map Active Ranges

Name	Active Range
PAGE0	0000000h – 03FFFFFh
PAGE1	0400000h – 07FFFFFh
PAGE2	0800000h – 0BFFFFFh
PAGE3	0C00000h – 0FFFFFFh
STRB	0000000h – 0FFFFFFh

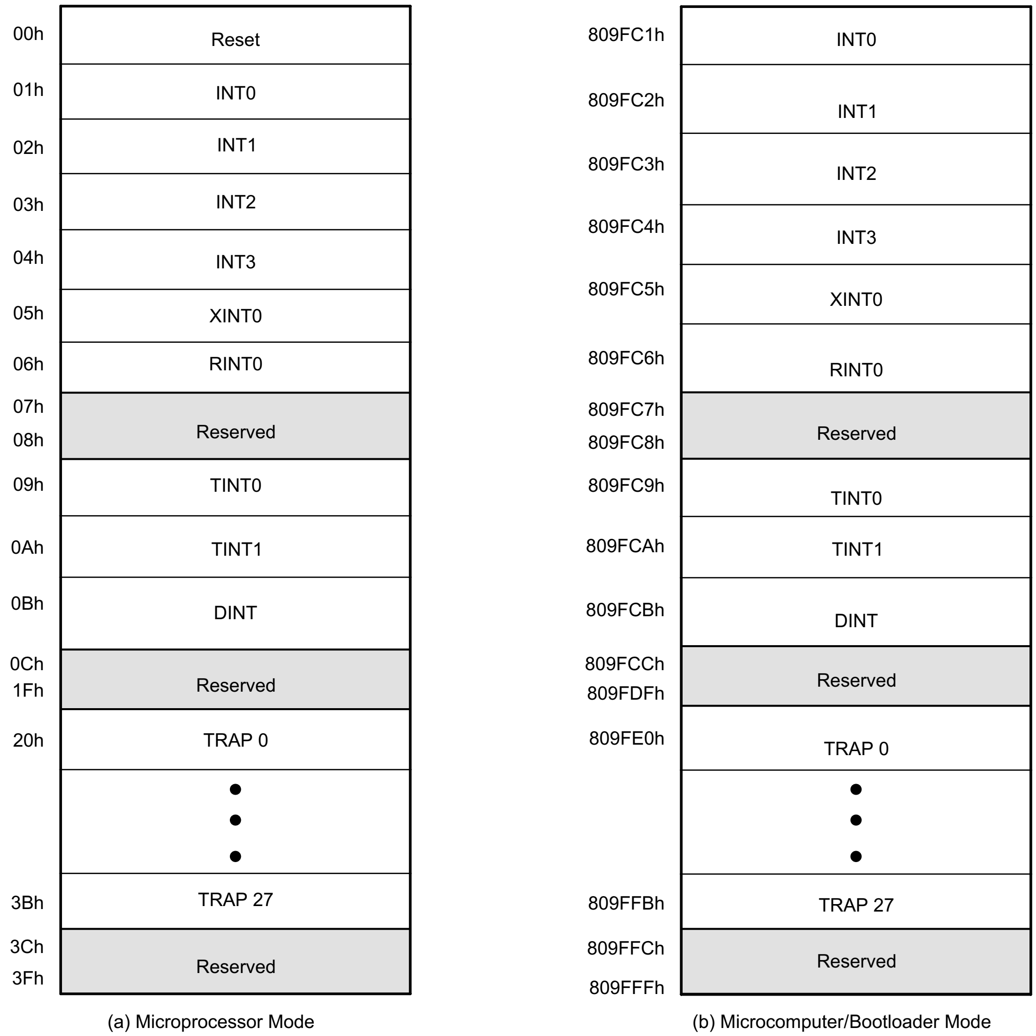


Figure 37. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

Address	Register
808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period Register
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Global Control
808042h	FSX/DX/CLKX Serial Port Control
808043h	FSR/DR/CLKR Serial Port Control
808044h	Serial R/X Timer Control
808045h	Serial R/X Timer Counter
808046h	Serial R/X Timer Period Register
808048h	Data-Transmit
80804Ch	Data-Receive
808064h	Primary-Bus Control

NOTE: Shading denotes reserved address locations.

Figure 38. Peripheral Bus Memory-Mapped Registers

9 Power Supply Recommendations

9.1 Power Sequencing Considerations

Though an internal ESD and CMOS latchup protection diode exists between CV_{DD} and DV_{DD}, it should not be considered a current-carrying device on power up. Use an external Schottky diode to prevent CV_{DD} from exceeding DV_{DD} by more than 0.7 V. The effect of this diode during power up is that if CV_{DD} is powered up first, DV_{DD} follows by one diode drop even when the DV_{DD} supply is not active.

Typical systems using LDOs of the same family type for both DV_{DD} and CV_{DD} track each other during power up. In most cases, this is acceptable; but if a high-impedance pin state is required on power up, the $\overline{SHZ}$ pin can be used to asynchronously disable all outputs. $\overline{RESET}$ should not be used in this case because some signals require an active clock for $\overline{RESET}$ to have an effect and the clock may not yet be active. The internal core logic becomes functional at approximately 0.8 V while the external pin IO becomes active at about 1.5 V.

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Device Support

10.2.1 Timing Parameter Symbology

Timing parameter symbols used herein were created in accordance with JEDEC standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

Table 9. Timing Parameter Meanings

Symbols	Meaning
A	Address lines (A23- A0)
ASYNCH	Asynchronous reset signals (XF0, XF1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, TCLK0, and TCLK1)
CLKX	CLKX0
CLKR	CLKR0
CONTROL	Control signals
D	Data lines (D31 to D0)
DR	DR
DX	DX
EXTCLK	EXTCLK
FS	FSX/R
FSX	FSX0
FSR	FSR0
GPI	General-purpose input
GPIO	General-purpose input/output; peripheral pin (CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, TCLK, and TCLK1)
GPO	General-purpose output
H1	H1
H3	H3
H	H1 and H3
HOLD	$\overline{\text{HOLD}}$
HOLDA	$\overline{\text{HOLDA}}$
IACK	$\overline{\text{IACK}}$
INT	$\overline{\text{INT3}}$ to $\overline{\text{INT0}}$
PAGE	$\overline{\text{PAGE0}}$ to $\overline{\text{PAGE3}}$
RDY	$\overline{\text{RDY}}$
RW	R/$\overline{\text{W}}$
RW	R/$\overline{\text{W}}$
RESET	$\overline{\text{RESET}}$
S	$\overline{\text{STRB}}$
SCK	CLKX/R
SHZ	$\overline{\text{SHZ}}$
TCLK	TCLK0, TCLK1, or TCLKx
XF	XF0, XF1, or XFx
XF0	XF0

Device Support (continued)

Table 9. Timing Parameter Meanings (continued)

Symbols	Meaning
XF1	XF1
XIN	XIN

10.2.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 DSP family devices and support tools. Each TMS320 DSP member has one of three prefixes: TMX, TMP, or TMS. TI recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully-qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

SMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

SM/SMJ Fully-qualified production device

Support tool development evolutionary flow:

TMDX Development support product that has not yet completed TI internal qualification testing.

TMDS Fully qualified development support product

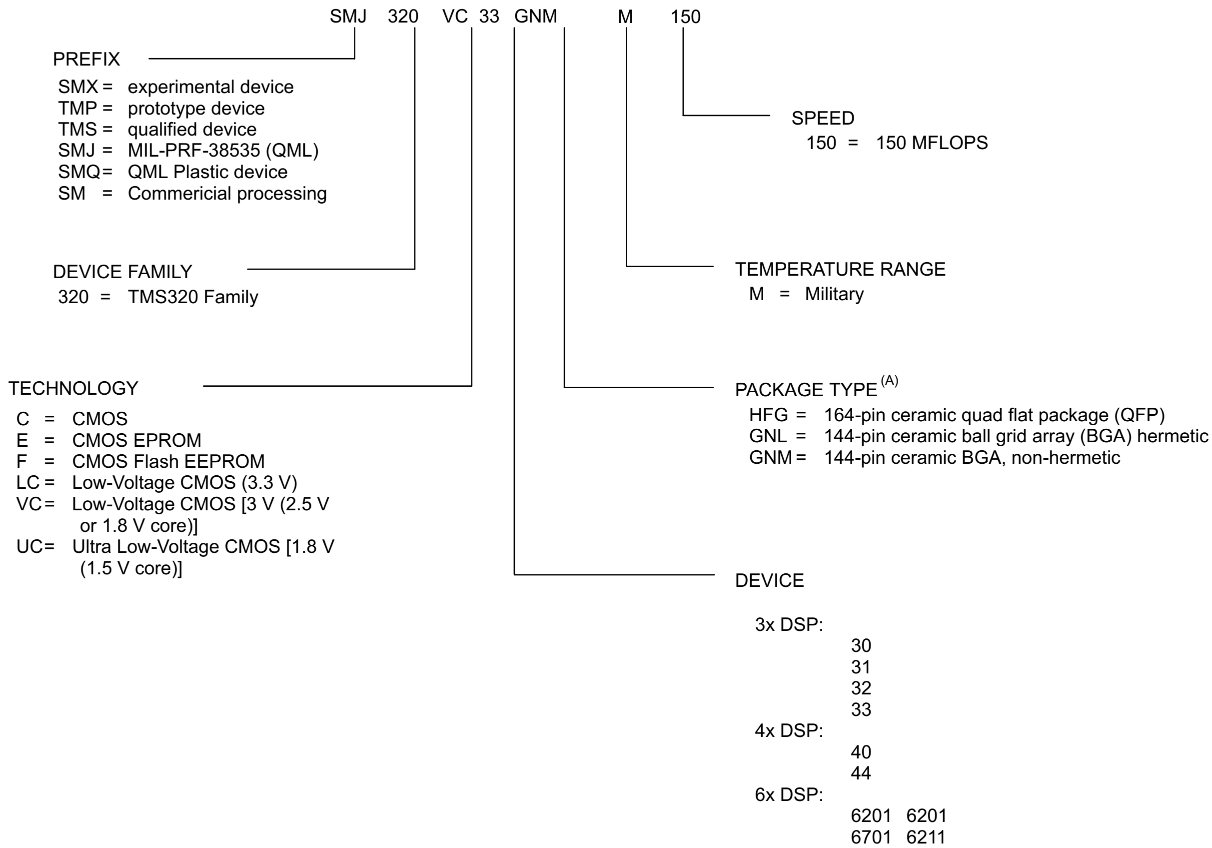
TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development support tools have been characterized fully, and the quality and reliability of the device has been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, HFG, GNM, or GNL) and temperature range (for example, M). Figure 39 provides a legend for reading the complete device name for any TMS320 DSP family member.



A. QFP = Quad flat package

LQFP = Low-profile quad flat package

BGA = Ball grid array

Figure 39. TMS320 DSP Device Nomenclature

10.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SM320VC33	Click here	Click here	Click here	Click here	Click here
SMJ320VC33	Click here	Click here	Click here	Click here	Click here

10.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 Trademarks

TImeline, SM320C3x, E2E are trademarks of Texas Instruments.
DuPont is a trademark of E. I. du Pont de Nemours and Company.
All other trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0053901QYA	ACTIVE	CFP	HFG	164	1	Non-RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	5962-0053901QY A SMJ320VC33HFGM 150	Samples
5962-0053901QYC	ACTIVE	CFP	HFG	164	1	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	5962-0053901QY C	Samples
SMJ320VC33HFGM150	ACTIVE	CFP	HFG	164	1	Non-RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	5962-0053901QY A SMJ320VC33HFGM 150	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

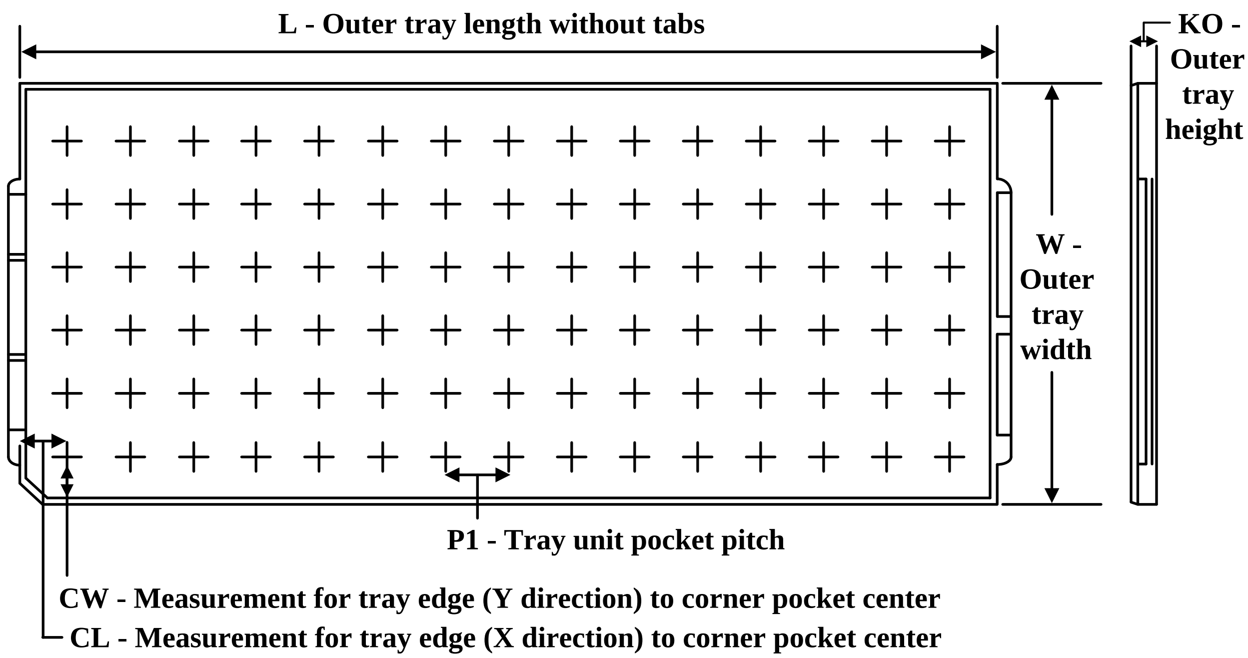
OTHER QUALIFIED VERSIONS OF SMJ320VC33 :

- Catalog : TMS320VC33

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TRAY

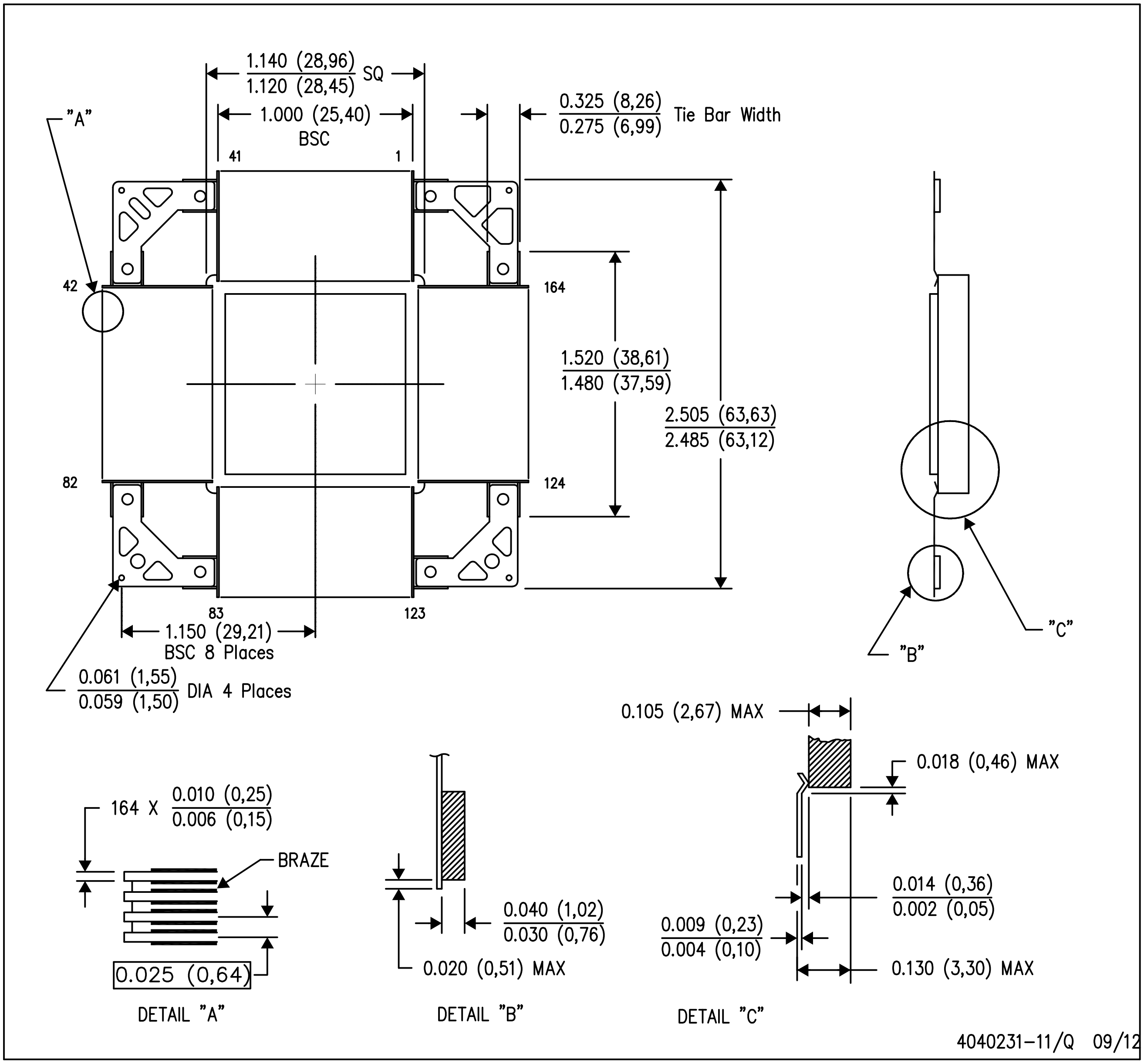


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-0053901QYA	HFG	CFP	164	1	1 x 4	75	315	135.9	12190	68	55.5	67.95
5962-0053901QYC	HFG	CFP	164	1	1 x 4	75	315	135.9	12190	68	55.5	67.95
SMJ320VC33HFGM150	HFG	CFP	164	1	1 x 4	75	315	135.9	12190	68	55.5	67.95

HFG (S-CQFP-F164) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Falls within JEDEC MO-113AA (REV D)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265