TSW3725EVM Evaluation Module

This document outlines the basic steps and functions that are required to ensure the proper operation of the TSW3725EVM evaluation module. This guide helps the user to quickly evaluate the performance of the TSW3725EVM TX, RX, and Feedback signal chain.

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1 Overview

The TSW3725EVM consists of the following components:

- TSW3725EVM board
- TSW3725 adaptor board
- USB cable

For evaluating the TX chain, the additional hardware requirements are:

- TSW3100EVM (includes 5-/6-V power supply, Ethernet cable, and Ethernet to USB adaptor)

For evaluating the RX or Feedback chain, the additional hardware requirements are:

- TSW1200EVM (includes 5-/6-V power supply and USB cable)

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2 General Description

The TSW3725EVM is a small-cell basestation development platform. It provides two real receive paths, two complex transmit paths, and a shared real feedback path.

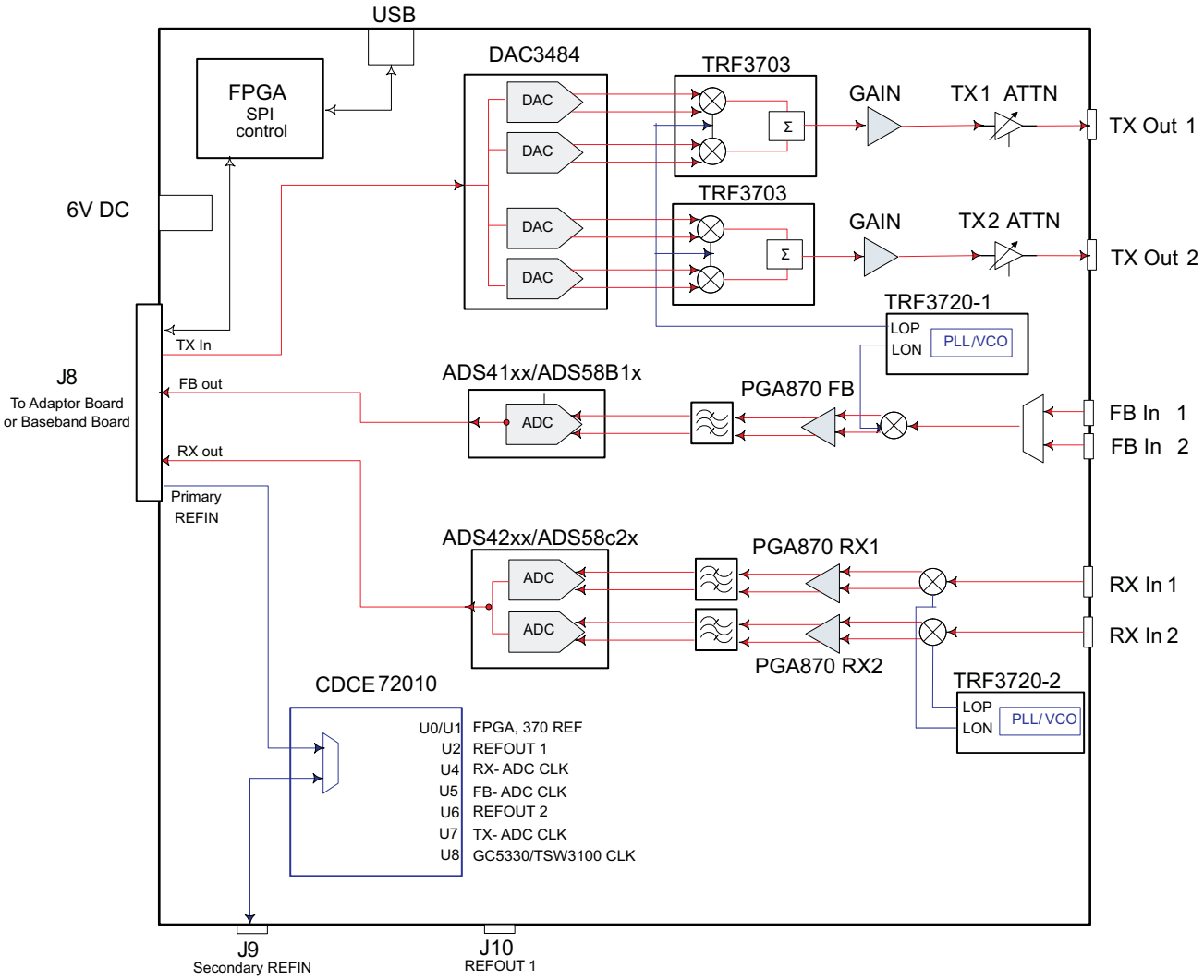

Figure 1. TSW3725EVM Block Diagram

The TSW3725 can be evaluated as a stand-alone board with the TSW3100EVM as a digital source board and the TSW1200EVM as a digital capture board. In this configuration, the TSW3725 adaptor board is required. A few of the possible configurations to evaluate this board in stand-alone are shown in Section 4.2 of this document.

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2.1 TSW3725 and TSW32725 Adaptor Board

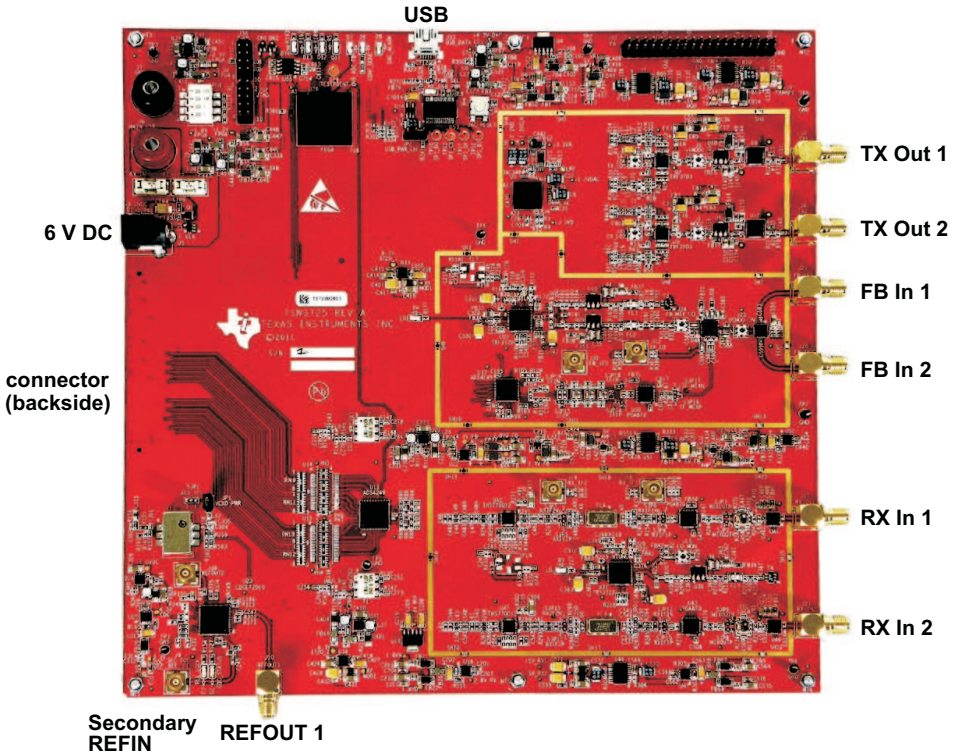

Figure 2. TSW3725EVM

Figure 2 shows the TSW3725 without RF shields over the Transmit (TX), Feedback (FB), and Receive (RX) signal chains. Shown in this figure are the locations for several connectors used to operate the TSW3725. The USB connector is used in Stand-Alone mode, which is described in following text. The J8 connector can either connect to the TSW3725 adaptor boards or the small-cell basestation platform (SCBP). The supply voltage can be connected from the 6-Vdc connector or the banana plug connectors shown in Figure 2, or it can be supplied directly form the TSW3725 adaptor or SCBP boards. The primary 30.72-MHz reference for the TSW3725 is supplied from the TSW3725 adaptor board or the SCBP. However, a connector option on the TSW3725 for a secondary reference is shown in Figure 2.

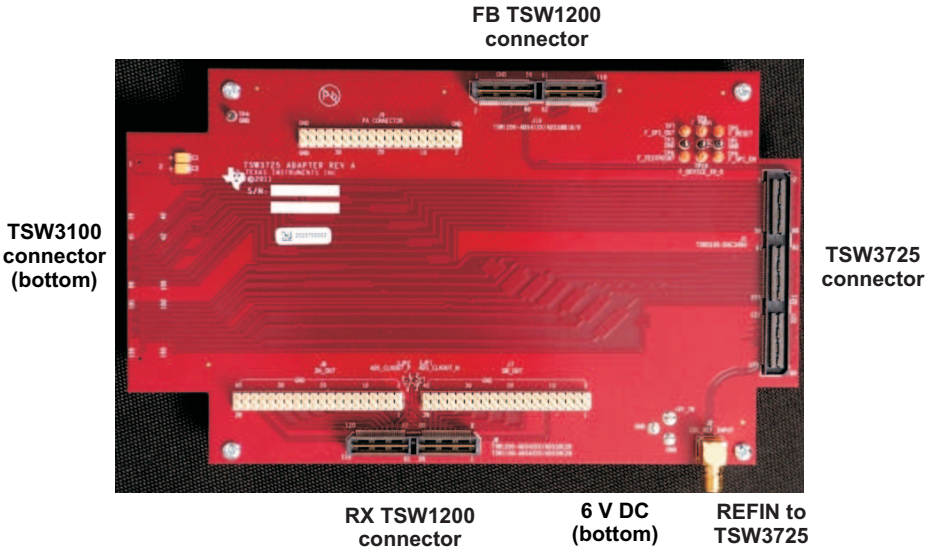

Figure 3. TSW3725 Rev-A Adaptor

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Figure 3 shows the TSW3725 adaptor board. This board is used in the stand-alone configuration to connect the TSW3725 to the TSW3100 digital source board for TX evaluation and the TSW1200 digital capture board for RX and FB evaluation. This board was also designed to work with the TSW1400, which is both a digital source and a capture board. At the time of publication of this document, the TSW1400 has not been released to market.

2.2 TSW3725 – Stand-Alone Configuration

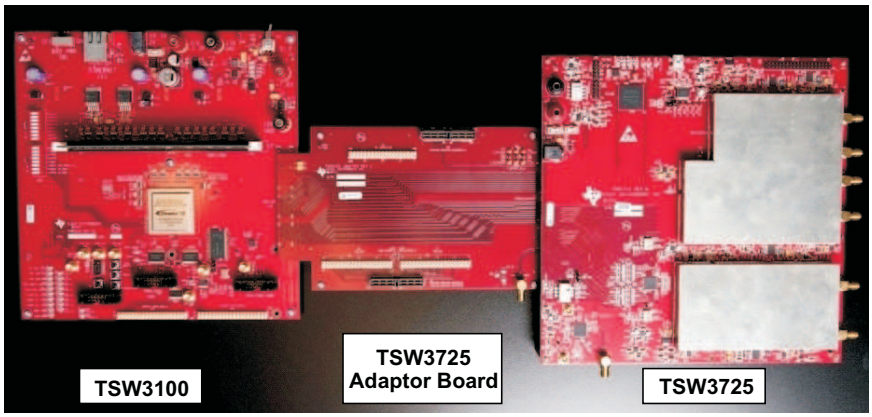

Figure 4. TSW3725 in Stand-Alone Configuration (TSW1200 Not Shown)

Figure 4 provides an example of the stand-alone configuration. In this figure, the TSW3725 adaptor board connects the TSW3725 to the TSW3100. In this mode, the 6-V power and a 30.72-MHz reference must be supplied to the TSW3725 adaptor board. Also in this mode, the TSW3725 requires a USB connection to configure the SPI interfaces of the TSW3725 components

3 Software Installation

For the TSW3725 stand-alone configuration, users must install the TSW3725EVM software, the TSW1200EVM software, and the TSW3100EVM software. The TSW1200EVM and TSW3100EVM software installation procedures are discussed in their respective user's guides. This section only discusses how to install the TSW3725EVM software.

3.1 Downloading TSW3725 Software and MATLAB™ MCR 7.13 (MATLAB™ Compiler Runtime)

1. Unzip file TSW3725 GUI and MCR INSTALLER.zip.
2. TSW3725 software is located in directory: TSW3725 GUI and MCR INSTALLER\TSW3725_GUI_EXE.
3. MATLAB™ 7.13 MCR installer is located in directory: TSW3725 GUI and MCR INSTALLER\2010a_MCR.

3.2 Installing FT245R Drivers

The TSW3725 uses the FT245R chip as the USB interface. If the FT245R D2XX drivers are not installed, the TSW3725 GUI will have the following error if the *Program All* button is selected.

- **??? Error using → loadlibrary at 480**
- **There was an error loading the library "pathname\TSW3725_GUI_EXE\TSW3725_GUI_mcr\DLL_drivers\tsw6011_usb_spi.dll"**
- **The specified module could not be found**

In most cases, installing these drivers occurs automatically when the TSW3725 USB cable is connected to a computer and a TSW3725 that have been powered up. The latest version of the D2XX driver can also be found on the FTDI chip Web site (http://www.ftdichip.com/Drivers/D2XX.htm). From here, users can download the files and executables required.

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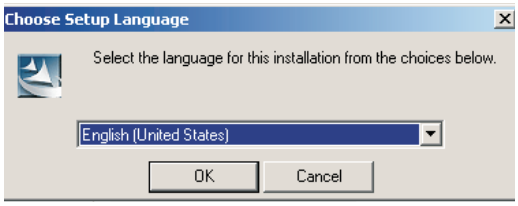
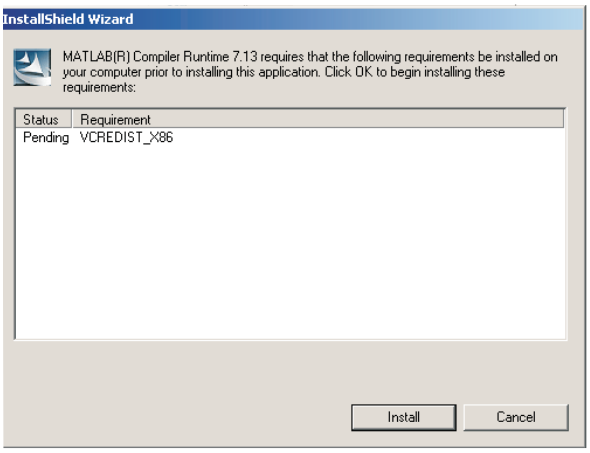
3.3 Installing MATLAB™ MCR 7.13 (MATLAB™ Compiler Runtime)

1. Enter Directory: TSW3725 GUI and MCR INSTALLER\2010a_MCR.
2. Select the file: MCRInstaller.exe. This starts the installation process.
3. Select desired language, and press *OK*.



4. When the following window appears, press *Install*.



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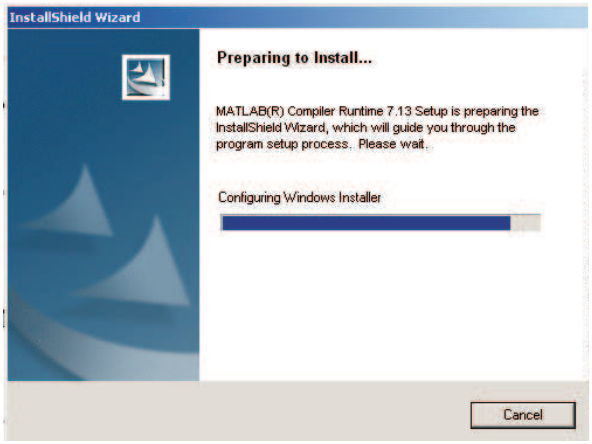
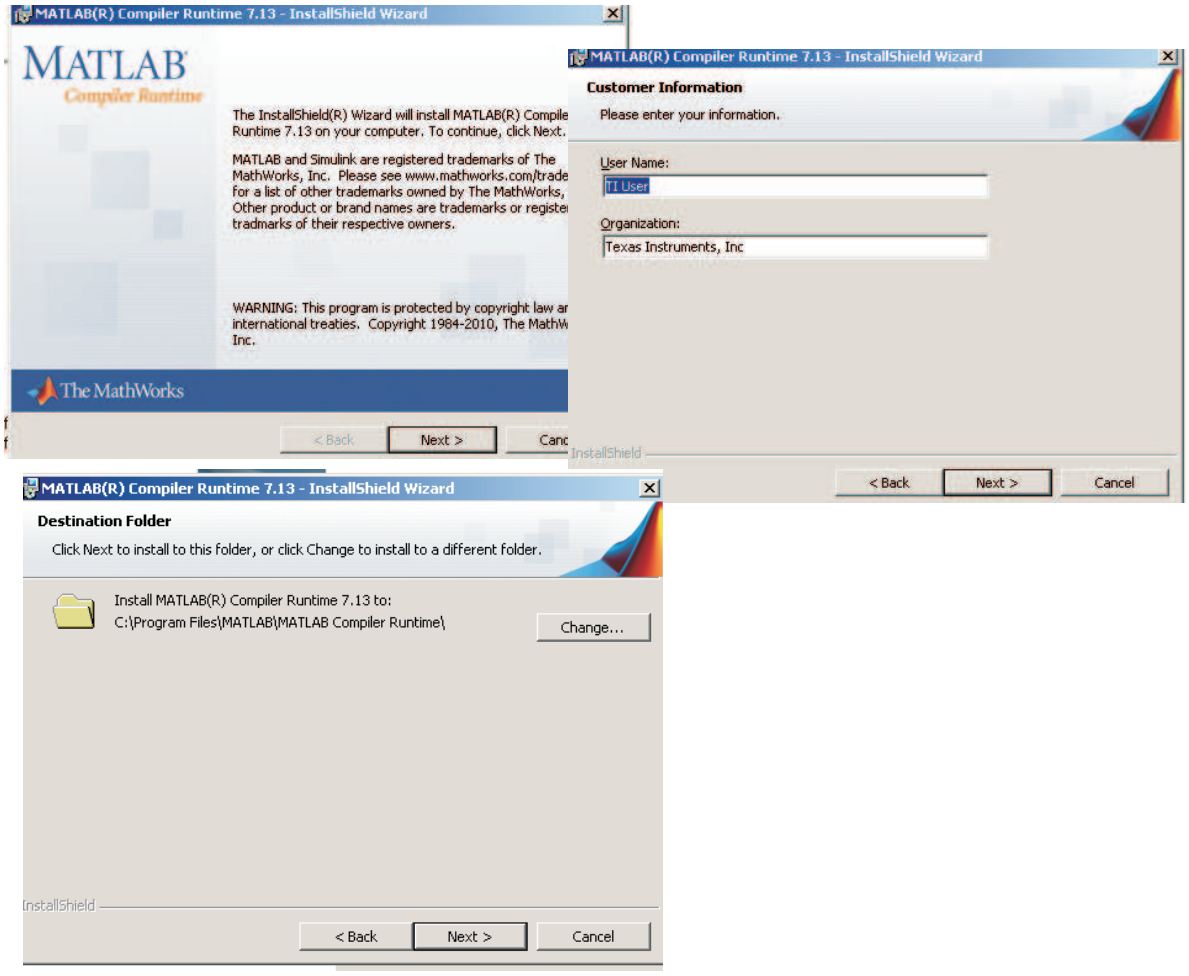
5. The following box appears while installing



6. Select *Next* in the following three windows that follow.



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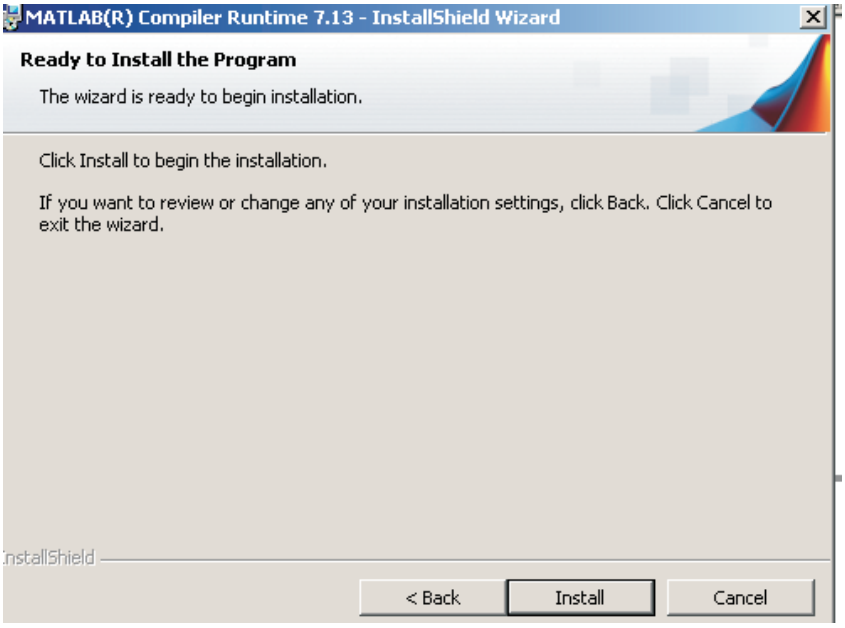
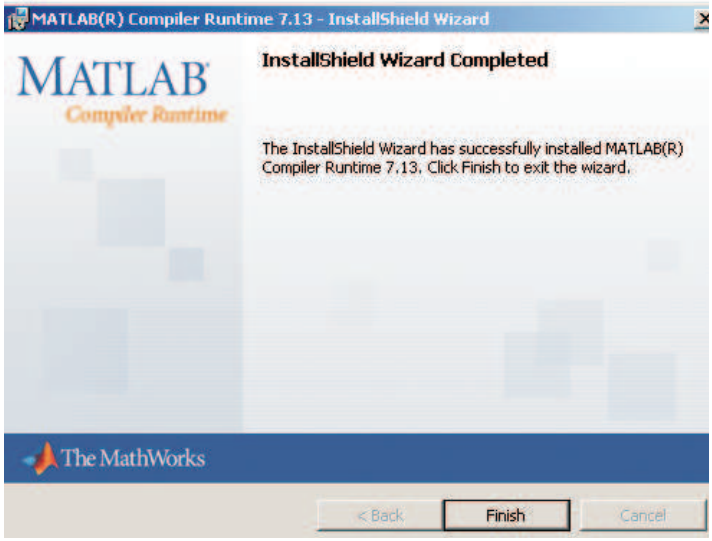
7. Select *Install* in the following box; a new box appears that says installation will take several minutes.



8. Select *Finish*.



9. Installation is complete.

4 Hardware Overview

The TSW3725 hardware can be used in two modes:

1. SCBP mode: Small-cell basestation platform
2. Stand-Alone

Section 4.1 discusses how to convert the TSW3725 from SCBP mode to Stand-Alone mode.
Section 4.2 discusses the hardware connections required in Stand-Alone mode.
Section 4.3 discusses the power-up sequence required in Stand-Alone mode.

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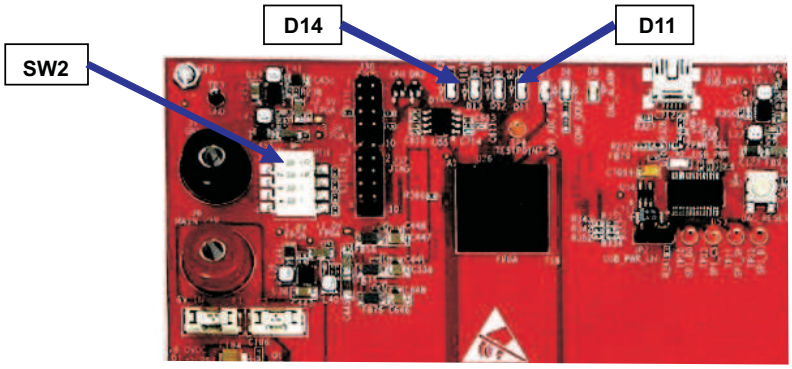
4.1 Converting From SCBP Mode to Stand-Alone Mode

Only one board modification is required to switch between SCBP mode and Stand-Alone mode. The switch 1 on SW2 determines if the TSW3725 is in SCBP or Stand-Alone mode.

1. **Stand-Alone mode:**
   (a) Push switch 1 on SW2 to the right, with respect to the following picture.
   (b) If board is powered, then LED D11 starts blinking and LED D14 should be off.
2. **SCBP mode:**
   (a) Push switch 1 on SW2 to the left, with respect to the following picture.
   (b) If board is powered, then LED D14 starts blinking and LED D11 should be off.



The TSW3725 does have two SPI settings updates when switching between modes. These are important to understand and perform, if the user is creating configuration files in Stand-Alone mode, and using this configuration file to program the SCBP in SCBP mode. These SPI settings are listed in the following table under default settings.

Stand-Alone Mode		
TSW3725 GUI	**Default Setting**	**Comments**
GC5330/TSW3100 CLK pulldown menu	Set to /8	TSW3100 clock rate determined by DAC3484 interpolation rate and DDR clock TSW3725 default DAC3484 interpolation setting = 4x; set clock rate = 1/(interpolation setting *2); the *2 is due to DDR clock
DAC3484 config 2, addr 02, bit 16 (MSB)	Set to 1	TSW3100 requires word wide mode
SCBP Mode		
TSW3725 GUI	**Default Setting**	**Comments**
GC5330/TSW3100 CLK pulldown menu	Set to /2	GC5330 requires data clock equal to half the DAC data rate
DAC3484 config 2, addr 02, bit 16 (MSB)	Set to 0	GC5330 on SCBP requires byte-wide mode

4.2 Hardware Setup and Connections – TSW3725 Stand Alone Configuration

The purpose of this section is to assist the user to set up the TSW3725 hardware quickly, using the TSW3100 digital source board and TSW1200 digital capture board. This document assumes that the user has familiarity with the TSW3100 and TSW1200 hardware and software, or that the user has access to the TSW3100 and TSW1200 EVM user's guides for TSW3100- or TSW1200-specific issues. Both user's guides are available on the TI Web site (www.ti.com).

When using the TSW3100 and TSW1200, the TSW3725 can be configured to run in almost any variety of measurement configurations as shown in the following illustration. To capture the feedback path and the RX path simultaneously with multiple TSW1200s, a second computer is required.

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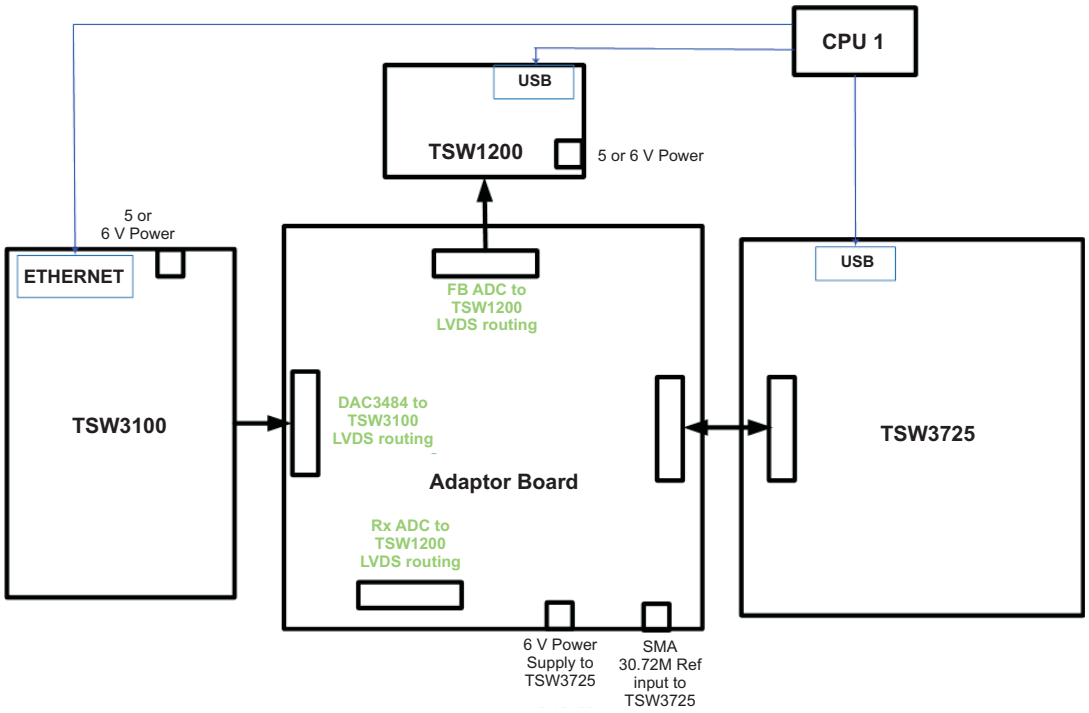

Figure 5. TX and FB Configuration

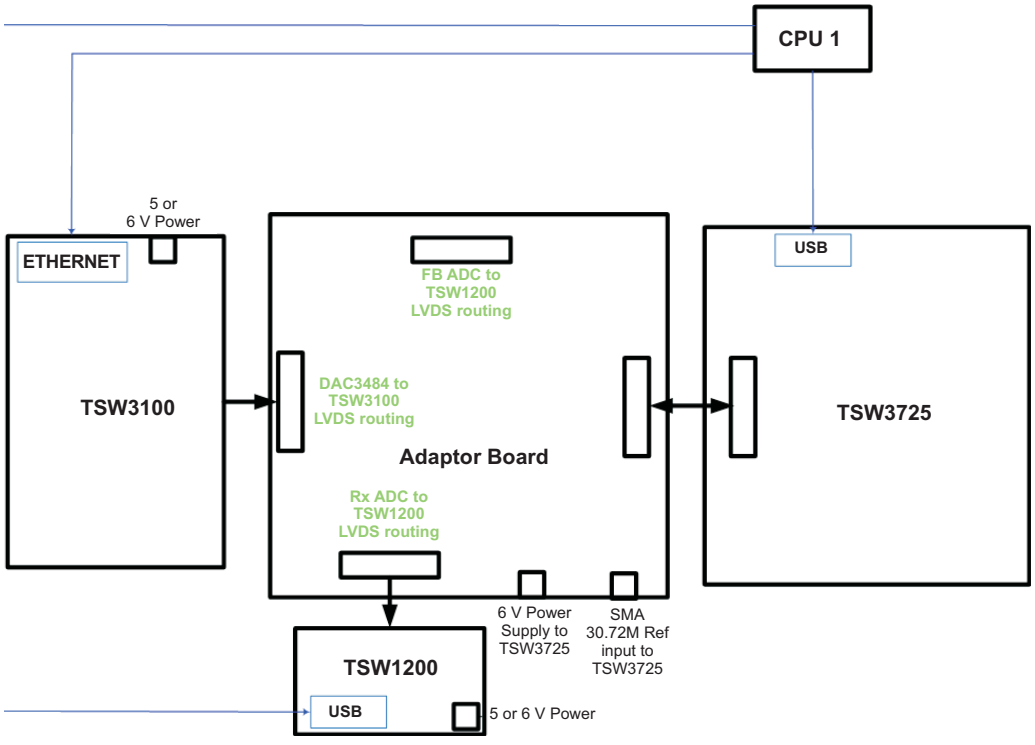

Figure 6. 2 TX and 2 RX Configuration

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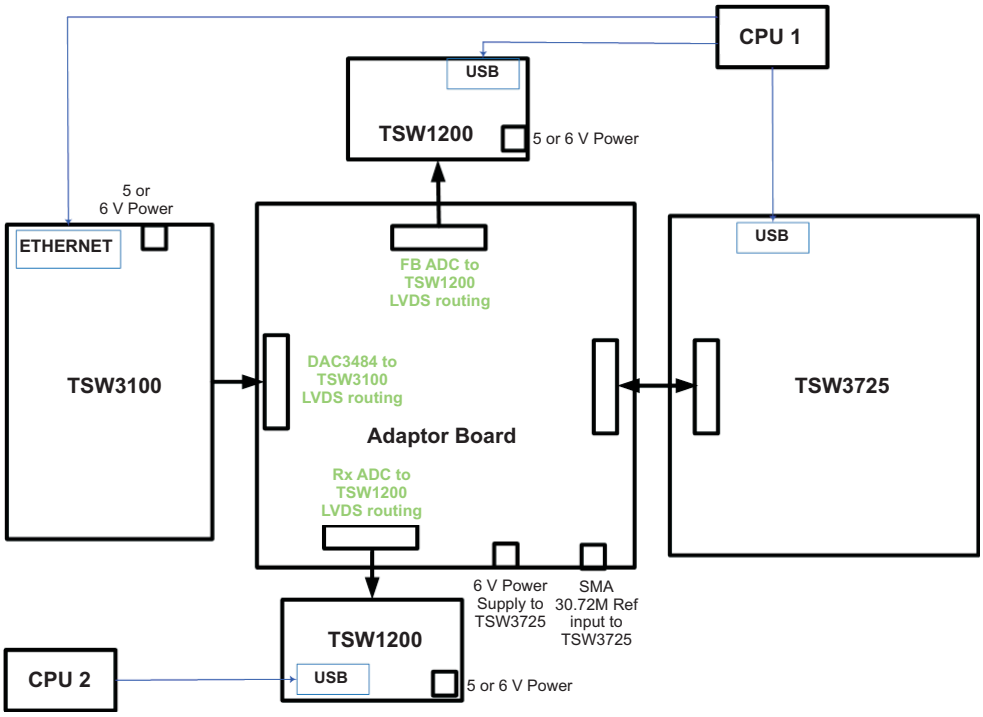

Figure 7. Two TX, FB, and Two RX Configuration (Requires Two Computers)

4.3 Power-Up Sequence

This section provides the order in which to connect and power up the TSW3725, TSW3100, and TSW1200 hardware. Depending on the user's desired configuration, some of the following optional sections can be disregarded.

Section A: **Required:**– this section is used for all TSW3725 Stand-Alone measurements.
Section B: **Optional:**– required to evaluate the TX Path.
Section C: **Optional:**– required to evaluate the Feedback Path.
Section D: **Optional:**– required to evaluate the RX Path.

Section A. Required Connection:
This section describes how to connect the TSW3725 to the TSW3725 Adaptor board.

1. Connect TSW3725 connector J8 to TSW3725 Adaptor board connector J1.
2. Connect TSW3725 to a 6-V/4-A supply via any of the three following options.
   (a) Option 1: TSW3725 Adaptor board connector J3 (+6V_IN)
   (b) Option 2: TSW3725 connector J5
   (c) Option 3: TSW3725 banana plugs J7 (GND) and J6 (6 V)
3. Verify the following LEDs are lit on the TSW3725.
   (a) D1 6 Vdc: green D2: CDC_STATUS: green
   (b) D6: FPGA CONFIG: green
   (c) D10: USB POWER: blue
   (d) D11: green (blinking), if D14 is blinking instead, then refer to Section 4.1.
4. Connect a 30.72M reference to TSW3725 Adaptor board connector J2.
   (a) Refin Input amplitude can range from 0.2 Vpp - 3.3 Vpp

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Section B. Optional Connection: TX Path Digital Source

This section describes how to connect the TSW3100 to the TSW3725 Adaptor board to evaluate the TSW3725 TX paths. A detailed explanation for the TSW3100 setup is described in the TSW3100EVM guide, which is available on the TI Web site (www.ti.com)

1. Connect TSW3725 Adaptor board connector J4 to TSW3100 connector J74.
2. Connect TSW3100 connector J9 (5V_IN) to a 5-V or 6-V supply.
3. Set TSW3100 SW1 (BRD_PWR) to ON.
4. Verify the following LEDs are illuminated on the TSW3100.
   (a) D3: green
   (b) D4: green
   (c) D5: green
   (d) D6: green
   (e) D11 FPGA CONFIG: orange
   (f) D13 PAT GEN IDLE: orange
   (g) D18 LVDS PLL LOCK: orange
   (h) D19 DDR2 PLL LOCK: orange
   (i) D20 NIOS PLL LOCK: orange
   (j) D25 STATUS 1: orange
   (k) D26 STATUS2: orange
5. Connect TSW3100 J13 Ethernet connector to the Ethernet cable; connect Ethernet cable to computer directly or through an Ethernet/USB adaptor.
6. Verify orange and green LEDs near J13 are illuminated.
7. See *TSW3100 High Speed Digital Pattern Generator* user's guide (SLLU101) for a detailed explanation on how to set the TSW3100 IP address

Section C. Optional Connection: Feedback Path Capture

This section describes how to connect the TSW1200 to the TSW3725 Adaptor board to evaluate the TSW3725s Feedback path. See *TSW1200EVM: High-Speed LVDS Deserializer and Analysis System* user's guide (SLAU212) for a detailed explanation for the TSW1200 setup.

1. Connect TSW3725 Adaptor board connector J10 to TSW1200 connector J9.
2. Connect 5-V supply to TSW1200 banana plugs J14 (GND) and J15 (+5 V).
3. Verify that the following LEDs are illuminated on the TSW3100.
   (a) D1: blue
   (b) D2: blue (blinks)
   (c) D4: blue (blinks)
   (d) D7: blue
   (e) D16: green
4. Connect TSW1200 USB port J8 to USB cable; connect USB cable to computer.

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Section D. Optional Connection: RX Path Capture

This section describes how to connect the TSW1200 to the TSW3725 Adaptor board to evaluate the TSW3725s RX paths. See *TSW1200EVM: High-Speed LVDS Deserializer and Analysis System* user's guide (SLAU212) for a detailed explanation for the TSW1200 setup.

1. Connect TSW3725 Adaptor board connector J6 to TSW1200 connector J9.
2. Connect 5-V supply to TSW1200 banana plugs J14 (GND) and J15 (+5 V).
3. Verify that the following LEDs are illuminated on the TSW3100.
   (a) D1: blue
   (b) D2: blue (blinks)
   (c) D4: blue (blinks)
   (d) D7: blue
   (e) D16: green
4. Connect TSW1200 USB port J8 to USB cable; connect USB cable to computer.

4.4 Power-Down Sequence

1. If used, turn off TSW3100 power using SW1.
2. Disconnect power to TSW3725EVM.
3. If used, disconnect power to the TSW1200EVM.

5 Quick Setup

This section assumes that the hardware setup was completed in Section 4 and that the hardware is powered up. The goal of this section is to provide the user a quick setup procedure to start the software and evaluate a simple single tone signal by using the TSW1200 and/or the TSW3100. This allows users to become familiar with all the software and hardware components required to use the TSW3725 hardware.

Section 6 discusses more complex waveforms and the related setup. Section 7 discusses the TSW3725 GUI in detail.

5.1 Starting the TSW3725 GUI Software

1. Ensure that TSW3725 hardware connections are completed as discussed in Section 4.
2. Start TSW3725 GUI by selecting the file TSW3725_GUI.EXE. This file resides in the directory TSW3725 GUI and MCR INSTALLER\TSW3725_GUI_EXE..

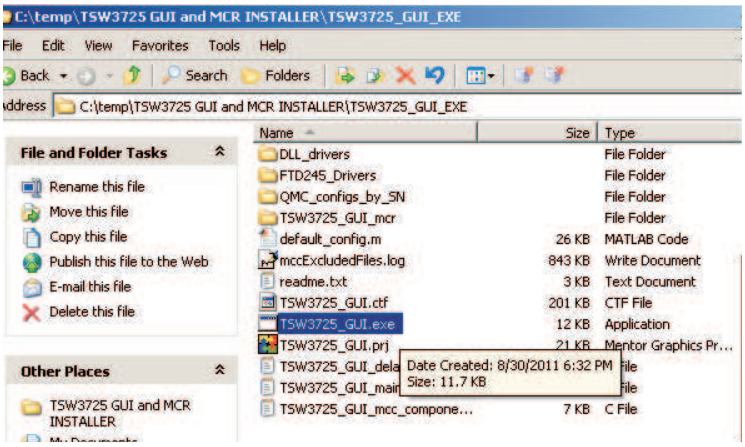

Figure 8. TSW3725_GUI.exe

3. The GUI appears as shown in Figure 9

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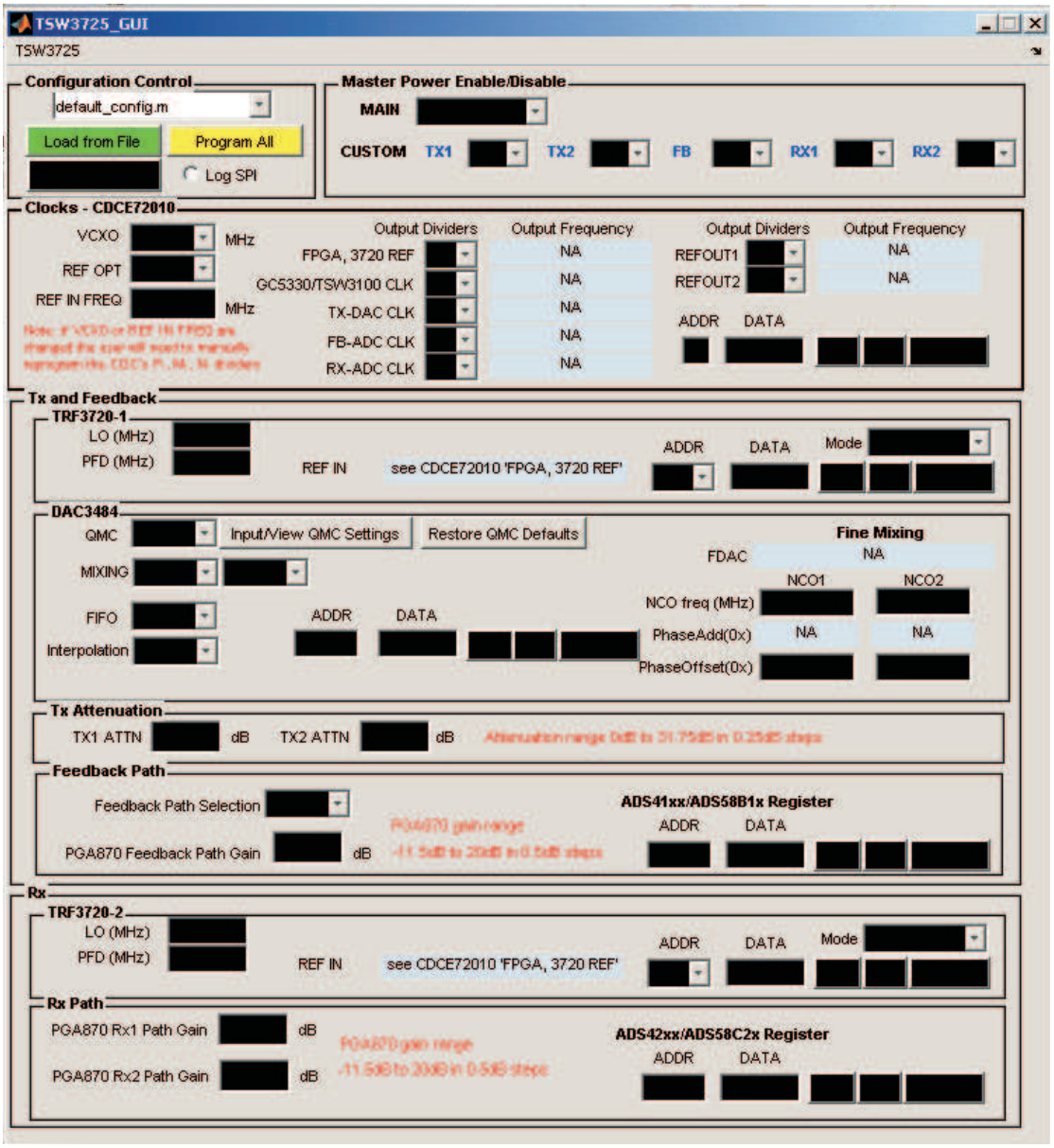

Figure 9. TSW3725 GUI at Start-Up

5.2 Load the Default TSW3725 Configuration

1. Select the yellow *Program All* button to program the recommended default settings to the TSW3725. Default settings are set up for Band 1 LTE and Band 1 WCDMA.

   (a) After the yellow *Program All* button is selected, it turns white and makes text updates as to which section of the board is being programmed.

   (b) This procedure takes approximately 25 seconds to complete.

   NOTE: If the following error appears in the cmd tool window that appears with the TSW3725 GUI, then see Section 3 about installing the FT245 drivers.

   ??? Error using → loadlibrary at 480
   There was an error loading the library
   "pathname\TSW3725_GUI_EXE\TSW3725_GUI_mcr\DLL_drivers\tsw6011_usb_spi.dll"
   The specified module could not be found

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2. When programming is complete, the TSW3725 GUI appears as Figure 10 shows.

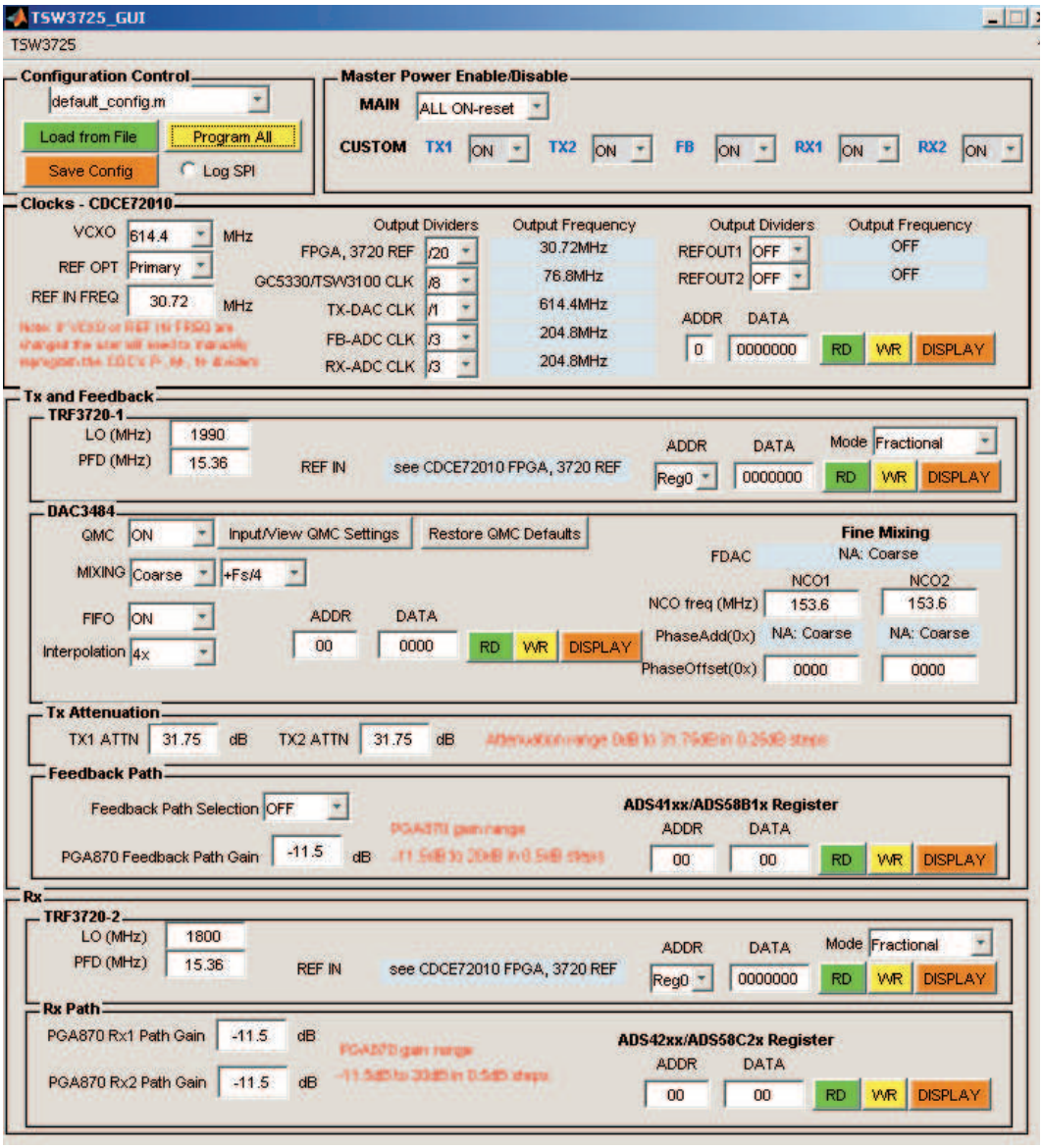

Figure 10. TSW3725 GUI After Load is Complete

3. When programming is complete, verify that the following LEDs on the TSW3725 HW are illuminated. If they are, then the TSW3725 was programmed correctly. If they are not, then start over at step 1.
   (a) D3 POLLOCK: green (confirms CDC chip is locked)
   (b) D4 LD: green (confirms TRF3720 for TX and Feedback paths is locked)
   (c) D5 LD: green (confirms TRF3720 for RX path is locked. Note: on Rev A hardware, this LED is under the RX RF Shield; this LED was moved outside of the RX RF Shield on Rev B hardware.)

5.3 TX Path: TSW3100 Software Setup – Single Tone Example

For a detailed explanation for the TSW3100 setup, see *TSW3100 High Speed Digital Pattern Generator* user's guide (SLLU101).

1. From the TI Web site, download and install the TSW3100EVM GUI v2.7 or later version. Earlier versions of the TSW3100EVM GUI software do not support the DAC3484 input data format that is required to run the TSW3725.

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2. Load the TSW3100_MultitonPattern_v2p7 GUI, and program the following settings to run a single tone at 5 MHz with the default settings of the TSW3725 GUI.
   (a) Signal Characteristics
      (i) Sample Rate: 153.6
      (ii) Back off: 0.99
      (iii) Resolution: 16
      (iv) Vector size: 2^15
   (b) Signal Type
      (i) Complex
   (c) Tone Groups
      (i) Select *Group 1.*
      (ii) Tone BW = 1
      (iii) # = 1
      (iv) Tone Center = 5
      (v) Gain(dB) = 0
   (d) TSW3100 Control
      (i) Select *master.*
      (ii) Select *16b QDAC.*
      (iii) Select *Two's Comp*.
      (iv) Select *Load and Run*.
      (v) Select *16b MSB Justify.*
      (vi) Ensure IP setting is correct (see SLLU101).
3. The TSW3100 appears as shown in Figure 11.

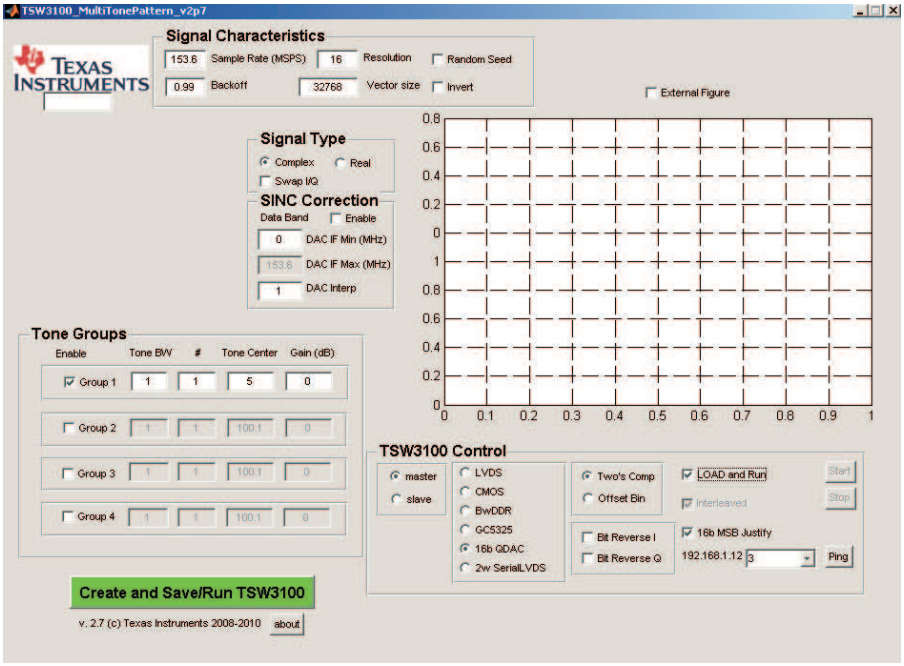

Figure 11. TSW3100 GUI

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4. Click on the green button *Create and Save/Run TSW3100*, when the TSW3100 is finished. The TSW3100 appears as shown in Figure 12.

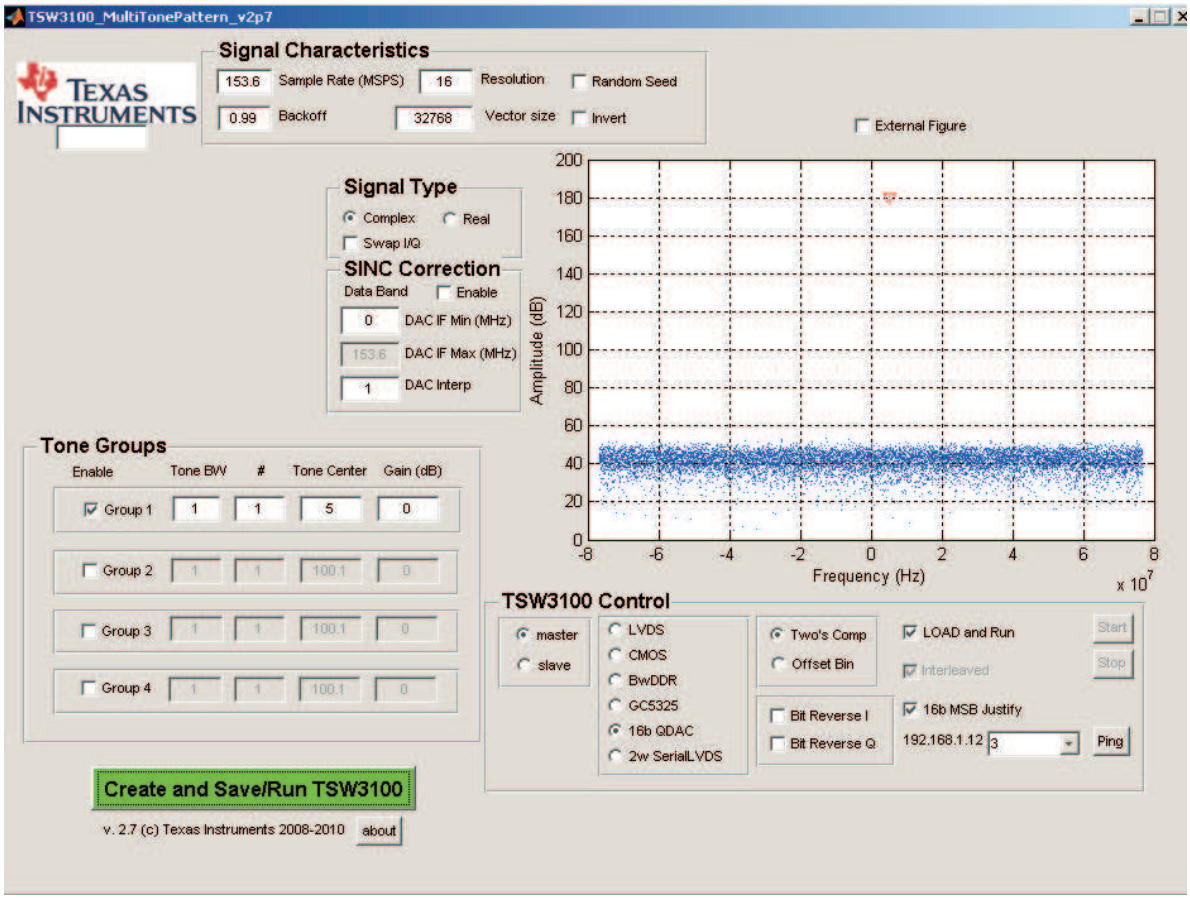

Figure 12. TSW3100GUI After Waveform Created

5. Verify that the following TSW3100 LEDs are illuminated. If these LEDs are not, verify that the TSW3725 is connected properly and its default settings are loaded,
   (a) D14: PAT GEN CLK
   (b) D15: PAT GEN RUN
6. If TSW3100 LED D16: FIFO EMPTY ERROR is illuminated, then the TSW3100 did not load correctly and step 4 needs to be repeated. If this continues, then power cycle the TSW3100 board before repeating step 4.
7. Ensure that the TSW3725 hardware is programmed with the *default_config.m* file.
8. The TSW3725 TX1 or TX2 output with these settings have roughly a -25-dBm signal at 2148.6. This can be calculated by the following equation.
   (a) LO frequency = 1990 MHz
   (b) Coarse mixer = Fs/4 = 614.4/4 = 153.6 Hz
   (c) Tone center in TSW3100 GUI = 5 MHz
   (d) Equation = LO frequency + coarse mixer + tone center = 1990 MHz + 153.6 MHz + 5 MHz = 2148.6 MHz

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5.4 Feedback Path: TSW1200 Software Setup – Single Tone Example

A detailed explanation for the TSW1200 setup is described in the user's guide SLAU212.

1. From the TI Web site, download and install the TSW1200GUI-SW v2.5 or later version.
2. Load TSW1200_v2p5 or later. The TSW1200 GUI appears as shown in Figure 13.

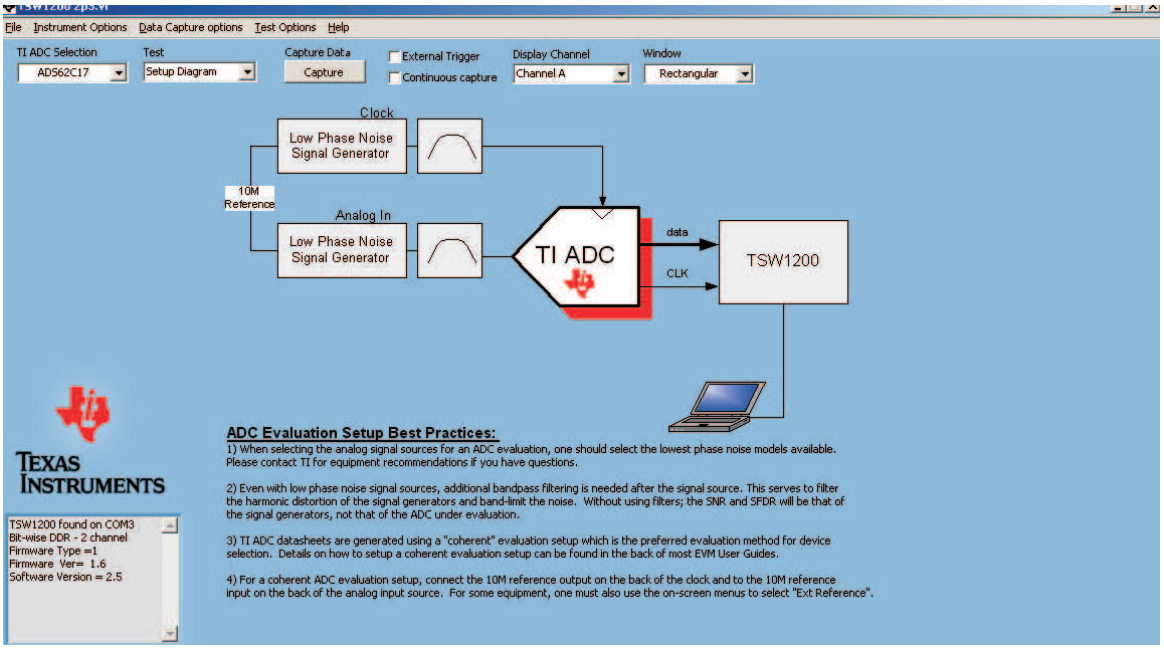

Figure 13. TSW1200 GUI

3. The text box in the bottom left states *TSW1200 found on COM3*. If the text box does not state this, then type CTRL+SHIFT+I. If that des not work, then power cycle the TSW1200 and type CTRL+SHIFT+I.
4. From the *TI ADC Selection* pulldown menu, select the Feedback ADC family that is installed on the TSW3725. The default ADC in the TSW3725 bill of materials is the ADS4149. In this case, select *ADS414x*.

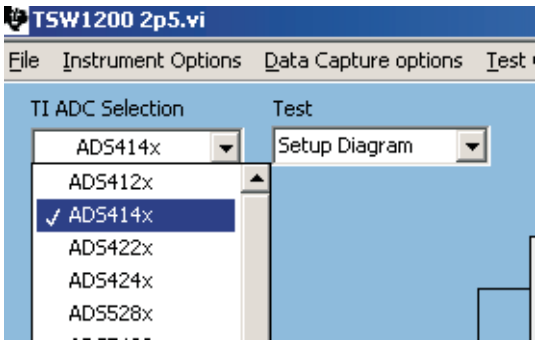

Figure 14. TSW1200 GUI – ADC Selection

5. Ensure that the TSW1200 data capture is in *Two's Complement Mode*. From the TSW1200 main toolbar, select *Data Capture options → Capture Options → Two's Complement Mode*. This matches the ADS4149 default SPI setting on the TSW3725 board.

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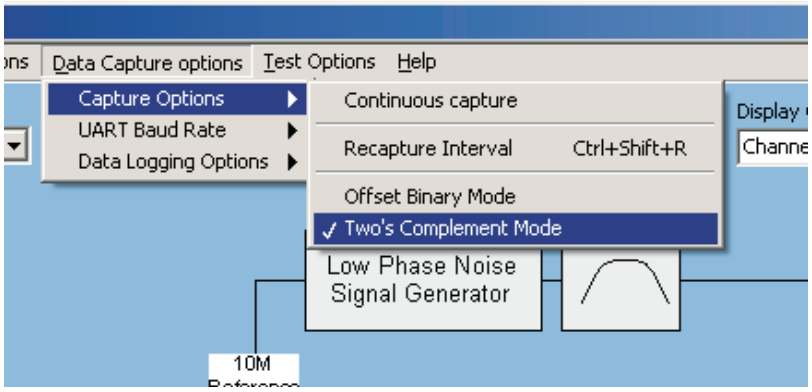

Figure 15. TSW1200 GUI – Capture Option

6. From the TSW1200 *Test* pulldown menu, select *Single Tone FFT.*

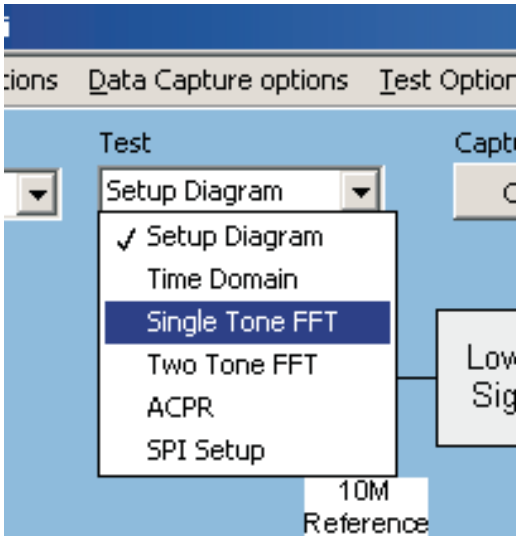

Figure 16. TSW1200 GUI – Test Selection

7. Ensure that the TSW3725 hardware is programmed with the *default_config.m* file.
8. Program the TSW1200 GUI – Single Tone Test Setup as follows
   (a) ADC Sample Rate (Fs) = 204.8M
   (b) ADC Input Frequency (Fc) = 153.6M
   (c) FFT Record Length (Ns) = 16384
   (d) Select the *Auto Calculation of Coherent Input Frequency* check box
9. The GUI now appears as shown in Figure 17.

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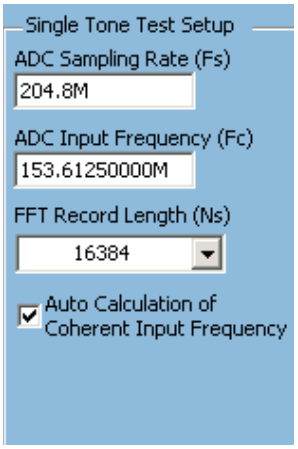
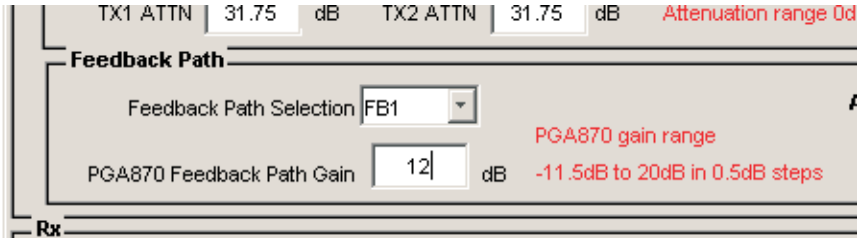


Figure 17. TSW1200 GUI – Test Setup Frequencies

10. Apply a +5-dBm, 1836.3875-MHz tone to the TSW3725 FB_IN1 J27 connector (Feedback Path 1). This frequency can be calculated from the following equation.
    (a) LO frequency = 1990 MHz
    (b) ADC input frequency = 153.6125 Hz
    (c) Equation = LO frequency – ADC input frequency = 1990M-153.6 MHz = 1836.3875 MHz
11. This signal can come from an external source or the TSW3725 TX chain.
12. From the TSW3725 GUI Feedback Path Selection pulldown menu, select *FB1* to select the Feedback Path 1.
13. From the TSW3725 GUI PGA870 Feedback Path, set Gain to 12dB



14. From the TSW1200 GUI click on the Capture button and view the results

5.5 RX Path: TSW1200 Software Setup – Single Tone Example

A detailed explanation for the TSW1200 setup is described in the TSW1200 EVM guide, which is available on the TI website (www.ti.com)

1. From the TI website download and install the TSW1200GUI-SW v2.5 or later version.
2. Load TSW1200_v2p5 or later. The TSW1200 GUI appear as shown in Figure 18

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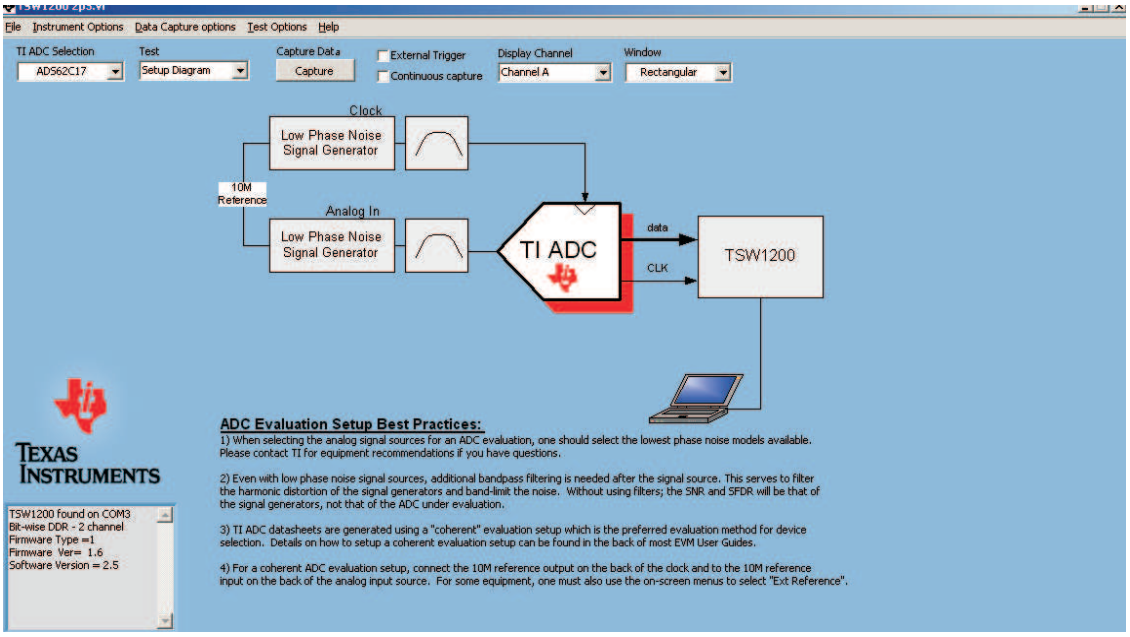

Figure 18. TSW1200 GUI

3. The text box in the bottom left states *TSW1200 found on COM3*. If the text box does not state this, then type CTRL+SHIFT+I. If that does not work, then power cycle the TSW1200, and type CTRL+SHIFT+I.
4. From the *TI ADC Selection* pulldown menu, select the Feedback ADC family that is installed on the TSW3725. The default ADC in the TSW3725 BILL OF MATERIALS is the ADS4249. In this case, select *ADS424x.*

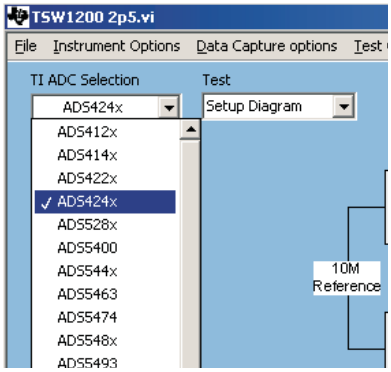

Figure 19. TSW1200 GUI – ADC Selection

5. Ensure that the TSW1200 data capture is in *Two's Complement Mode*. From the TSW1200 main toolbar, select *Data Capture options → Capture Options → Two's Complement Mode*. This will match the ADS4249 default SPI setting on the TSW3725 board.

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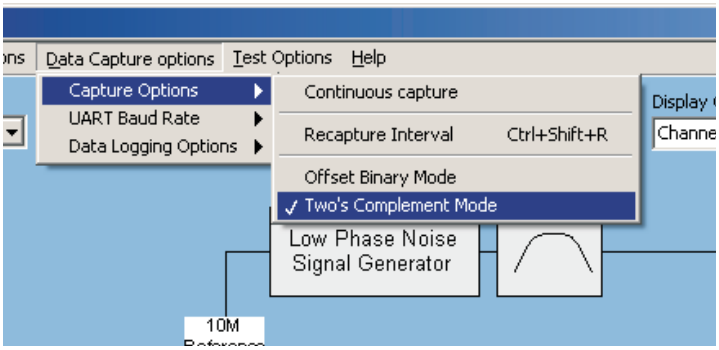

Figure 20. TSW1200 – Capture Option

6. From the TSW1200 *Test* pulldown menu, select *Single Tone FFT*.

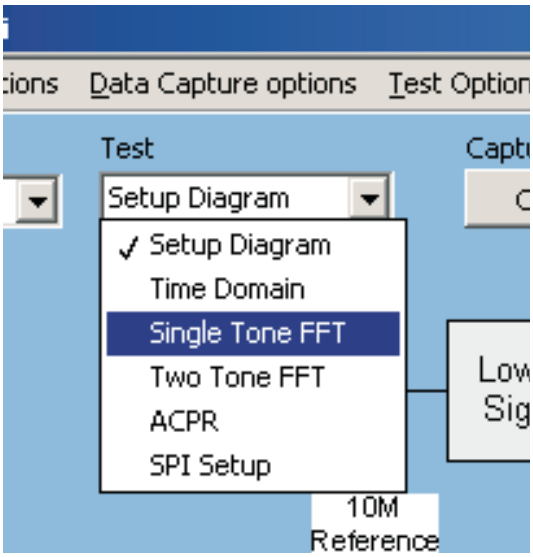

Figure 21. TSW1200 – Test Selection

7. Ensure that the TSW3725 hardware is programmed with the *default_config.m* file
8. Program the TSW1200 GUI – Single Tone Test Setup as follows.
   (a) ADC Sampling rate (Fs) = 204.8M
   (b) ADC Input Frequency (Fc) = 140M
   (c) FFT Record Length (Ns) = 16384
   (d) Select the *Auto Calculation of Coherent Input Frequency* check box
9. The GUI now appear as follows.

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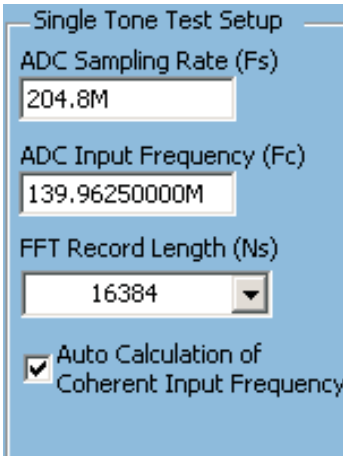

Figure 22. TSW1200 GUI – Test Setup Frequencies

10. From the TSW1200 GUI *Display Channel* pulldown menu, determine if Channel A or Channel B is going to be captured.

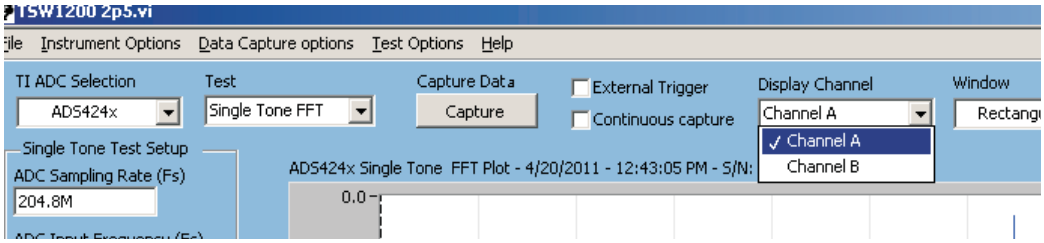

Figure 23. TSW1200 GUI – ADC Channel Selection

11. For a Channel A capture: apply a +5-dBm, 1660.0375-MHz tone to the TSW3725 RX_IN1 J17 connector. For a Channel B capture, apply this signal to the RXIN2 J21 connector. This frequency can be calculated from the following equation.
    (a) LO frequency = 1800 MHz
    (b) ADC input frequency = 139.9625 Hz
    (c) Equation = LO frequency - ADC input frequency = 1800 MHz - 139.9625 MHz = 1660.0375 MHz
    This signal can come from an external source or the TSW3725 TX chain.
12. For a Channel A capture, program the TSW3725 GUI's PGA870 RX1 Path Gain to –3 dB. For a Channel B capture, program the TSW3725 GUI's PGA870 RX2 Path Gain to –3 dB.

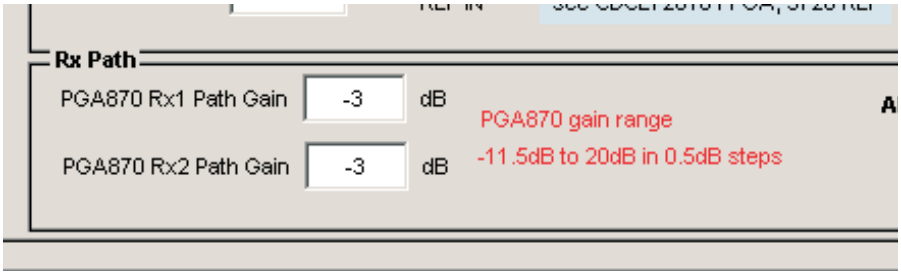

Figure 24. TSW3725 GUI – RX Path Gain

13. From the TSW1200 GUI, click on the Capture button and view the results

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6 LTE Demonstration

A detailed explanation for the TSW3100 setup is described in the TSW3100EVM guide (SLLU101).

1. From the TI Web site, download and install the TSW3100EVM GUI v2.7 or later version. Earlier versions of the TSW3100EVM GUI software do not support the DAC3484 input data format that is required to run the TSW3725.
2. Enter the *application* folder in the TSW3100 download. Select the file TSW3100_LTE_v2p7.exe to open the TSW3100 LTE GUI. Program the following settings to run a 5-MHz, single-carrier signal using the TM3.1 signal type.
   (a) Properties
      (i) Resolution: 16
      (ii) Back off(dB): 0.1
      (iii) Complex: check 6
      (iv) Freq (MHz): 153.
      (v) Frames: 1
   (b) Carriers
      (i) Center Freq (MHz): 0 – This controls the frequency offset for all carriers in the list.
      (ii) Relative Amplitude (dBc/Hz)
      (iii) Check the box for carrier 1 On
      (iv) Freq (MHz): 0 – This controls the frequency offset for carrier 1.
      (v) Amp (dB rel): 0
      (vi) Bandwidth: 5 MHz TM3.1
   (c) TSW3100 Control
      (i) Select *master.*
      (ii) Select *16b QDAC*.
      (iii) Select *Two's Comp.*
      (iv) Select *Load and Run.*
      (v) Select *16b MSB Justify*.
      (vi) Ensure that IP setting is correct (see SLLU101).
3. The TSW3100 appears as shown in Figure 25.

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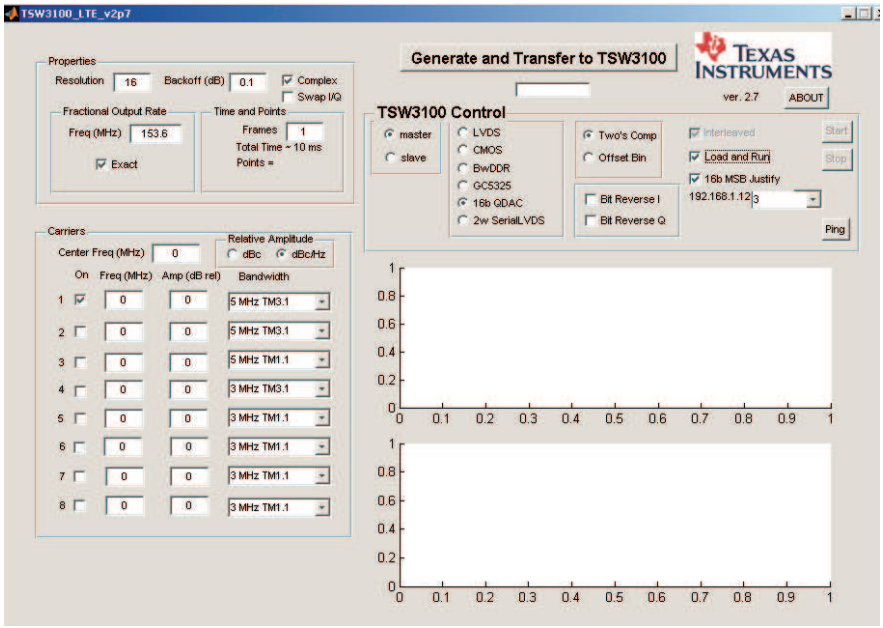

Figure 25. TSW3100 LTE GUI

4. Click on the gray button *Generate and Transfer TSW3100*. When the TSW3100 is finished, the TSW3100 appears as shown in Figure 26. This process takes 1 to 2 minutes.
   Version 2p7 of the TSW3100 does have some errors in generating certain LTE signals. This will be fixed in a later version of the TSW3100 software. The following signal types are generated correctly in version 2p7.
   (a) TM3.1 single carrier for 5-MHz, 10-MHz, 15-MHz, and 20-MHz bandwidths (1.4-MHz and 3-MHz do not demodulate).
   (b) TM1.1 single carrier for 5-MHz and 10-MHz bandwidths (1.4-MHz and 3 MHz do not demodulate).

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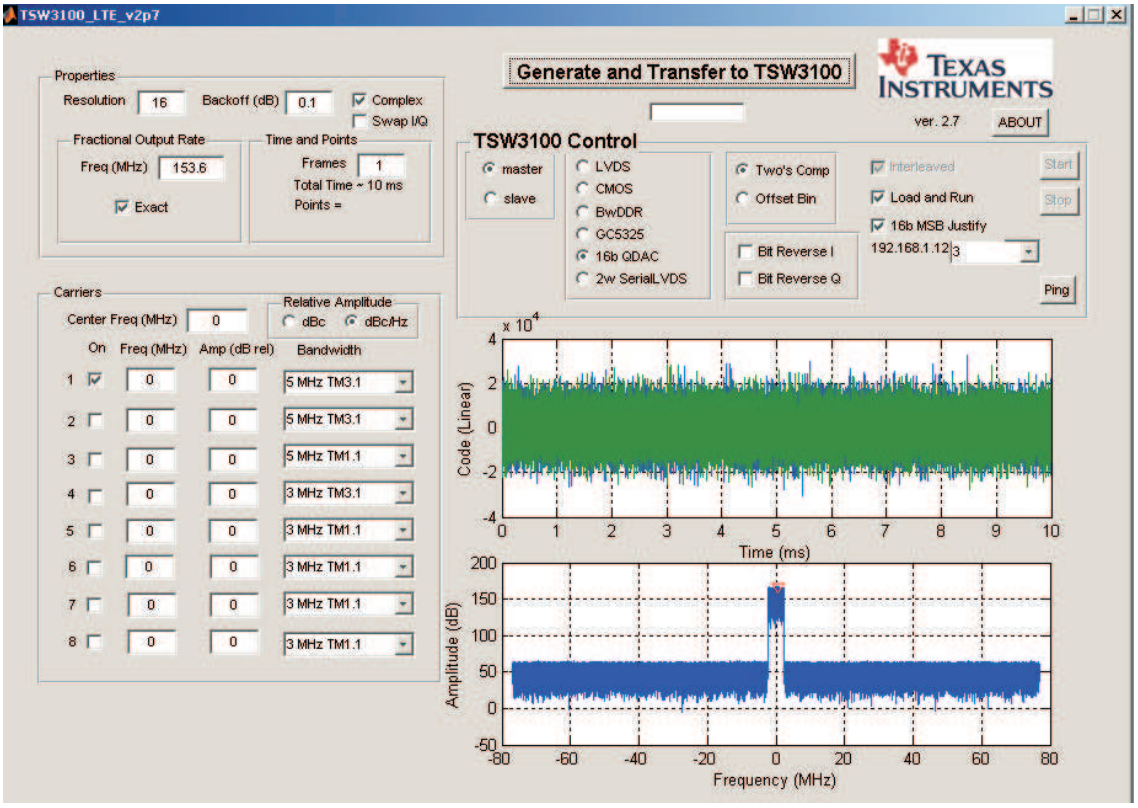

Figure 26. TSW3100 LTE GUI After Waveform Created

5. Verify that the following TSW3100 LEDs are illuminated. If these LEDs are not illuminated, verify that the TSW3725 is connected properly and its default settings are loaded,
   (a) D14: PAT GEN CLK
   (b) D15: PAT GEN RUN
6. If TSW3100 LED D16: FIFO EMPTY ERROR is illuminated, then the TSW3100 did not load correctly and step 4 needs to be repeated. If this continues, then power cycle the TSW3100 board before repeating step 4.
7. Ensure that the TSW3725 hardware is programmed with the *default_config.m* file.
8. The TSW3725 TX1 or TX2 output with these settings must have a 5-MHz LTE signal centered at 2143.6 MHz. This can be calculated by the following equation.
   (a) LO frequency = 1990 MHz
   (b) Coarse mixer = Fs/4 = 614.4/4 = 153.6 Hz
   (c) Tone Center in TSW3100 GUI = 0 MHz
   (d) Equation = LO frequency + coarse mixer + tone center = 1990 MHz + 153.6 MHz +0 MHz = 2143.6 MHz

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7 GUI Functions

This section describes how to program each panel of the TSW3725 GUI.

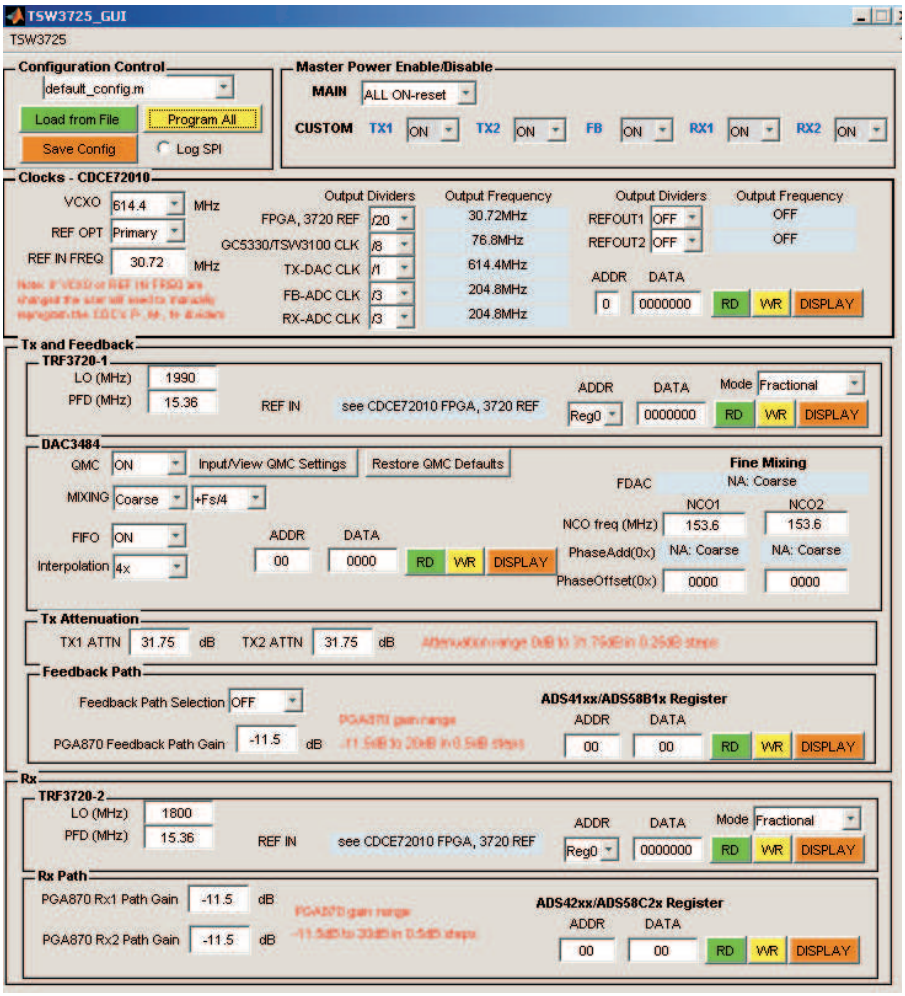

Figure 27. TSW3725 GUI

7.1 Configuration Control Panel

The Configuration Control panel consist of the following.

1. **Display Configuration box:** displays the configuration file that is loaded when *Program All* is selected.
2. **Load from File button:** when pressed, allows the user to select which configuration to load.
3. **Program All button:** when pressed, the TSW3725 hardware is programmed with the configuration displayed in the *Display Configuration Box*.
4. **Save Config button:** when pressed, allows user to save the configuration currently displayed in the TSW3725 to a new configuration file name.
5. **Log SPI radio button:** when selected, the TSW3725 records all the SPI commands sent to the *TSW3725 in the file tsw3725_SPI_commands.csv*.

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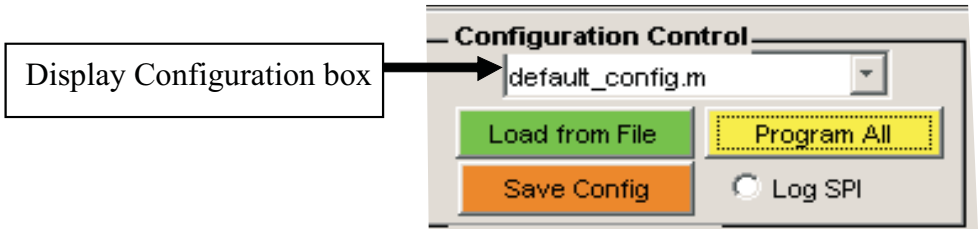

Figure 28. Configuration Control Panel

At Start Up

When the TSW3725 is first started, the Configuration Control panel appears as shown in Figure 29. Notice that the *Save Configuration* button has been blacked out. This implies that no configuration has been loaded to the TSW3725 hardware yet.

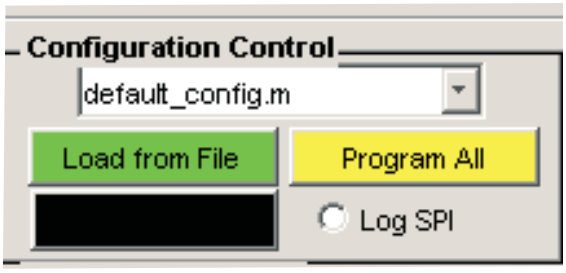

Figure 29. Configuration Control Panel on Initial Start-Up

Loading the Default Config

To load the file named *default_config.m*, press the *Program All* button. After the *Program All* button has been pressed, it turns white and provides status updates on the TSW3725 hardware section that is being programmed. After the TSW3725 hardware programming is complete, the *Program All* button displays the word *Done*; then it turns yellow and displays *Program All*. This process takes approximately 25 seconds.

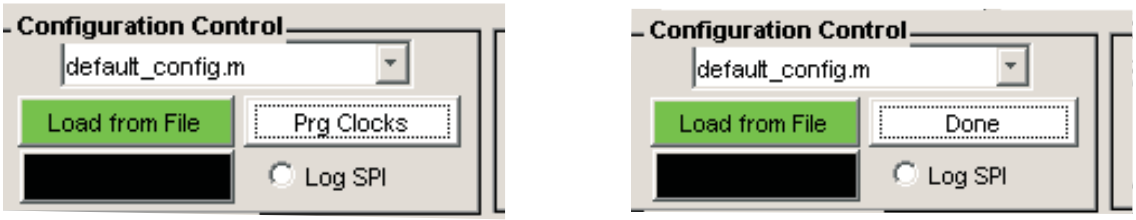

Figure 30. Configuration Control Panel While Programming the TSW3725

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If the TSW3725 hardware is not powered up, or if SW2 is in the wrong state (see Section 4.1), or if the TSW3725 USB cable is not connected, then the TSW3725 GUI fails to connect to the TSW3725 hardware. When the GUI fails to connect to the TSW3725 hardware, the Configuration Control panel displays the term *usb not connected* in the *Program All* button as shown in Figure 31. If this happens, fix the connection problem, and then press the *Program All* button again. Note: the *Program All* button still reads *usb not connected* when the button is pressed the second time.

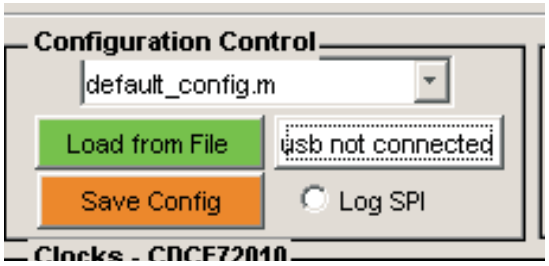

Figure 31. Configuration Control Panel When TSW3725 not Powered Up or USB Cable Not Connected

The *default_config.m* file is set up for Band 1 LTE and Band 1 WCDMA frequencies. To improve TX carrier suppression and sideband suppression numbers, see the immediately following section.

Loading Other Configuration Files

To load a configuration file other than the one displayed in the Display Configuration Box, press the *Load from File* button. The following file loader is displayed. Select the desired **_config.m* , and press the *Open* button. The Display Configuration Box now displays the new configuration file name. To load this new configuration file, press the *Program All* button.

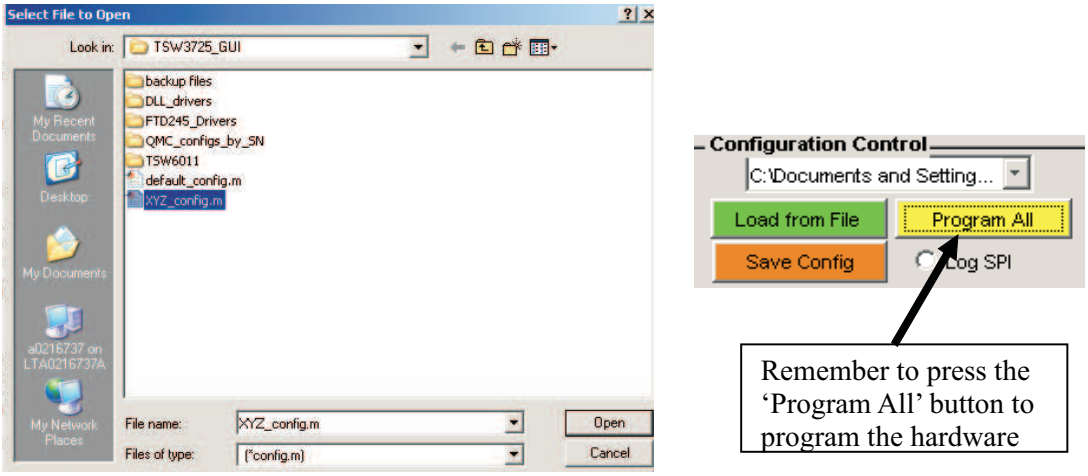

Figure 32. Configuration Control – Loading Other Configuration Files

The *default_config.m* file is setup for Band 1 LTE and Band 1 WCDMA frequencies. To improve TX carrier suppression and sideband suppression numbers for Band 1 LTE and Band 1 WCDMA at 25C, some board-specific files are available in the *QMC_configs_by_SN* (TSW3725 Stand-Alone mode) and *QMC_configs_by_SN/SCBP configs* (TSW3725 SCBP mode) directories located in the main TSW3725 GUI directory. These files have factory-adjusted DAC3484 settings that correct for offset, phase, and gain errors in the TX modulator. If this file does not exist for a certain serial number, one can either perform a self-calibration using the *DAC3484: QMC CONTROL* GUI or contact the factory to see if this file was created after the latest TSW3725 software release. **Refer to section 7.5.2** for instructions on how to program the *DAC3484: QMC CONTROL* GUI.

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Saving a New Configuration File

In some cases, the user may modify the settings in the TSW3725 GUI and want to save these settings to a unique file. To save the configuration currently programmed in the TSW3725 to a new file, press the *Save Configuration* button. The following file box is displayed (Figure 33). Save the file to a unique filename. The filename must end with *_config.m*.

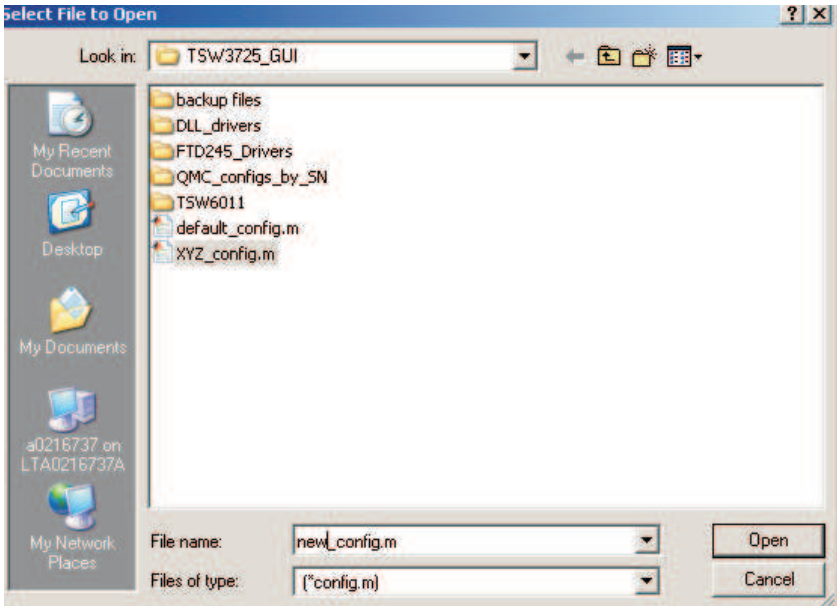

Figure 33. Configuration Control – Saving New Configuration Files

Log SPI Radio Button

By selecting the *Log SPI* radio button, the following happens:

1. The existing file *tsw3725_SPI_commands.csv* is removed.
2. A new file *tsw3725_SPI_commands.csv* is created.
3. All SPI commands are recorded in the file *tsw3725_SPI_commands.csv* until *Log SPI*' is deselected.

The file *tsw3725_SPI_commands.csv* has the following columns:

1. **chipid:** The FPGA on the TSW3725 selects which device the SPI command is sent to based on the chip ID number.
2. **spi_word_hex:** The hexadecimal word sent to the device that has been designated. This hexadecimal word includes the address and register bits in the order that the device is expecting.
3. **spi_word_length:** The length of the word sent to the designated device. This adds the number of address bits and register bits.
4. **addr_bin:** The address that is being programmed in binary form. This is another way of showing the same information in spi_word_hex.
5. **reg_bin:** The register bits in binary form that are sent to the address. This is another way of showing the same information in spi_word_hex.

This button allows the user to load any working configuration file and record all the spi commands sent to the TSW3725. At this point, the user can use the *tsw3725_SPI_commands.csv* to aid in programming the SCBP board to the user's unique configuration.

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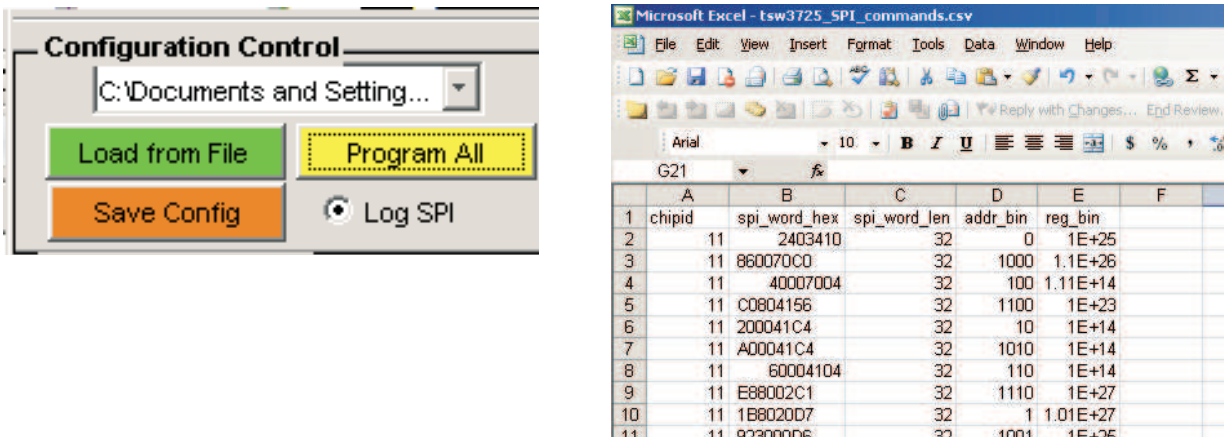

Figure 34. Log SPI

7.2 Master Power Enable/Disable Panel

The Master Power Enable/Disable panel consists of the following:

1. ***Main* pulldown menu:** allows the user three options (*ALL ON -reset*, *ALL-OFF-reset*, *CUSTOM*)
2. **Individual *Custom* pulldown menus**: In *CUSTOM* mode, these menus allow the user to power on or off individual sections of the TSW3725 hardware.

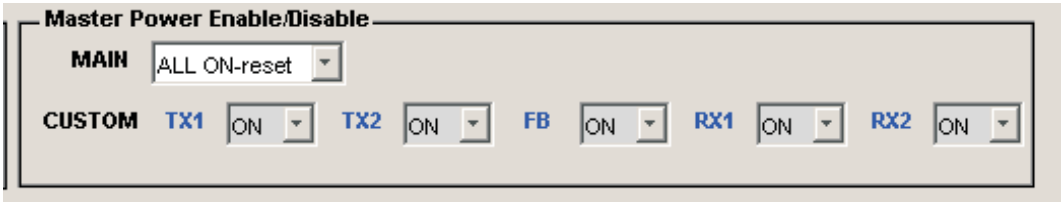

Figure 35. Master Power Enable/Disable Panel

The ability to quickly turn on and turn off large sections of circuitry can aid in debugging if the user is interested in optimizing performance. It also can be used to disable a specific signal chain if the user is interested in a subset of the TSW3725 functionality. The following tables describe the actions taken for certain combinations *CUSTOM* GUI settings.

Table 1. TX and FB Custom settings

TX1	TX2	TX3	Device State Changes
ON	ON	ON	All TX and FB components active
OFF	ON	ON	DAC3484: DAC A and B set to sleep mode DAC3484: QMC C&D GAIN = 0, QMC PHASE A and B = 0
ON	OFF	ON	DAC3484: DAC C and D set to sleep mode DAC3484: QMC C and D GAIN = 0, QMC PHASE C and D = 0
OFF	OFF	ON	DAC3484: DAC A, B, C, and D set to sleep mode DAC3484: QMC A, B, C, and D GAIN = 0, QMC PHASE A , B, C, and D = 0 DAC input clock output and divider from CDCE72010 disabled
ON	ON	OFF	FB PGA870 set to sleep mode FB ADC(ADS4149) set to sleep mode FB ADC input clock output and divider from CDCE72010 disabled

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Table 1. TX and FB Custom settings (continued)

TX1	TX2	TX3	Device State Changes
OFF	OFF	OFF	DAC3484: DAC A, B, C, and D set to sleep mode DAC3484: QMC A, B, C, and D GAIN = 0, QMC PHASE A and B, C and D = 0 DAC input clock output and divider from CDCE72010 disabled FB PGA870 set to sleep mode FB ADC(ADS4149) set to sleep mode FB ADC input clock output and divider from CDCE72010 disabled TX and FB LO (TRF3720-1) set to sleep mode TX and FB LO reference (TRF3720-1) output from CDCE72010 disabled (divider still enabled)

Table 2. RX Custom Settings

RX1	RX2	Device State Changes
ON	ON	All RX components active
OFF	ON	RX1 PGA870 set to sleep mode
ON	OFF	RX2 PGA870 set to sleep mode
OFF	OFF	RX1 and RX2 PGA870 set to sleep mode RX ADC(ADS4249) set to sleep mode RX ADC input clock output and divider from CDCE72010 disabled RX LO (TRF3720-2) set to sleep mode RX LO reference (TRF3720-2) output from CDCE72010 disabled (divider still enabled)

The MAIN pulldown menu options of *ALL ON-reset* and *ALL OFF-reset* are equivalent to programming a CUSTOM mode of TX1 = TX2 = FB = RX1= RX2 = ON and TX1 = TX2 = FB = RX1 = RX2 = OFF, respectively.

7.3 RD/WR/DISPLAY and the DISPLAY GUI

The TSW3725 GUI provides boxes and menus for the most common functions that the user will use to configure the TSW3725. However, for the less common options, the TSW3725 GUI has six RD/WR/DISPLAY options. These allow the user to program the serial interface directly to the following six parts.

1. CDCE72010
2. TRF3720-1 (TX LO)
3. DAC3484
4. ADS41xx/ADS58B1x (FB ADC)
5. TRF3720-2 (RX LO)
6. ADS42xx/ADS58C2x (RX dual ADC)

See the individual parts data sheets for part-specific register settings and functions.

Figure 36. Master Power Enable/Disable

The RD/WR/DISPLAY section consist of the following:

1. **ADDR:** input a valid address from the data sheet to read from or write to.
2. **DATA:** when the RD button is pressed, this displays the data programmed in the ADDR specified; when the WR button is pressed, this writes the data in this box to the ADDR specified.
3. **RD:** when pressed, this reads register DATA from the ADDR specified.
4. **WR:** when pressed, this writes register DATA to the ADDR specified.
5. **DISPLAY:** when pressed, this calls the DISPLAY GUI for the device of interest. The DISPLAY GUI provides read-back information for all registers of a given device. See the following *Display GUI* section for a more detailed description.

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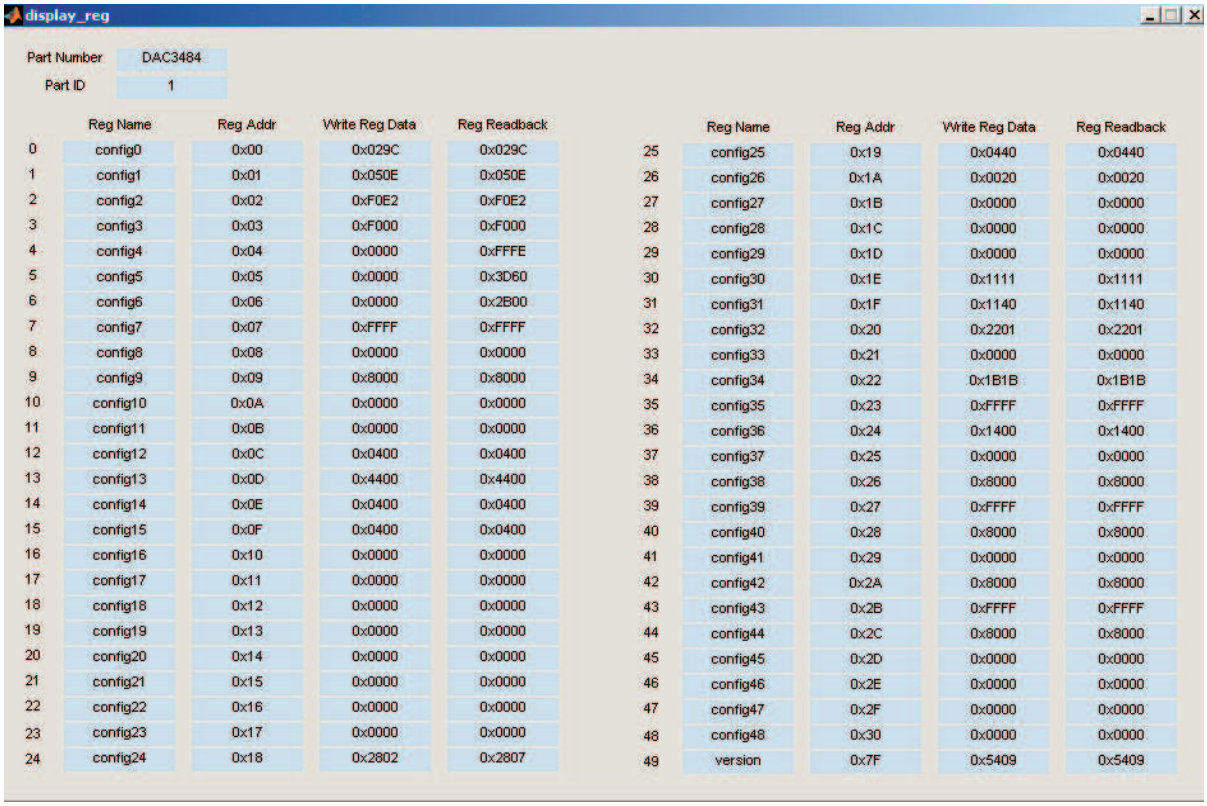
7.4 DISPLAY GUI

The DISPLAY GUI is used to quickly verify all register settings for a device. It also allows the user to compare the register data that was written to the part versus the register data read from the part. If a mismatch in the data written versus the data read is found, this may mean that the register is a read-only register or that an issue exists and the TSW3725 needs to be reprogrammed.

The DISPLAY GUI is a read-only GUI. It also does not update automatically when a change is made in the TSW3725 GUI. To see the new updates in the DISPLAY GUI, the user needs to press the DISPLAY button in the TSW3725 GUI.

The DISPLAY GUI consist of the following:

1. **Part Number:** displays the part number whose serial register information is displayed.
2. **Part ID:** This number refers to the ID number that the MATLAB™ software sends to the TSW3725 hardware to program a certain device.
3. **Reg Name:** in the individual device data sheet, the registers are given a name assignment for each register address.
4. **Reg Addr:** the register address programmed, displayed in hexadecimal format (MSB to LSB).
5. **Write Reg Data:** displays the data that was most recently written to a specific register address, displayed in hexadecimal format (MSB to LSB).
6. **Reg Readback:** displays the actual data read back from the device's specific register address, displayed in hexadecimal format (MSB to LSB).



	Reg Name	Reg Addr	Write Reg Data	Reg Readback
0	config0	0x00	0x029C	0x029C
1	config1	0x01	0x050E	0x050E
2	config2	0x02	0xF0E2	0xF0E2
3	config3	0x03	0xF000	0xF000
4	config4	0x04	0x0000	0xFFFE
5	config5	0x05	0x0000	0x3D60
6	config6	0x06	0x0000	0x2B00
7	config7	0x07	0xFFFF	0xFFFF
8	config8	0x08	0x0000	0x0000
9	config9	0x09	0x8000	0x8000
10	config10	0x0A	0x0000	0x0000
11	config11	0x0B	0x0000	0x0000
12	config12	0x0C	0x0400	0x0400
13	config13	0x0D	0x4400	0x4400
14	config14	0x0E	0x0400	0x0400
15	config15	0x0F	0x0400	0x0400
16	config16	0x10	0x0000	0x0000
17	config17	0x11	0x0000	0x0000
18	config18	0x12	0x0000	0x0000
19	config19	0x13	0x0000	0x0000
20	config20	0x14	0x0000	0x0000
21	config21	0x15	0x0000	0x0000
22	config22	0x16	0x0000	0x0000
23	config23	0x17	0x0000	0x0000
24	config24	0x18	0x2802	0x2807

	Reg Name	Reg Addr	Write Reg Data	Reg Readback
25	config25	0x19	0x0440	0x0440
26	config26	0x1A	0x0020	0x0020
27	config27	0x1B	0x0000	0x0000
28	config28	0x1C	0x0000	0x0000
29	config29	0x1D	0x0000	0x0000
30	config30	0x1E	0x1111	0x1111
31	config31	0x1F	0x1140	0x1140
32	config32	0x20	0x2201	0x2201
33	config33	0x21	0x0000	0x0000
34	config34	0x22	0x1B1B	0x1B1B
35	config35	0x23	0xFFFF	0xFFFF
36	config36	0x24	0x1400	0x1400
37	config37	0x25	0x0000	0x0000
38	config38	0x26	0x8000	0x8000
39	config39	0x27	0xFFFF	0xFFFF
40	config40	0x28	0x8000	0x8000
41	config41	0x29	0x0000	0x0000
42	config42	0x2A	0x8000	0x8000
43	config43	0x2B	0xFFFF	0xFFFF
44	config44	0x2C	0x8000	0x8000
45	config45	0x2D	0x0000	0x0000
46	config46	0x2E	0x0000	0x0000
47	config47	0x2F	0x0000	0x0000
48	config48	0x30	0x0000	0x0000
49	version	0x7F	0x5409	0x5409

Figure 37. DISPLAY GUI for DAC3484

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7.5 Clocks – CDCE72010 Panel

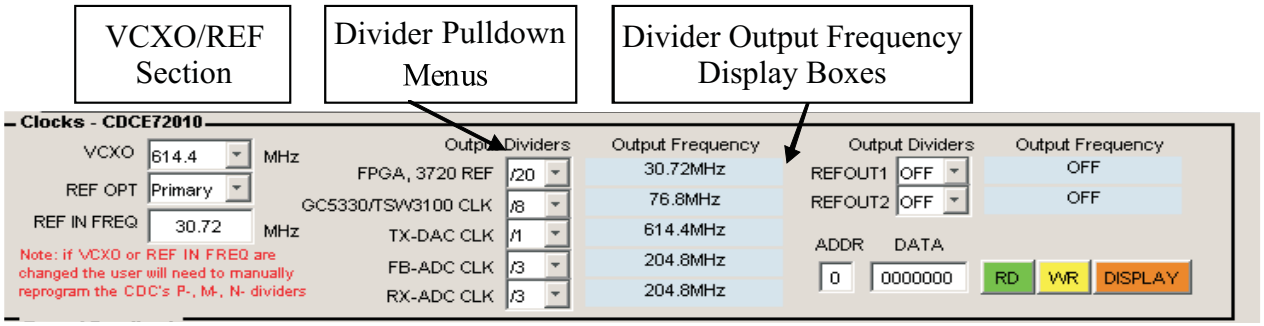

Figure 38. CDCE72010 Panel

The *Clocks – CDCE72010* panel consist of the following:

1. **VCXO/REF Section:**
   (a) VCXO: VCXO frequency in MHz, matches the frequency of schematic component Y1. The default hardware comes with a 614.4-MHz VCXO. If a different VCXO frequency is selected in the GUI, remember to manually reprogram the CDCE72010's P-, —, and N-dividers so that the VCXO and REF IN divide down properly.
   (b) REF OPT: Primary (default setting) or Secondary reference
      (i) The Primary reference is connected through the TSW3725 high-speed connector J8 on pin 179. This is the option used when the external reference is applied to J2 of the TSW3725 Adaptor Board or if the user has connected the digital baseband board.
      (ii) Secondary reference is the option used when the external reference is applied to J9 of the TSW3725 hardware.
   (c) REF IN FREQ: The default setting is 30.72 MHz. This is the frequency supplied to the connector described in the REF OPT section. If a different REF IN frequency is written to the GUI, remember to manually reprogram the CDCE72010's P-, —, and N-dividers so that the VCXO and REF IN divide down properly. This frequency must meet the CDCE72010 data sheet frequency and amplitude specifications.
2. **Divider Pulldown Menus:** Allows for direct programming of seven of the CDCE72010 output divider frequencies. The default setting for each is provided in Table 3. These settings are the defaults based on the TSW3725 default hardware configuration used with the TSW3100 for driving the TX chain.
   (a) For the most part, if any of these settings are changed, then some hardware modifications are required.
   (b) The FPGA, 3720 reference must not be programmed *OFF* in most cases, as this is the clock supplied to the FPGA that allows the serial interface programming to work.
   (c) The TSW3100 CLK is calculated by this equation: VCXO frequency/(DAC3484 interpolation setting × 2). The × *2* in the denominator is due to the DDR clock of the DAC3484.
   See Table 3 for individual divider information.

Table 3. Divider Pulldown Menu Description

Divider Pulldown Menu Name	CDCE72010 Pin Name/Signal Type	TSW3725 Function
FPGA, 3720 REF	U0N/LVCMOS U1P/LVCMOS U1N/LVCMOS	FPGA clock reference TRF3720-1 reference input (TX and FB) TRF3720-2 reference input (RX)
REFOUT1	U2P/LVCMOS	Sent to SMA connector J10 (ac coupled)
RX-ADC CLK	U4P/LVCMOS	Sent to Bandpass filter, converted to a differential signal via a transformer than sent to RX Dual ADC
FB-ADC CLK	U5P/LVCMOS	Sent to Bandpass filter, converted to a differential signal a via transformer than sent to Feedback ADC
REFOUT2	U6P/LVCMOS	Sent to MCX connector J38 (dc coupled)

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Table 3. Divider Pulldown Menu Description (continued)

Divider Pulldown Menu Name	CDCE72010 Pin Name/Signal Type	TSW3725 Function
TX-DAC CLK	U7/LVPECL	DAC3484 DACCLK pins
GC5330/TSW3100 CLK	U8/LVDS	Sent to high-speed connector J8. J8 connects to the TSW3725 adaptor board for the TSW3100 FPGA clock, or to the digital baseband board for the GC5330 clock

(d) **Divider Output Frequency Display Boxes:** these are display-only boxes for quick reference. The display boxes show the result of this equation, (VCXO frequency)/(output divider setting)

(e) **RD/WR/DISPLAY:** read/write programmability of the CDCE72010 serial interface. See the 'RD/WR/DISPLAY' section for more details.

7.6 TX and Feedback Panel

7.6.1 TRF3720-1 Panel

The 'TRF3720-1' panel consists of the following:

1. **LO (MHz):** Type in the desired LO frequency and press enter. Several TRF3720 register values are automatically calculated and updated when the LO frequency is changed. This text box will turn red if the REF IN frequency in the CDCE72010 menu changes after the TRF3720 is programmed. The red indicates the TRF3720 needs to be reprogrammed. The REF IN text box will also turn red and state 'REF from CDC changed, update LO'. To reprogram the TRF3720 set your cursor in the LO text box and press enter.
2. **PFD (MHz):** Type in the desired PFD frequency and press enter. Several TRF3720 register values are automatically calculated and updated when the PFD frequency is changed. This text box will turn red if the TRF3720 reference frequency from the CDCE72010 device is not an integer multiple of the PFD frequency. The REF IN text box will also turn red and state 'PFD&REFIN, are not integer multiples'. To correct this, enter a PFD frequency that is an integer sub-multiple of the TRF3720 reference frequency.
3. **REF IN:** A text box that reminds the user that the TRF3720 reference input frequency is set by one of the CDCE72010 output dividers. When this box turns red it indicates the TRF3720 register settings are not programmed correctly. The text in the box will either read 'PFD&REFIN, are not integer multiples' or 'REF from CDC changed, update LO'. The actions taken to correct these errors are described directly above in the LO (MHz) and PFD (MHz) descriptions.
4. **Mode:** Allows users to choose between Fractional and Integer mode. In Integer mode, the LO frequency is updated by rounding down to the next closest working integer LO frequency. Several TRF3720 register values are automatically calculated and updated when the mode is switched from integer to fractional or vice versa.
5. **RD/WR/DISPLAY:** read write programmability of the TRF3720 serial interface. See the *RD/WR/DISPLAY* section for more details.???

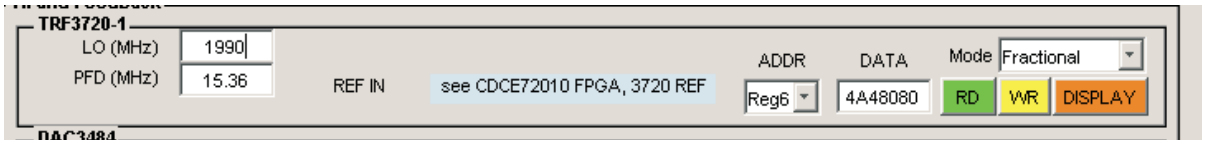

Figure 39. TRF3720-1 Panel

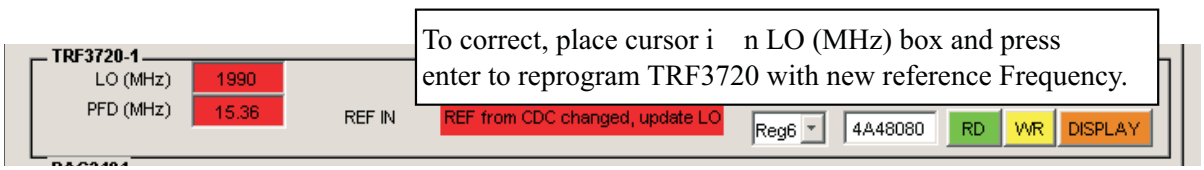

Figure 40. TRF3720-1 Error, TRF3720's Ref Is Changed in CDCE72010 Menu

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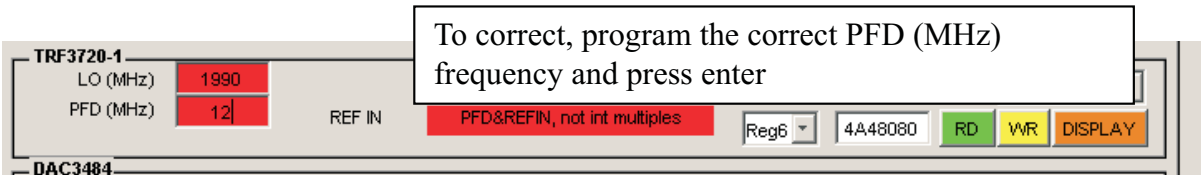

Figure 41. TRF3720-1 Error, REFIN Is Not an Integer Multiple of PFD.

7.6.2 DAC3484 Panel

The *DAC3484* panel consists of the following:

1. **QMC section (Quadrature Modulation Correction):** allows user to easily program the QMC section of the DAC3484. A detailed description of the QMC section is follows.
2. **Mixing options:** allows user to easily program the digital coarse or fine mixers in the DAC3484.
3. **FIFO menu:** allows user to turn the FIFO on or off. The default state is on.
4. **Interpolation menu:** allows users to select the 1x, 2x, 4x, 8x, or 16x interpolation modes. The default state is 4x interpolation. Changing the interpolation mode requires users to change the *GC5330/TSW3100CLK* frequency or the *TX-DAC CLK* frequency in the *Clock – CDCE72010* section, because TX-DAC CLK clock = (DAC input data rate x interpolation mode). The TSW3100 accepts a DDR clock; remember this when determining the *GC5330/TSW3100CLK*. The TSW3100 input waveform may need to be recalculated if the interpolation mode is changed.
5. **RD/WR/DISPLAY:** read/write programmability of the DAC3484 serial interface. See Section 7.3 for more details.

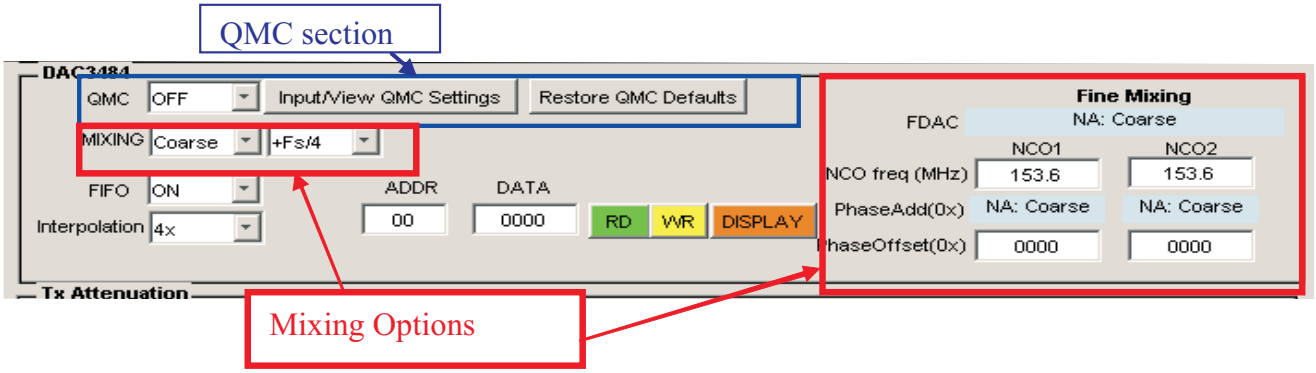

Figure 42. DAC3484 Panel

Detailed Descriptions:

1. **DAC3484 QMC section:**
   (a) **QMC pulldown menu:** allows the user to turn the DAC3484's QMC mode on or off.
   (b) **Restore QMC Defaults button:** When pressed, the default QMC settings are loaded from the configuration file that was loaded to the TSW3725 in the *Configuration Control* panel of the TSW3725 GUI. This allows the user the ability to reload the ideal QMC configuration setting without having to reload the **_config.m* file.
   (c) **Input/View QMC Settings button:** When pressed, the *DAC3484: QMC CONTROL* GUI is made available. The instructions to program this GUI are provided in the bottom left corner of the GUI window. This GUI allows the user to view/program the QMC offset, gain, and phase adjust values more efficiently than using the *RD/WR/DISPLAY* boxes provided in the DAC3484 panel. This allows users to find an ideal QMC setting for their specific board and conditions. The user can then save this setup to a new configuration file using the *Save Configuration* button in the *Configuration Control* panel of the TSW3725 GUI.

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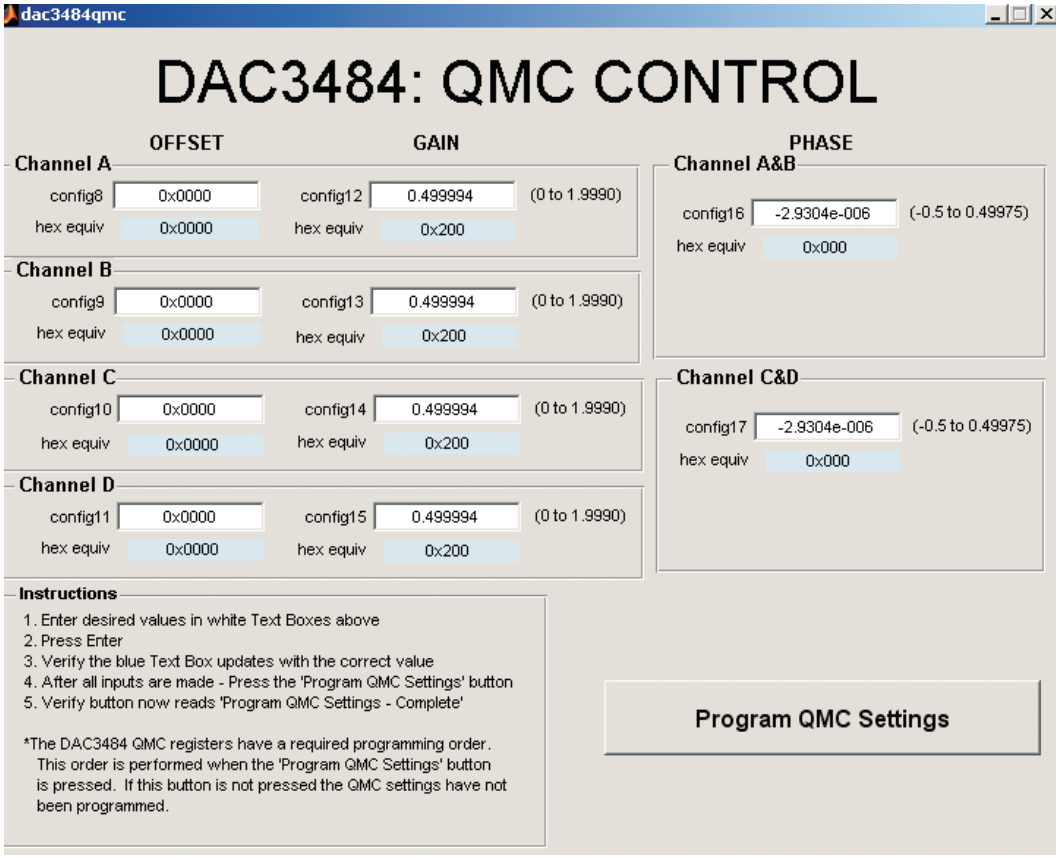

Figure 43. DAC3484 QMC CONTROL

2. **QMC Carrier Correction Technique Hints**
   (a) For TX1: modify Channels A & B OFFSET configurations.
   (b) For TX2: modify Channels C & D OFFSET configurations.
   (c) Set TSW3725 TX paths to minimum attenuation (**see section 7.6.3**)
   (d) Monitor the appropriate channels TX carrier frequency (LO frequency) amplitude on a spectrum analyzer.
   (e) After programming a new OFFSET configuration, verify this lowered the amplitude of the carrier on a spectrum analyzer.
   (f) Example TX1:
      (i) Record carrier amplitude with default settings.
      (ii) Change Channel A offset to 0x0100.
         – If carrier amplitude decreases, change Channel A offset to 0x0200.
         – If carrier amplitude increases, change Channel A offset to 0x1FF.
      (iii) Continue increasing or decreasing offset values until no improvement is seen.
      (iv) Change Channel B offset to 0x0100.
         – If carrier amplitude decreases, change Channel A offset to 0x0200.
         – If carrier amplitude increases, change Channel A offset to 0x1FF.
      (v) Continue increasing or decreasing offset values until no improvement seen.
      (vi) Repeat Step b to e, except this time, vary the hexadecimal location denoted by an Y; 0x00Y0.
      (vii) Repeat Step b to e, except this time, vary the hexadecimal location denoted by an Z; 0x000Z.

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3. **QMC Sideband Correction Technique Hints**
   (a) For TX1: modify Channels A and B GAIN, PHASE configurations.
   (b) For TX2: modify Channels C and D GAIN, PHASE configurations.
   (c) Set TSW3725 TX paths to minimum attenuation (**see section 7.6.3**).
   (d) Monitor the appropriate channels TX sideband frequency (LO frequency) amplitude on a spectrum analyzer.
   (e) After programming a new GAIN or PHASE configuration, verify this lowered the amplitude of the carrier on a spectrum analyzer.
   (f) Example TX1:
      (i) Record sideband amplitude with default settings.
      (ii) Change Channel A gain to 0.498.
         – If sideband amplitude decreases, change Channel A gain to 0.497.
         – If sideband amplitude increases, change Channel A gain to 0.501.
      (iii) Continue increasing or decreasing gain values until no improvement is seen.
      (iv) Now Change Channel B gain to 0.498.
         – If sideband amplitude decreases, change Channel A gain to 0.497.
         – If sideband amplitude increases, change Channel A gain to 0.501.
      (v) Continue increasing or decreasing offset values until no improvement is seen.
      (vi) Change Channel A&B Phase to 0.001.
         – If sideband amplitude decreases, change Channel A&B phase to 0.002.
         – If sideband amplitude increases, change Channel A&B phase to –0.001.
      (vii) Repeat Steps b to d except varying smaller significant digits for each setting; repeat until sideband amplitude is acceptable or cannot be decreased anymore.

4. **DAC3484 Mixing Options:**
   (a) **Mixer Selection menu:** Allows the user to select between the Coarse Mixer, the Fine Mixer, and the option of turning the coarse and fine digital mixers in the DAC3484 off.
   (b) **Coarse Mixer Programming menu:** Enabled when the *Mixer Selection* menu is set to Coarse. Allows user to chose between the coarse mixer frequency settings of –Fs/4, +Fs/2, +Fs/4, +Fs/8, –3Fs/8, +3Fs/8, and –Fs/8. When the *Mixer Selection* menu is set to Fine or Off, the Coarse Mixer Programming turns gray and displays the word *N/A*.
   (c) **Fine Mixer Programming section:** Enabled when the *Mixer Selection* menu is set to Fine. When Fine Mixing is enabled, the FDAC text box displays the same frequency that is shown in the CDCE72010 'TX-DAC CLK' output frequency text box. The user can manually enter the NCO frequencies and phase offset for both NCOs in this section. After a value is entered, press *enter* and the GUI programs the DAC3484 to the new setting. The PhaseADD text boxes are updated after a new NCO freq (MHz) or FDAC frequency are programmed.

The following examples show what the Fine Mixer Programming section looks like when the Mixer Selection box is set to Coarse, Fine, or OFF.

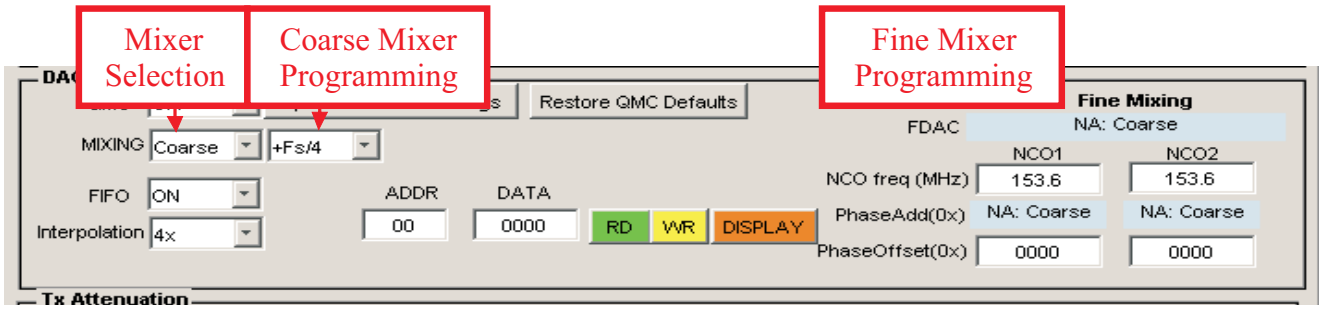

Figure 44. DAC3484 Mixing Options – Coarse Mixing

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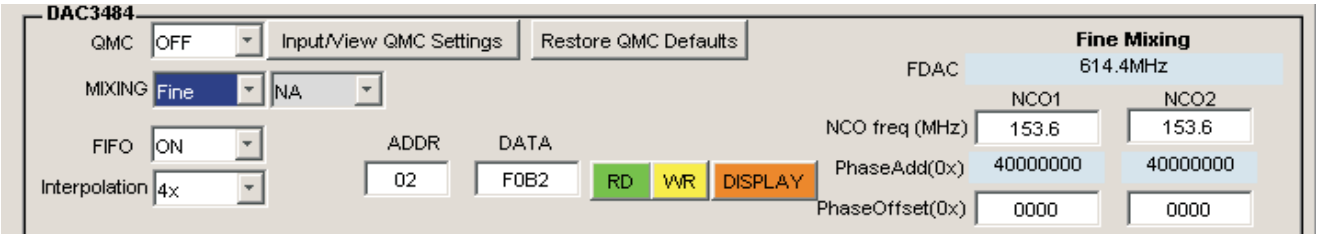

Figure 45. DAC3484 Mixing Options – Fine Mixing

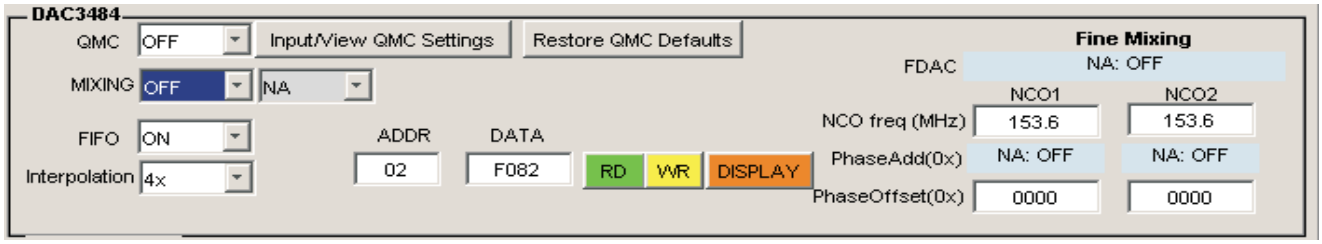

Figure 46. DAC3484 Mixing Options – OFF

7.6.3 TX Attenuation Panel

The TX Attenuation panel allows for individual control of the attenuators on the TX1 and TX2 paths. The default attenuators on the TSW3725 have an attenuation range from 0 dB to 31.75 dB in 0.25-dB steps. In the default_config configuration file, the attenuation settings default to the maximum attenuation of 31.75 dB to reduce the chances of damaging components connected to the TX1 and TX2 output SMA connectors.

To program a different attenuation setting in the GUI, type a new value and press *Enter*. If an improper value is typed, then the GUI software automatically modifies the value to the closest valid attenuation setting.

Figure 47. TX Attenuation Panel

7.6.4 Feedback Path Panel

The *Feedback Path* panel consists of the following:

1. **Feedback Path Selection:** The TSW3725 has a shared feedback path for TX1 and TX2. The Feedback Path Selection menu has three options – FB1, FB2, or OFF. This menu allows the user to control the RF switch that selects the SMA to feedback path 1 (FB1), the SMA to feedback path 2 (FB2), or it deselects both feedback paths (OFF).
2. **PGA870 Feedback Path Gain:** Allows the user the ability to set the gain of the PGA870 in the feedback path. The PGA870 has a gain range of -11.5 to 20 dB in 0.5-dB steps. To program a different gain setting in the GUI, type a new value and press *Enter*. If an improper value is typed, then the GUI software automatically modifies the value to the closest valid gain setting. The PGA870 does have a power-down mode, but that can only be programmed via the *Master Power Enable/Disable* panel of the TSW3725 GUI.
3. **RD/WR/DISPLAY:** Generally, the ADC settings remain constant after the TSW3725 is initialized. However, read/write programmability of the Feedback ADC serial interface is provided. See the *RD/WR/DISPLAY* section for more details.

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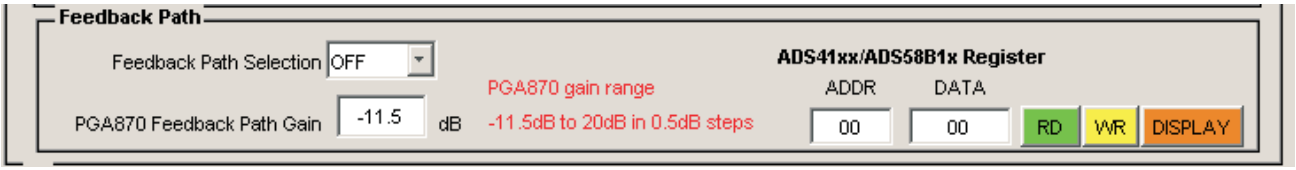

Figure 48. Feedback Path Panel

7.7 RX Panel

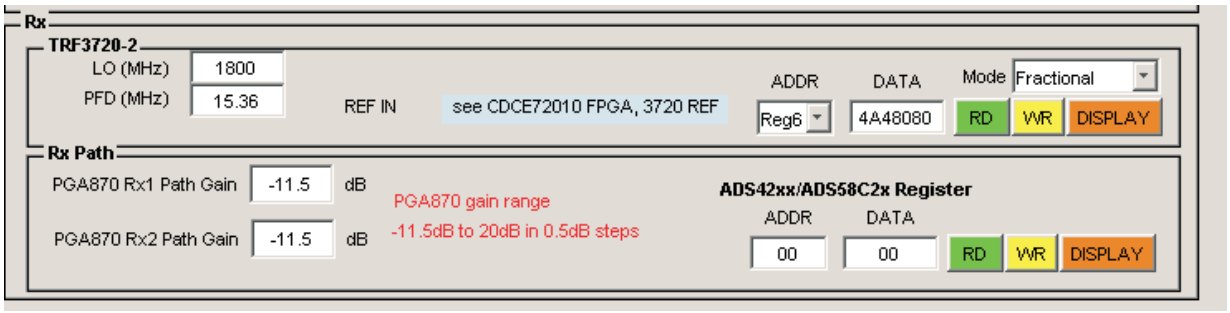

Figure 49. RX Path

7.7.1 TRF3720-2 Panel

The TRF3720-2 panel provides the LO frequency for the RX1 and RX2 mixers. Programming of this panel is identical to TRF3720-1 panel in the TX section. See *TX and Feedback, TRF3720-1* for an overview of this panel.

7.7.2 RX Path Panel

The RX Path panel gives the user the ability to program the RX path 1 PGA870 gain, RX path 2 PGA870 gain, and the Dual RX ADC. This panel behaves much like the *TX and Feedback, Feedback Path* programming. See *TX and Feedback, Feedback Path* for an overview of this panel.

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8 Typical Performance Numbers

8.1 TSW3725 Electrical Characteristics

PARAMETER	TEST CONDITION	TYP	UNIT
DC PARAMETERS			
Supply voltage		6	V
Supply current	TX1, TX2, FB, RX1, RX2 ON; default configuration	3.2	A
		19.2	W
PWDN current	TX1, TX2, FB, RX1, RX2 PWDN; default configuration	1.9	A
		11.4	W
SERIAL INTERFACE PARAMETERS			
FCLK (maximum)		5	MHz

8.2 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, TX attn = 0 dB, DAC3484 IF=153.6 MHz, DAC3484 QMC gain setting = 0.5, DAC clk = 614.4 MHz, Fractional LO

PARAMETER		TEST CONDITION	TYP	UNIT
TRANSMIT PARAMETERS				
TX LO		Default schematic		
	Max freq	Limited by LPF on LO path	2200	MHz
	Min freq	Limited by splitter on LO path	1350	MHz
RF output power		RFOut = 1550 MHz to 2250 MHz	6	dB
RF output attenuation	Max		31.75	dB
	Min		0	dB
	step size		0.25	dB
Gain flatness		RF = 1650 MHz to 2250 MHz, TX attn = 0	1	dB
		RF = 1650 MHz to 2250 MHz, TX attn = 15	1	dB
Output noise		Pout = –16 dBm, integrate 1 kHz to 10 MHz		
		RF out = 1550 MHz	410	mdeg
		RF out = 1900 MHz	360	mdeg
		RF out = 2250 MHz	380	mdeg
OIP2		RF out = 2050 MHz; fbb = 5 MHz, 6 MHz	45	dBm
OIP3		RF out = 2050 MHz; fbb = 5 MHz, 6 MHz	33	dBm
Sideband suppression	Unadjusted		–38	dBc
	Adjusted	Hand-tuned for given temp/frequency	–70	dBc
Carrier	Unadjusted		–22	dBm
	Adjusted	Hand-tuned for given temp/frequency	–70	dBm
Crosstalk		TX2 to TX1 (aggressor to victim)	68	dB
		FB1 to TX1	95	dB
		FB2 to TX1	95	dB
		RX1 to TX1	90	dB
		RX2 to TX1	90	dB
		TX1 to TX2 (aggressor to victim)	78	dB
		FB1 to TX2	85	dB
		FB2 to TX2	95	dB
		RX1 to TX2	90	dB
		RX2 to TX2	90	dB

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8.3 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, TX attn = 0 dB, DAC3484 IF=153.6 MHz, DAC3484 QMC gain setting = 0.5, DAC clk = 614.4 MHz, Fractional LO

PARAMETER	TEST CONDITION	TYP	UNIT
TRANSMIT PARAMETERS			
ACPR LTE Single Carrier TM1.1			
ACPR: 5 MHz BW	RF out = 1700 MHz	–70	dBc
	RF out = 2050 MHz	–70	dBc
ACPR: 10 MHz BW	RF out = 1700 MHz	–69	dBc
	RF out = 2050 MHz	–69	dBc
ACPR: 20 MHz BW	RF out = 1700 MHz	–67	dBc
	RF out = 2050 MHz	–67	dBc
EVM LTE Single Carrier TM			
EVM: 5 MHz BW	RF out = 1700 MHz	0.85	%rms
	RF out = 2050 MHz	0.85	%rms
EVM: 10 MHz BW	RF out = 1700 MHz	0.85	%rms
	RF out = 2050 MHz	0.85	%rms
EVM: 20 MHz BW	RF out = 1700 MHz	0.85	%rms
	RF out = 2050 MHz	0.85	%rms

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8.4 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, RX PGA Gain = 20 dB, IF Frequency=140 MHz, ADC clk = 204.8 MHz, Fractional LO = 1800 MHz

PARAMETER		TEST CONDITION	TYP	UNIT
RECEIVE PARAMETERS				
RX LO		Default schematic		
	Max freq	Limited by LPF on LO path	2200	MHz
	Min freq	Limited by splitter on LO path	1350	MHz
IF filter		Frequency	140	MHz
		BW	20	MHz
IF programmable gain	Max		20	dB
	Min		–11.5	dB
	Step size		0.5	dB
Idle channel noise		LO=1880 MHz	–153	dBF_S/Hz
SNR		ADC amplitude = –1 dBFs, PGA = 20 dB notch 6.25 MHz BW LO noise around carrier	65	dBc
HD2		ADC input amplitude = –1 dBFs, PGA = 10 dB	73	dBc
HD3		ADC input amplitude = –1 dBFs, PGA = 10 dB	65	dBc
Maximum RF input amplitude		ADC input amplitude = –1 dBFs, PGA = 20 dB	–9	dBm
		ADC input amplitude = –1 dBFs, PGA = 10 dB	1	dBm
		ADC input amplitude =–1 dBFs, PGA = 5 dB	6	dBm
P1dB		RX input	8	dBm
OIP3		PGA = 20 dB, RF1 = 1690 MHz, RF2 = 1700.7 MHz, LO = 1840 MHz, Ain = –9 dB	40	dBm
EVM LTE Single Carrier LTE Uplink(SC-FDMA), 64QAM				
EVM: 5 MHz BW		RF in = 1700 MHz, RX input power = –30 dBm	0.7	%rms
		RF in = 2050 MHz, RX input power = –30 dBm	0.8	%rms
EVM: 10 MHz BW		RF in = 1700 MHz, RX input power = –30 dBm	0.8	%rms
		RF in = 2050 MHz, RX input power = –30 dBm	0.8	%rms
EVM: 20 MHz BW		RF in = 1700 MHz, RX input power = –30 dBm	0.8	%rms
		RF in = 2050 MHz, RX input power = –30 dBm	0.9	%rms

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8.5 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, RX PGA Gain = 20 dB, IF Frequency=153.6 MHz, ADC clk = 204.8 MHz, Fractional LO = 1990 MHz

PARAMETER	TEST CONDITION	TYP	UNIT
FEEDBACK PARAMETERS			
FB LO	Default schematic		
Max freq	Limited by LPF on LO path	2200	MHz
Min freq	Limited by mixer input frequency range	1700	MHz
FB Filter	Frequency	153.6	MHz
	BW	100	MHz
FB programmable gain			
Max		20	dB
Min		-11.5	dB
step size		0.5	dB
Idle channel noise	LO = 2140 MHz	150	dBF_S/Hz
SNR	ADC amplitude = –1 dBFs, PGA=20dB notch 6.25 MHz BW LO noise around carrier	63	dBc
HD2	ADC input amplitude = –1 dBFs, PGA = 20 dB	73	dBc
HD3	ADC input amplitude = –1 dBFs, PGA = 20 dB	87	dBc
Maximum RF input amplitude	ADC input amplitude = –1 dBFs, PGA = 20 dB	-3	dBm
	ADC input amplitude = –1 dBFs, PGA = 10 dB	7	dBm
	ADC input amplitude = –1 dBFs, PGA = 5 dB	12	dBm
P1dB	RX input	23.3	dBm
OIP3	PGA = 20 dB, RF1 = 1847 MHz, RF2 = 1846 MHz, LO = 2000 MHz, Ain = –6.5 dB	41	dBm
ACPR LTE Single Carrier TM1.1			
ACPR: 5 MHz BW	RF in = 1700 MHz; FB input power = –10 dBm	-67	dBc
	RF in = 2050 MHz; FB input power = –10 dBm	-67	dBc
ACPR: 10 MHz BW	RF in = 1700 MHz; FB input power = –10 dBm	-65	dBc
	RF in = 2050 MHz; FB input power = –10 dBm	-65	dBc
ACPR: 20 MHz BW	RF in = 1700 MHz; FB input power = –10 dBm	-62	dBc
	RF in = 2050 MHz; FB input power = –10 dBm	-62	dBc
EVM LTE Single Carrier TM3.1			
EVM: 5 MHz BW	RF in = 1700 MHz; FB input power = –20 dBm	0.6	%rms
	RF in = 2050 MHz; FB input power = –20 dBm	0.6	%rms
EVM: 10 MHz BW	RF in = 1700 MHz; FB input power = –20 dBm	0.6	%rms
	RF in = 2050 MHz; FB input power = –20 dBm	0.6	%rms
EVM: 20 MHz BW	RF in = 1700 MHz; FB input power = –20 dBm	0.7	%rms
	RF in = 2050 MHz; FB input power = –20 dBm	0.7	%rms

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9 Typical Performance Plots

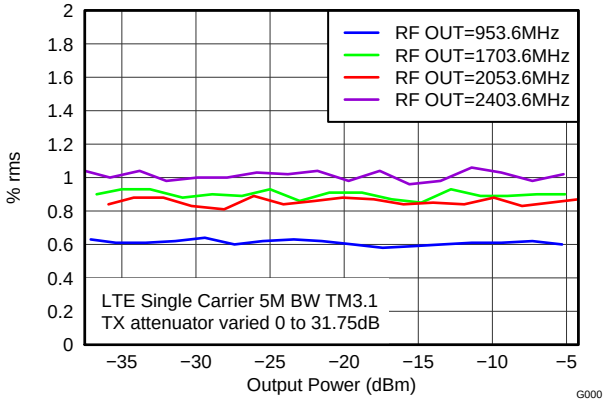

Figure 50. Tx EVM vs Frequency/Attenuation LTE 5 MHz TM3.1

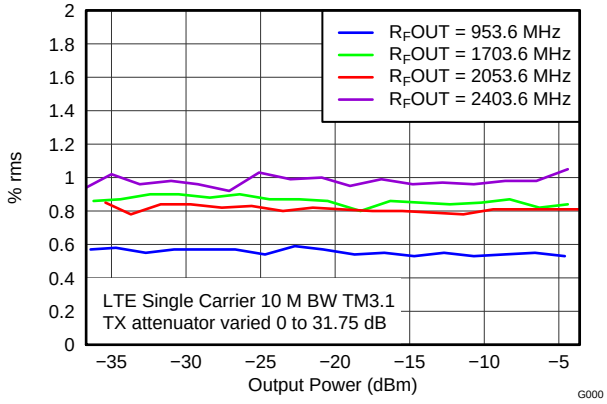

Figure 51. Tx EVM vs Frequency/Attenuation LTE 10 MHz TM3.1

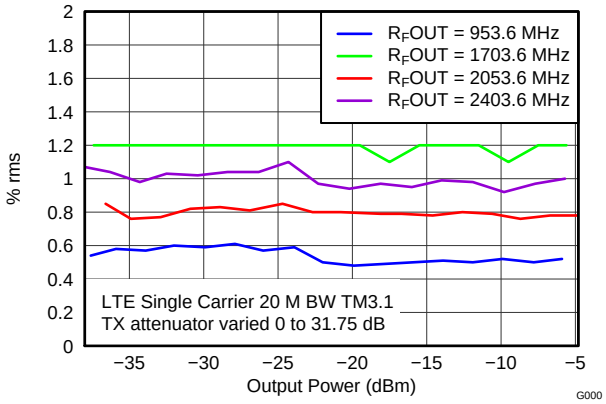

Figure 52. Tx EVM vs Frequency/Attenuation LTE 20 MHz TM3.1

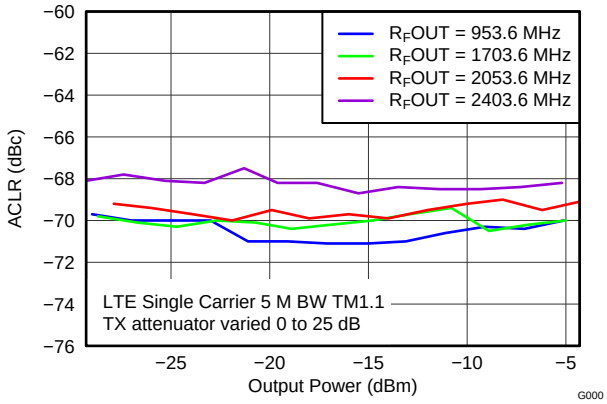

Figure 53. Tx ACLR vs Frequency/Attenuation LTE 5 MHz TM1.1

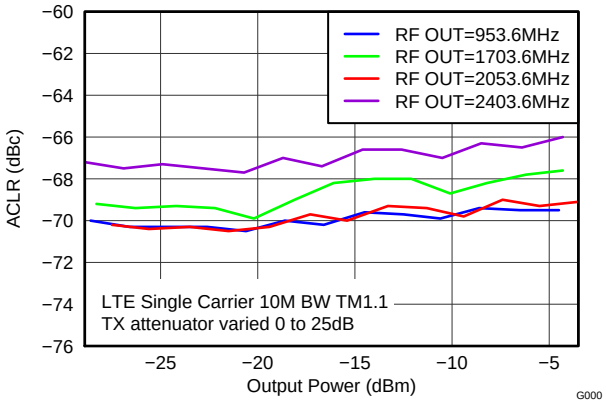

Figure 54. Tx ACLR vs Frequency/Attenuation LTE 10 MHz TM1.1

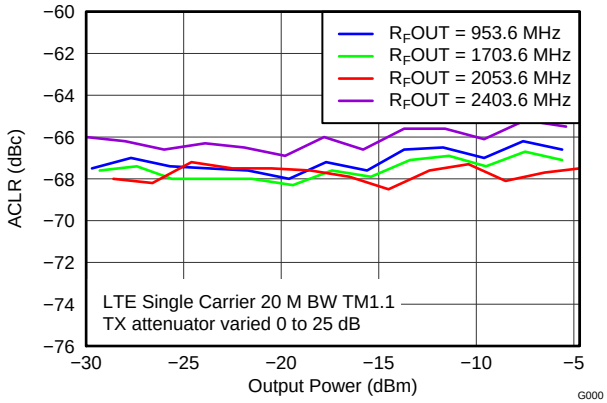

Figure 55. Tx ACLR vs Frequency/Attenuation LTE 20 MHz TM1.1

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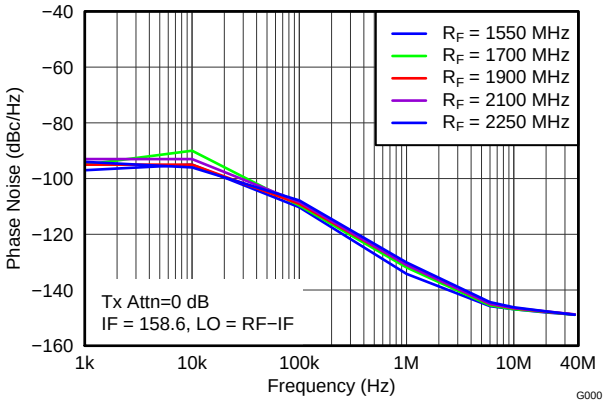

Figure 56. Tx Output Phase Noise vs Frequency Minimum Attenuation

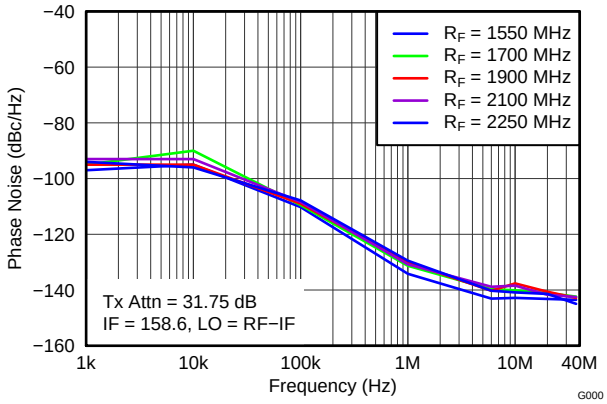

Figure 57. Tx Output Phase Noise vs Frequency Maximum Attenuation

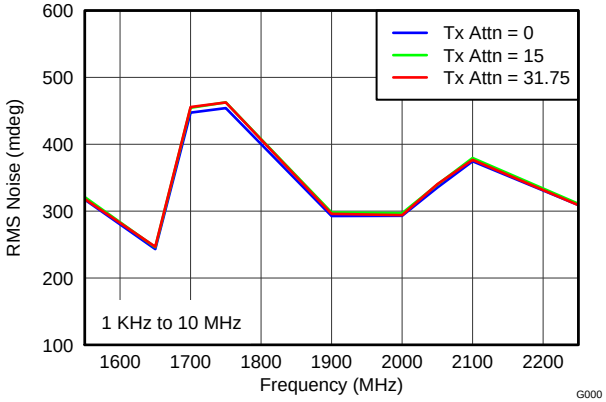

Figure 58. Tx Output Noise vs Frequency

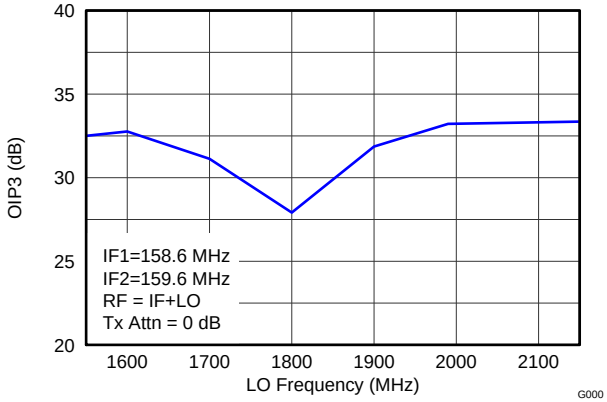

Figure 59. Tx OIP3 vs LO Frequency

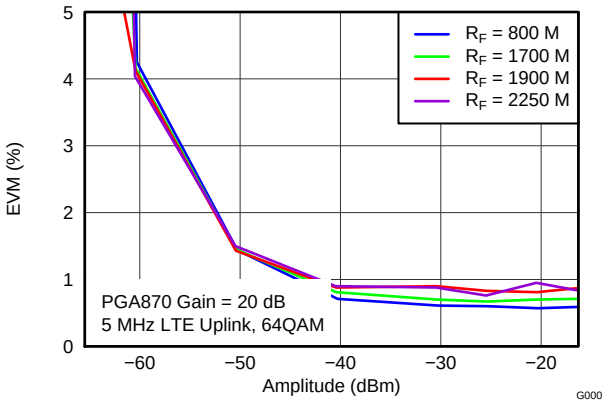

Figure 60. Rx EVM vs Frequency/RF Input Amplitude LTE 5-MHz Uplink, 64 QAM

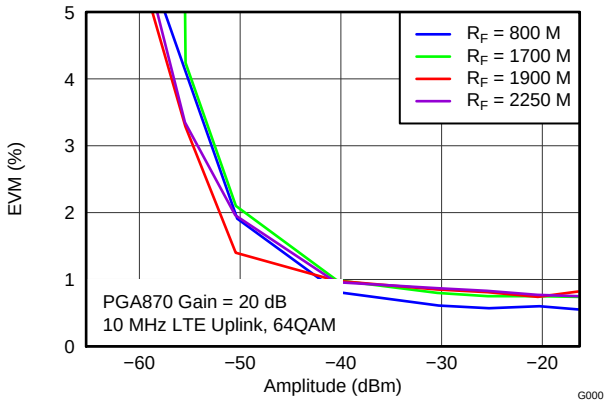

Figure 61. Rx EVM vs Frequency/RF Input Amplitude LTE 10-MHz Uplink, 64 QAM

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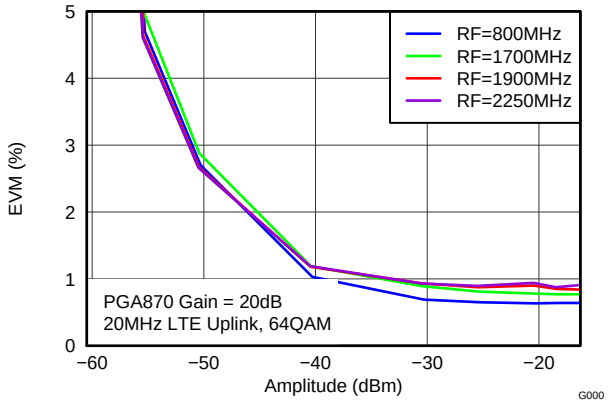

Figure 62. Rx EVM vs Frequency/RF Input Amplitude LTE 20-MHz Uplink, 64 QAM

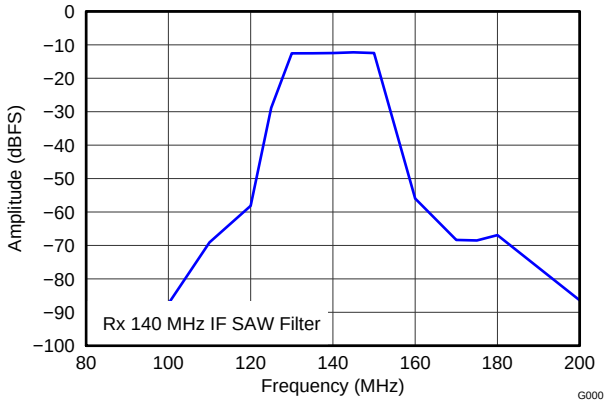

Figure 63. Rx IF Filter Response

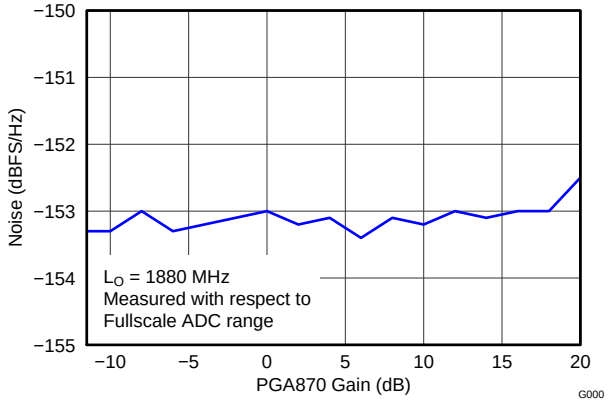

Figure 64. Rx Idle Channel Noise vs PGA870 Gain Setting

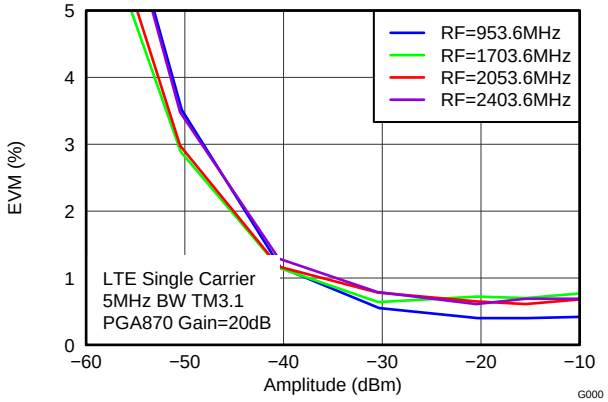

Figure 65. FB EVM vs Input Amplitude/Frequency LTE 5 MHz TM3.1

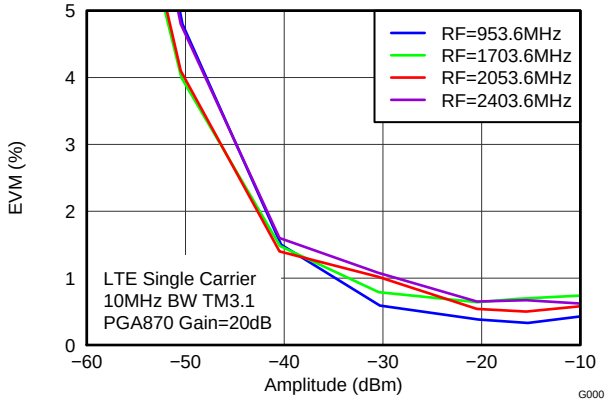

Figure 66. FB EVM vs Input Amplitude/Frequency LTE 10 MHz TM3.1

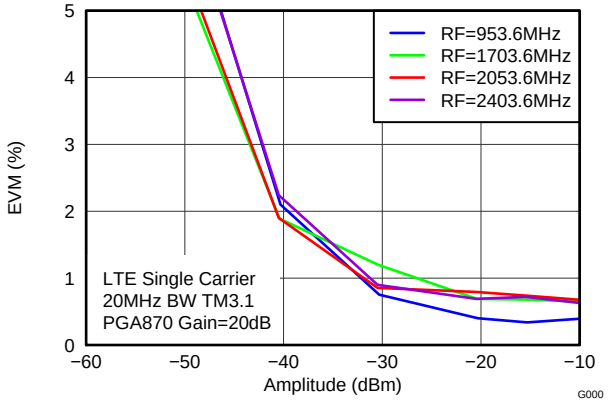

Figure 67. FB EVM vs Input Amplitude/Frequency LTE 20 MHz TM3.1

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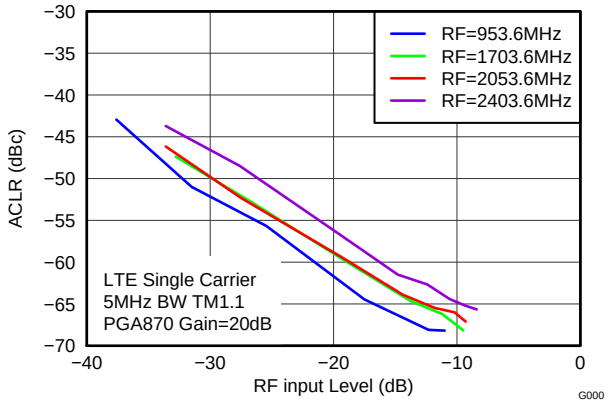

Figure 68. FB ACLR vs Input Amplitude/Frequency LTE 5 MHz TM1.1

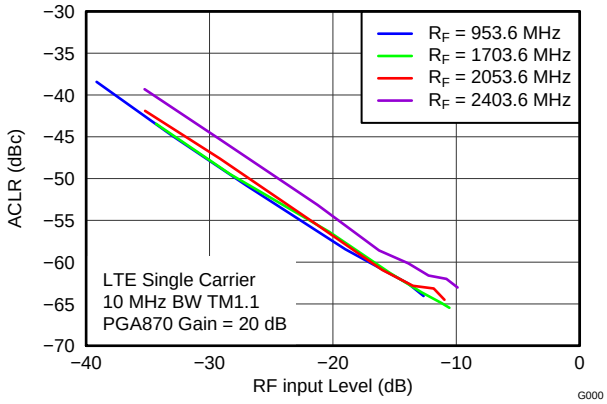

Figure 69. FB ACLR vs Input Amplitude/Frequency LTE 10 MHz TM1.1

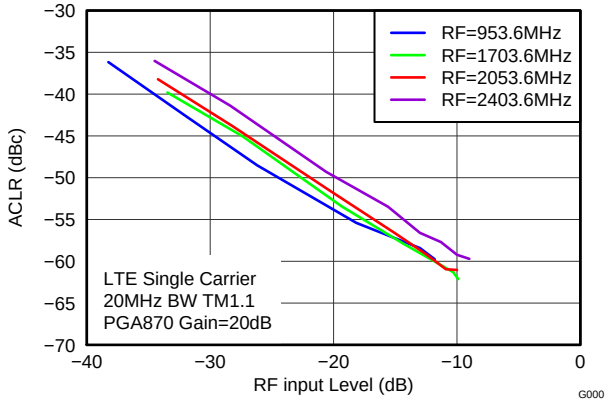

Figure 70. FB ACLR vs Input Amplitude/Frequency LTE 20 MHz TM1.1

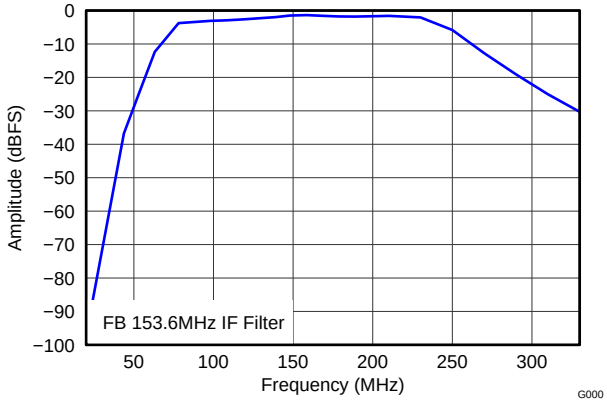

Figure 71. FB IF Filter Response

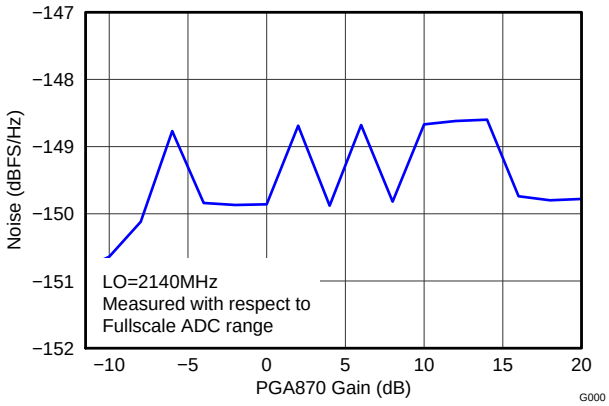

Figure 72. FB Idle Channel Noise

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10 Programming Information

In Stand-Alone mode the TSW3725 GUI handles all the serial interface programming. However, as a debug or development aid, the following information is provided.

The following table lists the device ids required to access the serial interface of given device.

Device ID [xxxx]	Device P/N	Schematic Designator	Description	Comment
1	DAC3484	U1	TX quad DAC	
2	ADS4149	U17	FB ADC	
3	ADS4249	U13	Dual RX ADC	
4	TRF3720-1	U27	TX and FB LO	
5	TRF3720-2	U31	RX LO	
6	PGA870 - RX1	U40	RX path 1	
7	PGA870 - RX2	U43	RX path 2	
8	PGA870 - FB	U50	FB feedback	
9	PE43701 - TX_1	U9	TX path 1	
10	PE43701 - TX_2	U12	TX path 2	
11	CDCE72010	U23	clock	
14	MISC		FB SWITCH and PGA PWDN BITS	D0: HIGH D1: FB SWITCH: CTRL1_PE4257 D2: FB SWITCH: CTRL2_PE4257 D3: RX1 PGA870 PWDN BIT D4: RX2 PGA870 PWDN BIT D5: FB PGA870 PWDN BIT

The following table lists the bit sequence that the TSW3725 expects to receive from the SCBP board

MSB-->LSB																															
Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC3484	NA								Address								Data															
									7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADS4149	NA																Address								Data							
																	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
ADS4249	NA																Address								Data							
																	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TRF3720	Address					Data																										
	0	1	2	3	4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
PGA870	NA																										Gain Bits					
																											5	4	3	2	1	0
PE43701	NA																Data								Address							
																	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
CDCE72010	Address				Data																											
	0	1	2	3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
RESERVED	NA																										Data					
																											5	4	3	2	1	0

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5.5 V to 6.25 V and the output voltage range of 0 V to 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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