



ABSTRACT

The *TPSM5601R5EVM* features the *TPSM5601R5* synchronous-buck power module and the *TPSM5601R5SEVM* features the *TPSM5601R5S* synchronous-buck power module which offers frequency spread-spectrum operation. Both EVMs are configured for operation with typical 4.2-V to 60-V input bus applications. The output voltage is set to one of five popular values by using a configuration jumper. The EVM supplies the full output current rating of the device. Input and output capacitors are included to accommodate the entire range of input voltage and the selectable output voltages on the EVM. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points and jumpers are provided for use of the enable (EN) and power-good (PGOOD) features of the device. The recommended PCB layout of the EVM maximizes thermal performance and minimizes output ripple and noise.

Table of Contents

1 EVM Setup	2
2 EVM Connectors and Test Points	4
3 Test Results	5
4 PCB Layouts	6
5 Schematics	9
6 Bill of Materials	10
7 Revision History	10

List of Figures

Figure 1-1. EVM User Interface.....	2
Figure 3-1. ENABLE Start-Up Waveform.....	5
Figure 3-2. ENABLE Shutdown Waveform.....	5
Figure 3-3. Output Voltage Ripple.....	5
Figure 3-4. Transient Performance.....	5
Figure 4-1. Top Silk Screen (Top View).....	6
Figure 4-2. Top Copper Layer.....	6
Figure 4-3. Signal Layer 1.....	7
Figure 4-4. Signal Layer 2.....	7
Figure 4-5. Bottom Layer.....	8
Figure 4-6. Bottom Layer Silk Screen (Bottom View).....	8
Figure 5-1. <i>TPSM5601R5EVM</i> Schematic.....	9

List of Tables

Table 2-1. Test Point Descriptions.....	4
Table 6-1. <i>TPSM5601R5EVM</i> BOM.....	10

Trademarks

All trademarks are the property of their respective owners.

1 EVM Setup

Note

This EVM user's guide applies to both devices, TPSM5601R5 and TPSM5601R5S. The only difference between the two EVMs are the U1 IC and the silk screen labeling.

Figure 1-1 highlights the user interface items associated with the EVM. The *VIN* Power terminal block (J1) is used for connection to the host input supply and the *VOUT* Power terminal block (J4) is used for connection to the load. These terminal blocks accept up to 16-AWG wire.

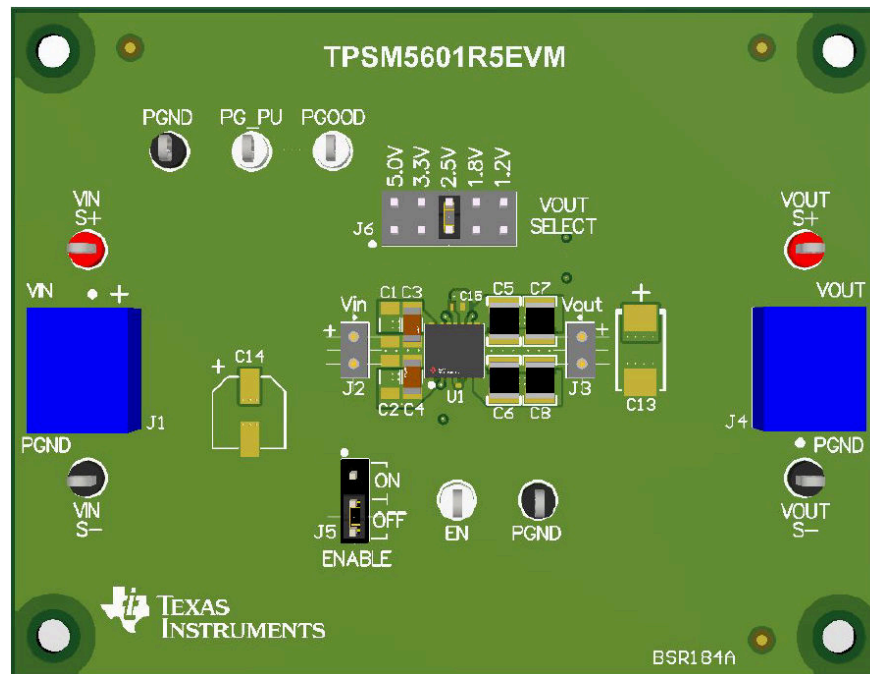


Figure 1-1. EVM User Interface

- Use the VIN S+ and VIN S– test points along with the VOUT S+ and VOUT S– test points located near the power terminal blocks as voltage monitoring points where voltmeters can be connected to measure VIN and VOUT. *Do not use these S+ and S– monitoring test points as the input supply or output load connection points.* The PCB traces connecting to these test points are not designed to support high currents.
- Use the VIN scope (J2) and VOUT scope (J3) test points to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended to use un-hooded scope probes outfitted with a low inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1-in centers. Connect the scope probe tip to the top socket labeled "+" and connect the scope ground lead to the bottom socket.
- The control test points located near the bottom of the EVM test the features of the device. Refer to [Section 2](#) for more information on the individual control test points.
- The VOUT SELECT jumper (J6) is provided to select the desired output voltage:
 - 1.2 V
 - 1.8 V
 - 2.5 V
 - 3.3 V
 - 5.0 V

Before applying power to the EVM, make sure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.

- The device can be turned on or off using the enable jumper (J5). Place the jumper in the ON position to enable the device. Place the jumper in the OFF position to disable the device. The undervoltage lockout (UVLO) can be set by populating resistors R1 and R2 located on the bottom side of the EVM. Refer to the data sheet for recommended UVLO resistor values. The power good (PGOOD) test point is available

to monitor when a valid output voltage is present on the EVM. Additionally, the PG_PU pin is present as a convenient point to connect a pullup voltage for the PGOOD signal.

2 EVM Connectors and Test Points

Wire-loop test points and scope probe sockets are included for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. [Table 2-1](#) ⁽¹⁾ describes each test point.

Table 2-1. Test Point Descriptions

TEST POINT	DESCRIPTION
VIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
VIN S–	Input ground monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
VOUT S+	Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
VOUT S–	Output ground monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
PGND	Power ground test points
VIN Scope (J2)	Input voltage scope monitor. Connect an oscilloscope probe to this set of points to measure input ripple voltage.
VOUT Scope (J3)	Output voltage scope monitor. Connect an oscilloscope probe to this set of points to measure output voltage ripple and transient response.
EN (VIN)	Enable test point. EN test point is connected to VIN. Do not connect this test point to ground or any other signal. Use the ENABLE Control header (J5) to disable the device. To monitor the enable signal, monitor pin 2 of header J5.
ENABLE Control (J5)	Enable select jumper. Enable or disable the device using a jumper.
PGOOD	Power good test point. Monitors the power-good signal of the device. This is an open-drain signal. A 49.9-kΩ resistor is connected to this pin and the PG_PU pin on the EVM.
PG_PU	PGOOD pullup test point. Apply a voltage to this pin to use as a pullup voltage for the PGOOD signal. A 49.9-kΩ resistor is connected to this pin and the PGOOD pin on the EVM.

(1) Refer to the product data sheet for absolute maximum ratings associated with the features in this table.

3 Test Results

Figure 3-1 through Figure 3-4 demonstrate the performance of the TPSM5601R5EVM under the following condition of a 24-V input voltage, 5-V output voltage, and 1-A load.

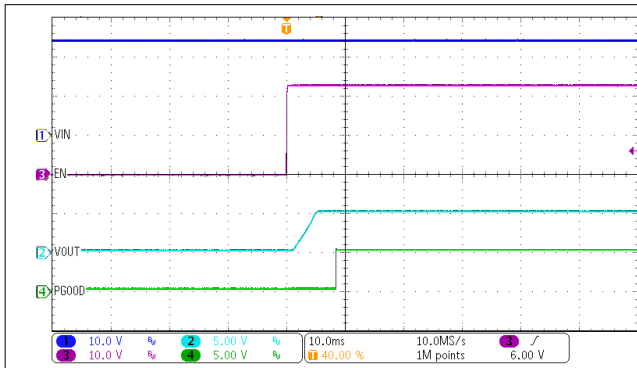


Figure 3-1. ENABLE Start-Up Waveform

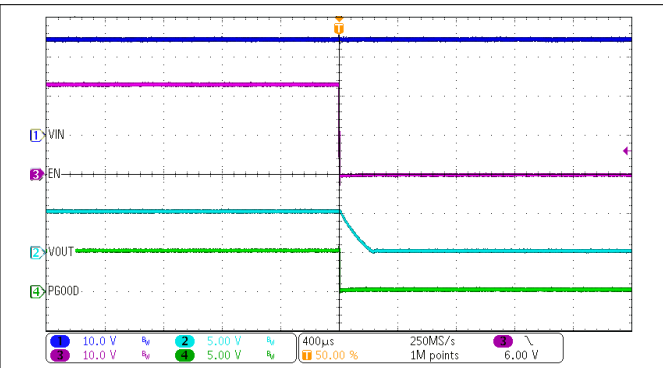


Figure 3-2. ENABLE Shutdown Waveform

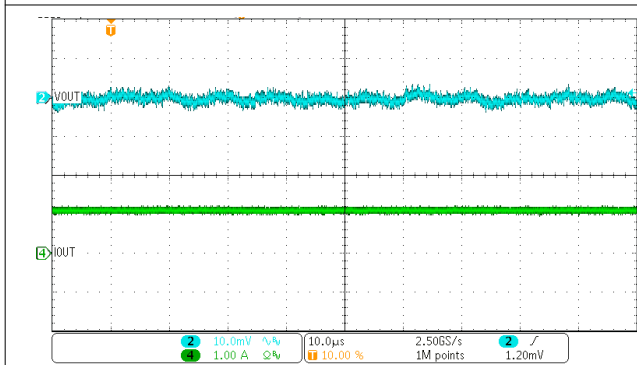


Figure 3-3. Output Voltage Ripple

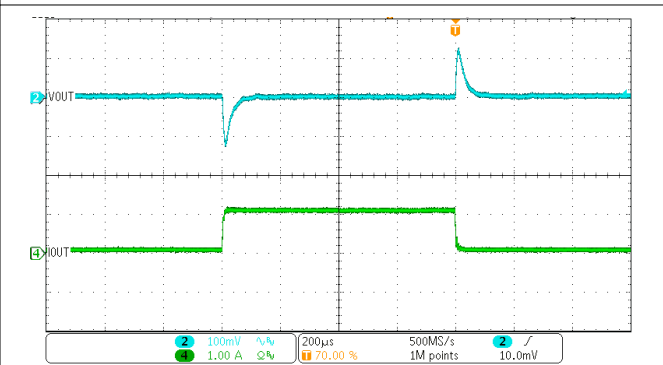


Figure 3-4. Transient Performance

4 PCB Layouts

Figure 4-1 through Figure 4-6 show the EVM PCB layout images.

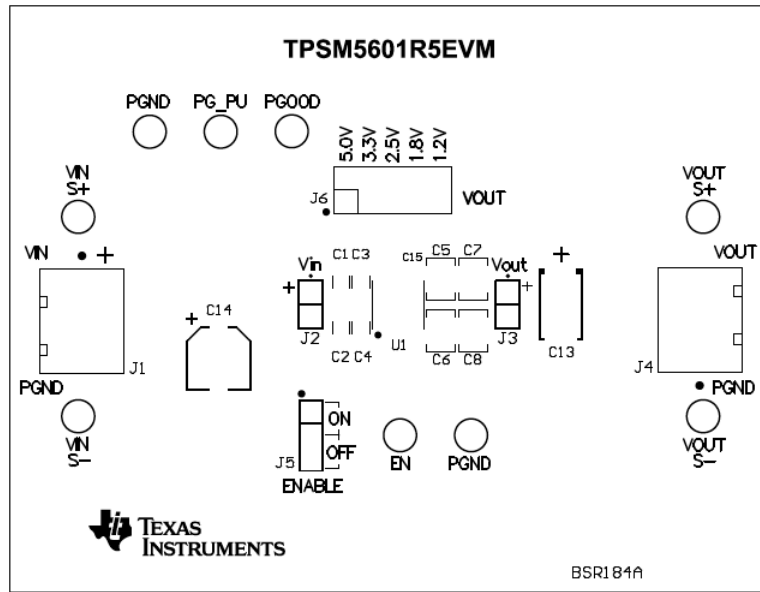


Figure 4-1. Top Silk Screen (Top View)

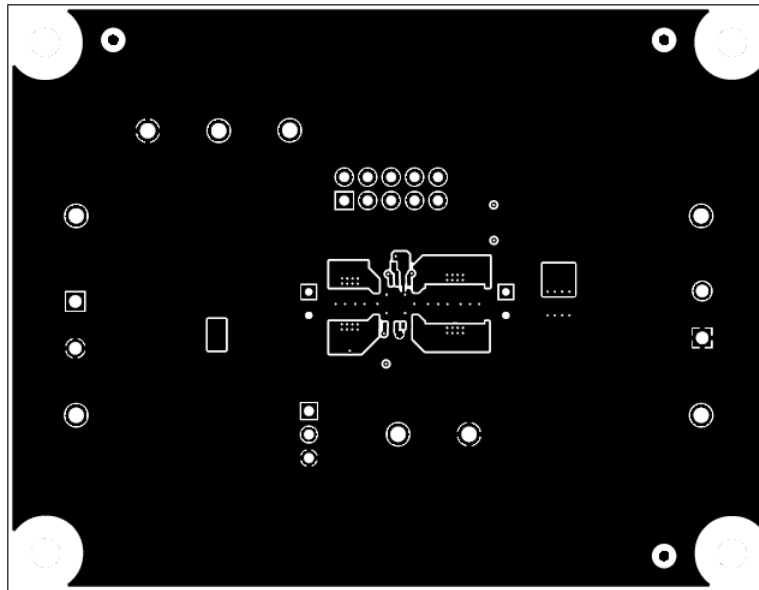


Figure 4-2. Top Copper Layer

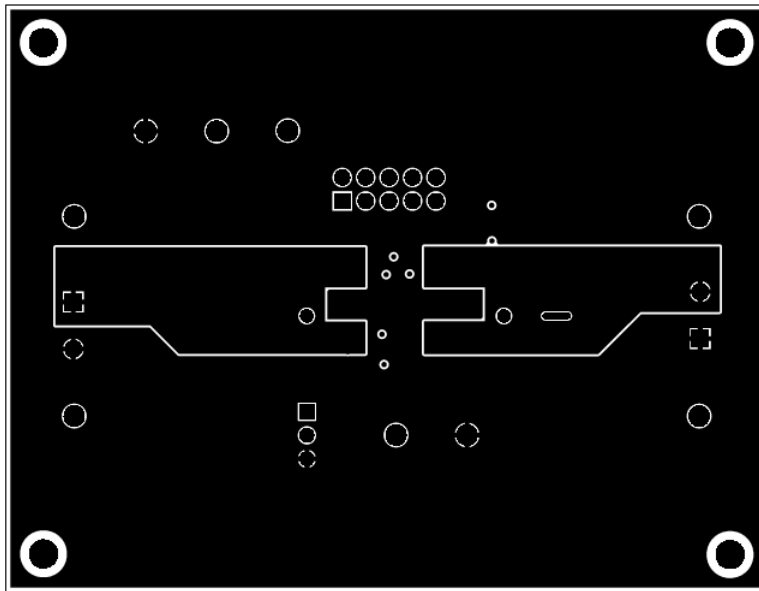


Figure 4-3. Signal Layer 1

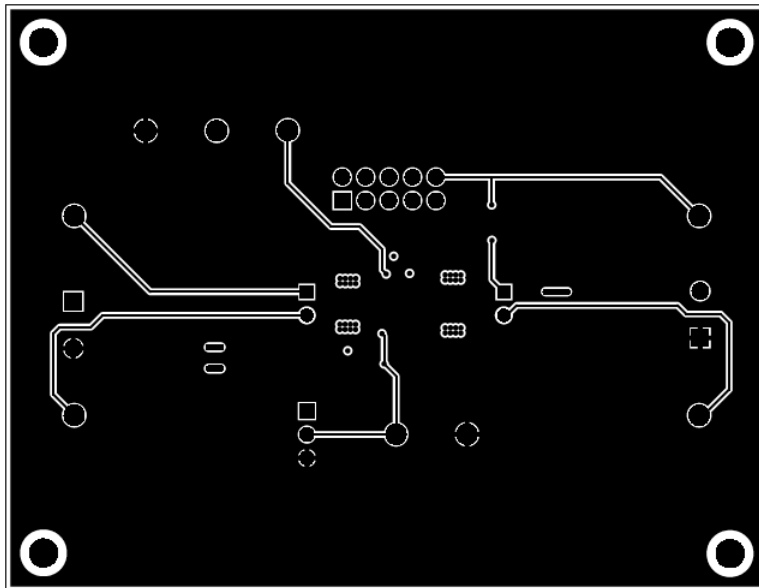


Figure 4-4. Signal Layer 2

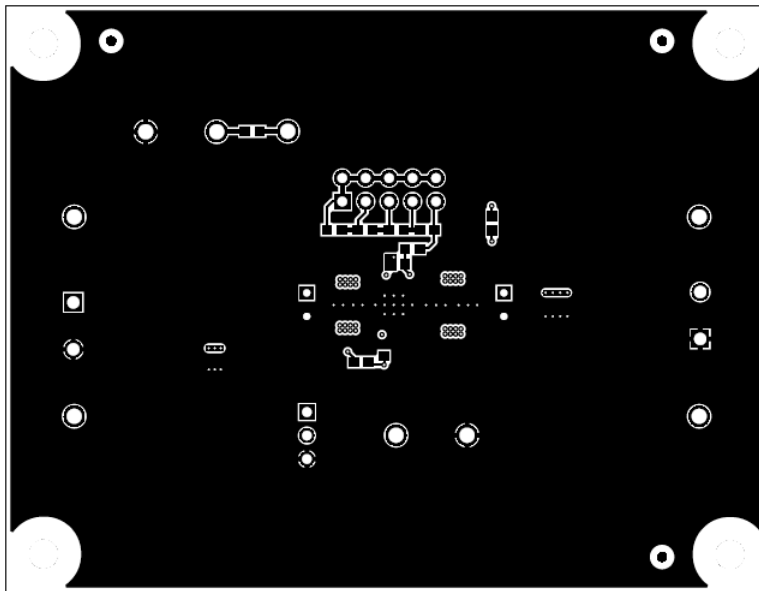


Figure 4-5. Bottom Layer

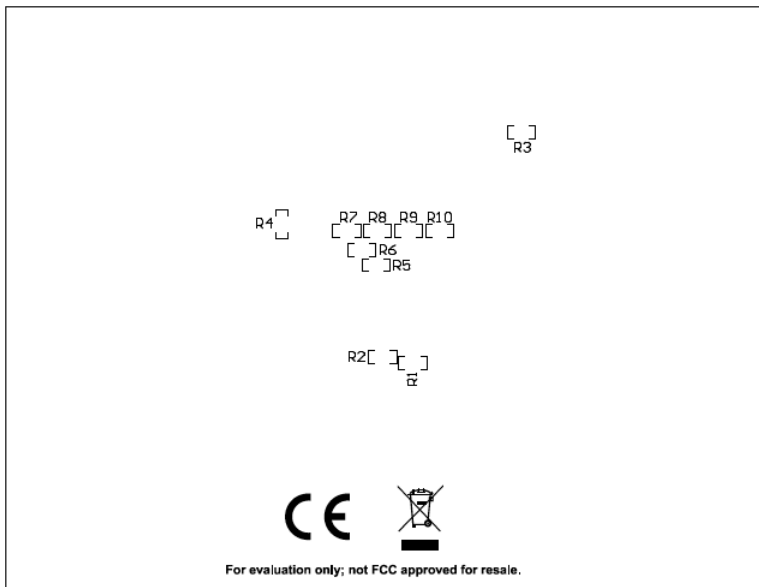


Figure 4-6. Bottom Layer Silk Screen (Bottom View)

5 Schematics

The schematic for both the TPSM5601R5EVM and TPSM5601R5SEVM are identical with the only difference being the U1 IC. Figure 5-1 illustrates the TPSM5601R5EVM schematic with the device (U1) populated by TPSM5601R5.

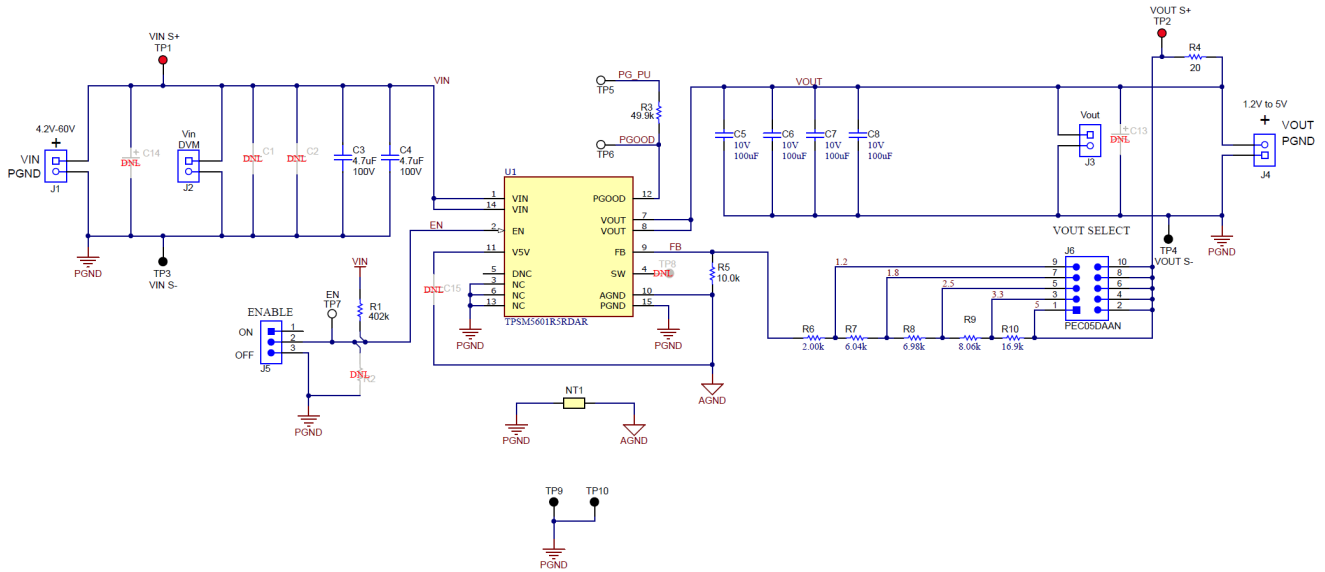


Figure 5-1. TPSM5601R5EVM Schematic

6 Bill of Materials

Table 6-1 lists the TPSM5601R5EVM or TPSM5601R5SEVM bill of materials (BOM).

Table 6-1. TPSM5601R5EVM BOM

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER
C3, C4	2	4.7 μ F	CAP, CERM, 4.7 μ F, 100 V, X7S	1206	GRM31CC72A475KE11L
C5, C6, C7, C8	4	100 μ F	CAP, CERM, 100 μ F, 10 V, X5R	1210	GRM32ER61A107ME20L
J1, J4	2		Terminal Block, 2 \times 1, 5.08 mm	2 \times 1	OSTTA024163
J2, J3	2		Socket Strip, 2 \times 1, 100 mil	100 mil, 2 pin	310-43-102-41-001000
J5	1		Header, 100 mil, 3 \times 1	3 pin, 100 mil	PEC03SAAN
J6	1		Header, 100 mil, 5 \times 2	5 \times 2, 100 mil	PEC05DAAN
R1	1	402 k	RES, 402 k, 1%, 0.1 W	0603	CRCW0603402KFKEA
R3	1	49.9 k	RES, 49.9 k, 1%, 0.1 W	0603	CRCW060349K9FKEA
R4	1	20	RES, 20, 5%, 0.1 W	0603	CRCW060320R0JNEA
R5	1	10.0 k	RES, 10.0 k, 1%, 0.1 W	0603	CRCW060310K0FKEA
R6	1	2.00 k	RES, 2.0 k, 1%, 0.1 W	0603	RC0603FR-072KL
R7	1	6.04 k	RES, 6.04 k, 1%, 0.1 W	0603	RC0603FR-076K04L
R8	1	6.98 k	RES, 6.98 k, 1%, 0.1 W	0603	RC0603FR-076K98L
R9	1	8.06 k	RES, 8.06 k, 1%, 0.1 W	0603	CRCW06038K06FKEA
R10	1	16.9 k	RES, 16.9 k, 1%, 0.1 W	0603	RC0603FR-0716K9L
TP1, TP2	2		Test Point, Multipurpose, Red		5010
TP3, TP4, TP9, TP10	4		Test Point, Multipurpose, Black		5011
TP5, TP6, TP7	3		Test Point, Multipurpose, White		5012
U1	1		60-V input, 1-V to 6-V output, 1.5-A Power Module	B3QFN	TPSM5601R5
			60-V input, 1-V to 6-V output, 1.5-A Power Module with Spread Spectrum operation		TPSM5601R5S
C1, C2	0			1206	
C13	0			7343-40	
C14	0			6.3 \times 5.8 mm	
C15	0			0402	
R2	0			0603	

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (August 2021)	Page
• Added the TPSM5601R5SEVM.....	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated