TPS6381xEVM

This user's guide describes the operation and use of the TPS6381xEVM evaluation module (EVM). The EVM is designed to help users easily evaluate and test the operation and functionality of the TPS6381x buck-boost converter family. The EVM has the output voltage set to 3.3 V or 3.45 V, depending on jumper setting. The output voltage can be programmed via I^2C interface between 1.8 V and 5.2 V. The EVM operates with an input voltage between 2.2 V and 5.5 V. The output current can go up to 2.5 A in buck mode and up to 2 A in boost mode. This document includes setup instructions for the hardware, together with the schematic and the PCB layout of the EVM. Throughout this document, the abbreviations EVM, TPS6381xEVM, and the term evaluation module are synonymous with the TPS6381x, unless otherwise noted.

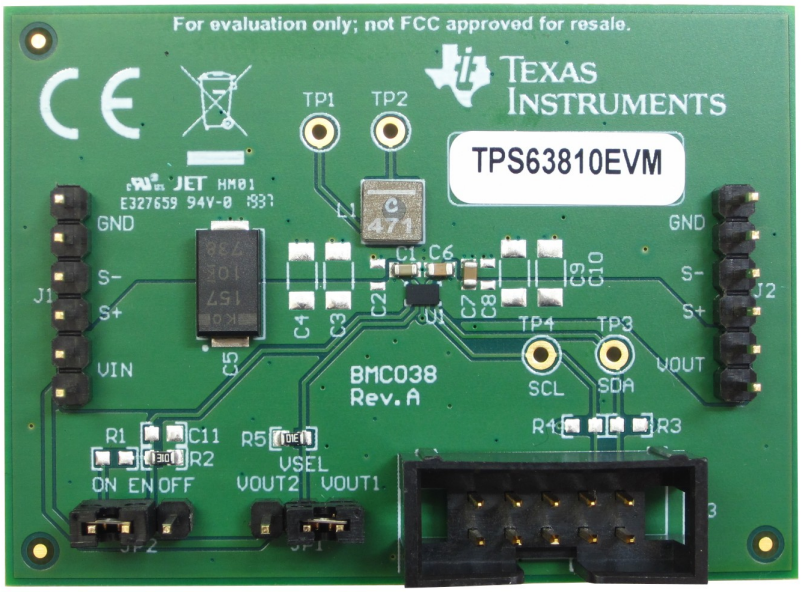

Figure 1. TPS6381xEVM

Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The Texas Instruments TPS6381x is a highly efficient, single-inductor, internally compensated buck-boost converter in a 15-pin, 2.3-mm × 1.4-mm WCSP package. The output voltage can be selected between two I^2C-programmable values in the range from 1.8 V to 5.2 V in 25-mV steps. There are two versions of the EVM, depending on the device being used:

- TPS63810EVM uses the TPS63810, in which the power-up value of the ENABLE bit is 1.
- TPS63811EVM uses the TPS63811, in which the power-up value of the ENABLE bit is 0.

The ENABLE bit in the control register controls the output state of the power stage. See Section 6 for more details.

1.1 Background

The TPS6381xEVM uses the TPS6381x integrated circuit (IC) , and is set to 3.3 V or 3.45 V output voltage, depending on jumper setting. The EVM operates with an input voltage between 2.2 V and 5.5 V.

1.2 Performance Specification

Table 1 provides a summary of the TPS6381xEVM performance specifications. All specifications are given for ambient temperature of 25°C.

Table 1. Performance Specification Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		2.2		5.5	V
Output voltage		1.8		5.2	V
Output current	$V_{IN} \geq 2.5$ V, $V_{OUT} = 3.3$ V			2.5	A

1.3 Modifications

The printed-circuit board (PCB) for the EVM is designed to accommodate the TPS6381x. Extra positions are available for additional input and output capacitors, EN pin voltage divider, and I^2C pullup resistors.

1.3.1 IC U1 Operation

This EVM requires an appropriate I^2C interface, such as the TI USB2ANY, to reconfigure the TPS6381x. The output voltage can be chosen between two I^2C-programmable values by using an on-board jumper. See Section 6 for the available output voltage values.

2 Setup

This section describes how to properly use the TPS6381xEVM.

2.1 Input and Output Connectors, Test Points, and Headers Description

2.1.1 J1, Pin 1 and 2 – VIN

Positive input voltage connection from the input power supply for the EVM.

2.1.2 J1, Pin 3 and 4 – S+/S-

Input voltage sense connections. Measure the input voltage at this point.

2.1.3 J1, Pin 5 and 6 – GND

Input voltage GND return connection from the input power supply for the EVM, common with J2 GND connection

2.1.4 J2, Pin 1 and 2 – VOUT

Positive output voltage connection

2.1.5 J2, Pin 3 and 4 – S+/S-

Output voltage sense connections. Measure the output voltage at this point.

2.1.6 J2, Pin 5 and 6 – GND

Output voltage GND return connection, common with J1 GND connection

2.1.7 TP1, TP2 – L1, L2

Test points connected to L1 and L2 switch node pins of the TPS6381x

2.1.8 TP3, TP4 – GND

Test points connected to SDA and SCL pins of the TPS6381x

2.1.9 J3 – I2C

10-pin header used to connect the USB2ANY adaptor to the EVM

2.1.10 JP1 – VSEL

Placing a jumper across VSEL and VOUT1 pins sets the output voltage to the value in VOUT1 register. Placing a jumper across VSEL and VOUT2 pins sets the output voltage to the value in VOUT2 register.

2.1.11 JP2 – ENABLE

Placing a jumper across pins EN and ON enables the device. Placing a jumper across pins EN and OFF disables the device.

2.2 Setup

To operate the EVM, connect a power supply with the positive lead to J1 VIN pins and the negative lead to J1 GND pins. Connect a load with the positive lead to J2 VOUT pins and the negative lead to J2 GND pins. Place a jumper across VSEL and VOUT1 or VOUT2 pins on JP1 to select the corresponding output voltage register. Place a jumper across EN and ON pins on JP2 to enable the device.

3 Board Layout

This section provides the TPS6381xEVM board layout and illustrations.

3.1 Layout

Figure 2 through Figure 6 show the component placement and PCB layout of the TPS6381xEVM.

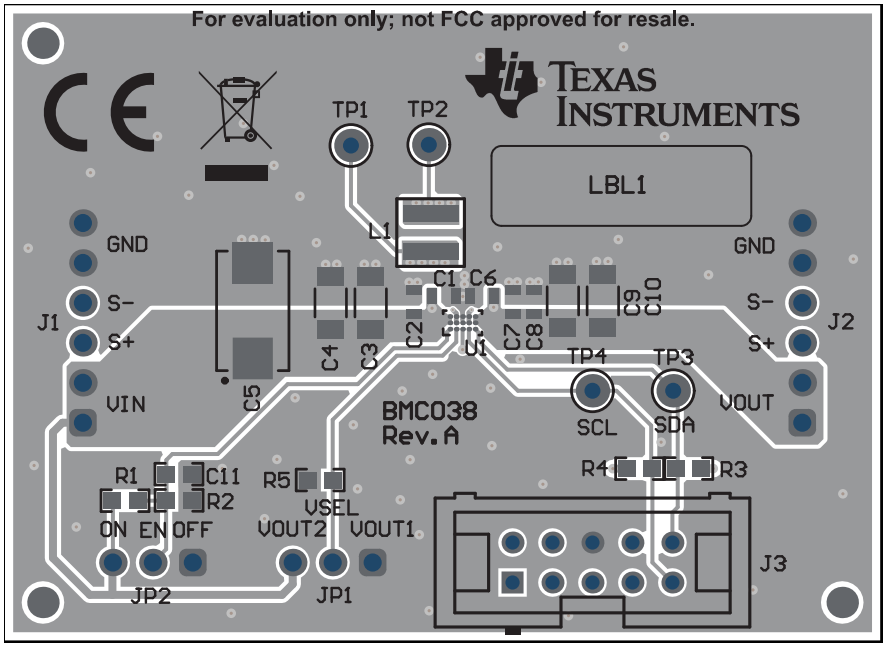

Figure 2. TPS6381xEVM PCB - Assembly Layer

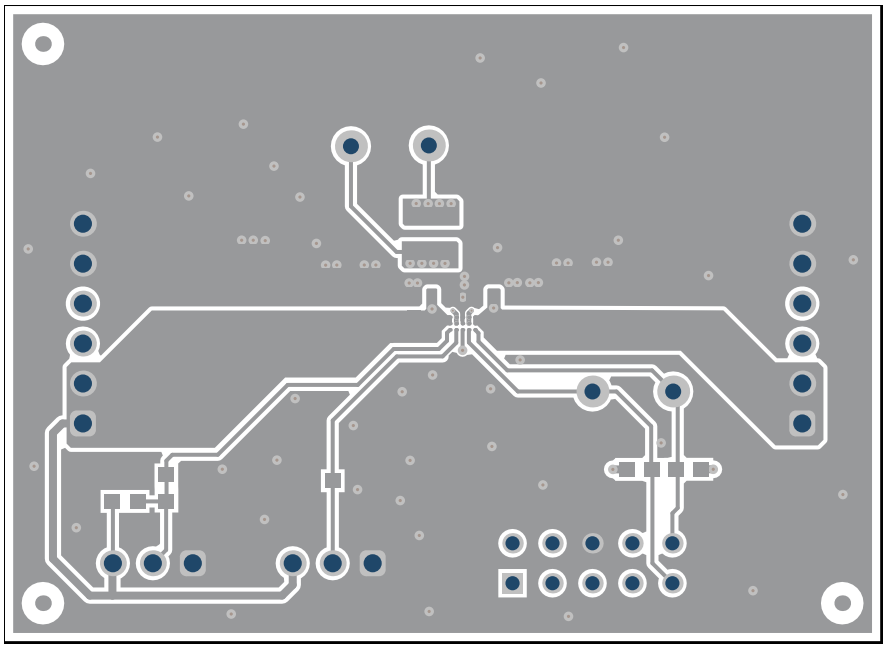

Figure 3. TPS6381xEVM PCB - Top Layer

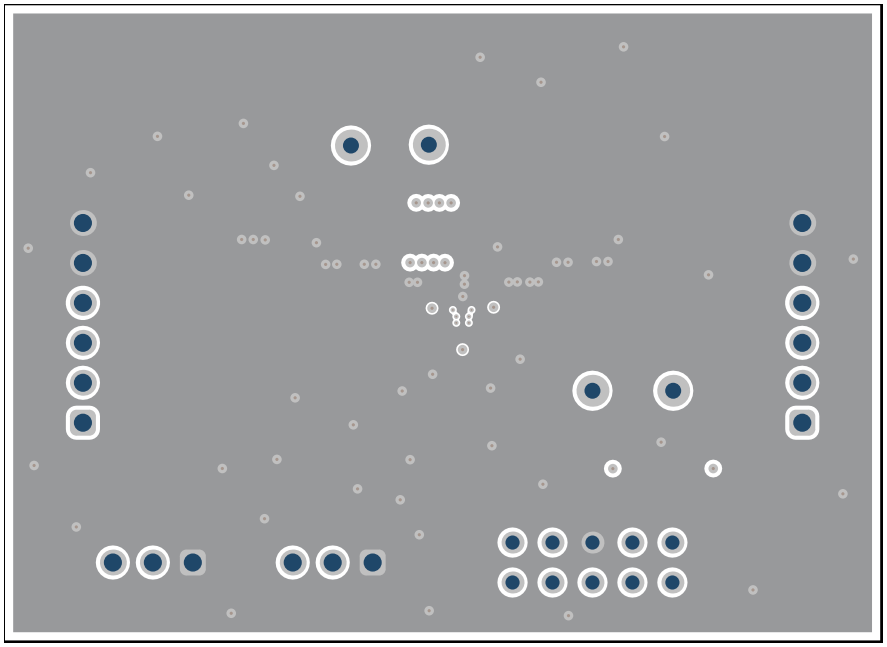

Figure 4. TPS6381xEVM PCB - Signal Layer 1 (Top View)

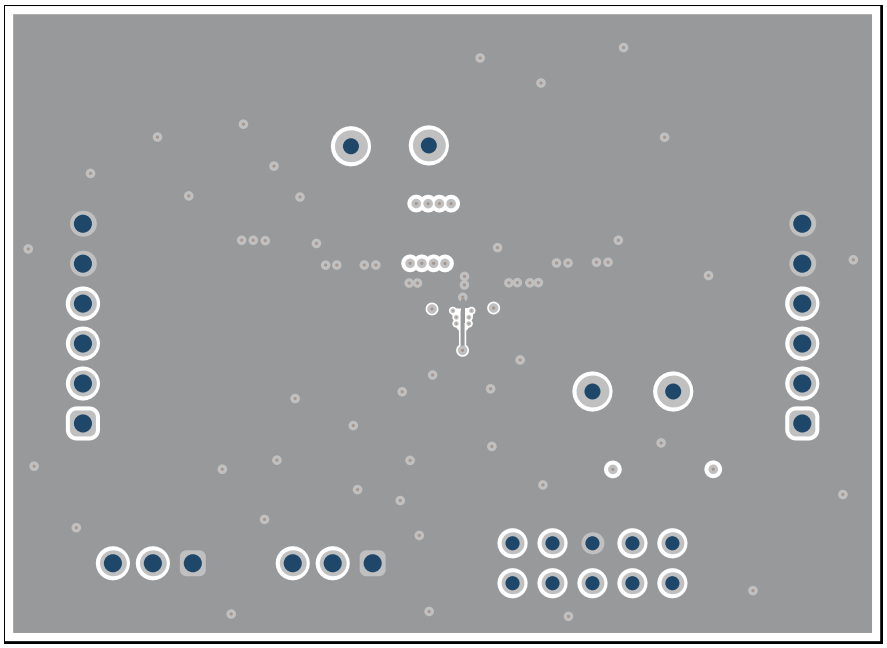

Figure 5. TPS6381xEVM PCB - Signal Layer 2 (Top View)

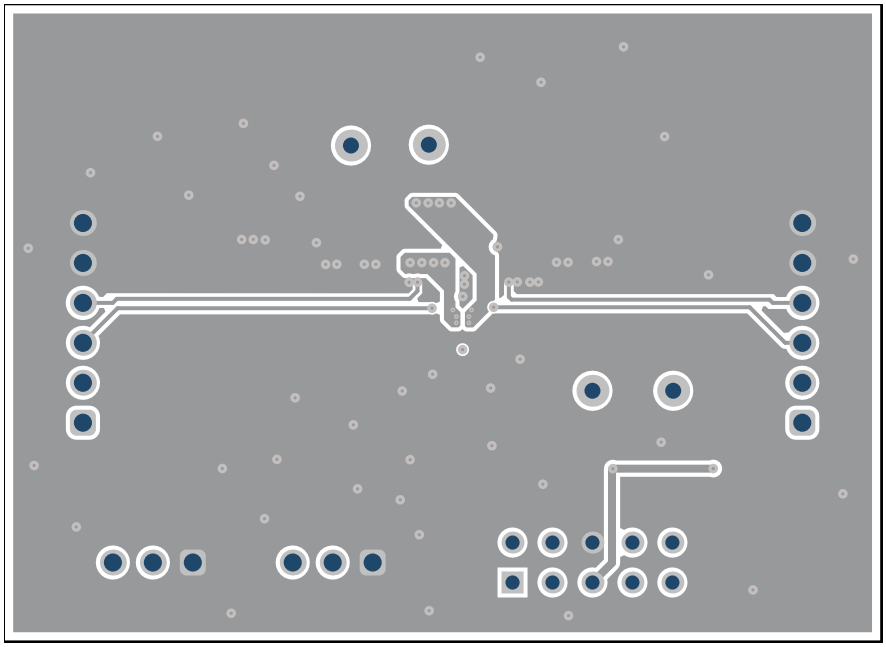

Figure 6. TPS6381xEVM PCB - Bottom Layer (Top View)

4 Schematic and Bill of Materials

This section provides the TPS6381xEVM schematic and bill of materials.

4.1 Schematic

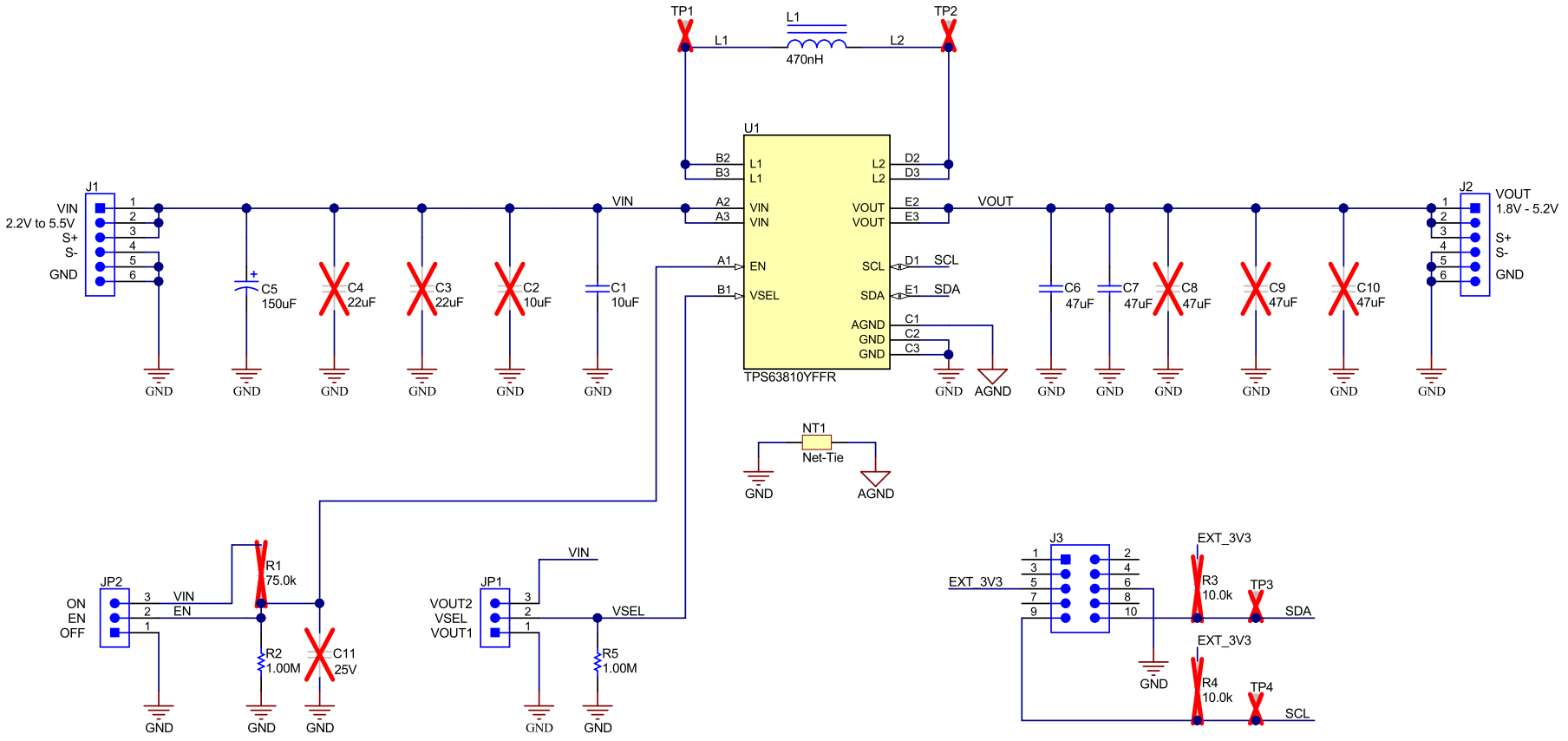

Figure 7. TPS6381xEVM Schematic

4.2 Bill of Materials

Table 2. TPS63810EVM Bill of Materials

QTY	DESIGNATOR	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
1	C1	10 µF	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J106ME84	Murata
1	C5	150 µF	CAP, TA, 150 µF, 10 V, ±20%, 0.005 Ω	7343-31	T530D157M010ATE005	Kemet
2	C6, C7	47 µF	CAP, CERM, 47 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J476ME15D	Murata
1	L1	470 nH	Inductor, Shielded, Composite, 470 nH, 3.5A, 7.6 mΩ	4x4x1.5 mm	XFL4015-471MEC	Coilcraft
1	R2, R5	1.00 MΩ	RES, 1.00 M, 1%, 0.1 W, 0603	0603	CRCW06031M00FKEA	Vishay-Dale
1	U1	N/A	IC, Single Inductor Buck-Boost Converter	2.3x1.4x1 mm	TPS63810YFFR	TI

Table 3. TPS63811EVM Bill of Materials

QTY	DESIGNATOR	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
1	C1	10 µF	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J106ME84	Murata
1	C5	150 µF	CAP, TA, 150 µF, 10 V, 20%, 0.005 Ω	7343-31	T530D157M010ATE005	Kemet
2	C6, C7	47 µF	CAP, CERM, 47 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J476ME15D	Murata
1	L1	470 nH	Inductor, Shielded, Composite, 470 nH, 3.5 A, 7.6 mΩ	4x4x1.5 mm	XFL4015-471MEC	Coilcraft
1	R2, R5	1.00 MΩ	RES, 1.00 M, 1%, 0.1 W, 0603	0603	CRCW06031M00FKEA	Vishay-Dale
1	U1	N/A	IC, Single Inductor Buck-Boost Converter	2.3x1.4x1 mm	TPS63811YFFR	TI

5 Software User Interface

5.1 Software Setup

A graphical user interface (GUI) is available from ti.com website (*http://www.ti.com/product/TPS63810/toolssoftware*) which allows simple and convenient programming of the device through the TI USB2ANY (*http://www.ti.com/tool/USB2ANY*) device. Alternatively, the user can use any I^2C-standardized programming tool or I^2C host to configure the device. Mind the I^2C pins specification, such as timing parameters and proper pullup resistors, provided with the *High Current, High Efficiency Single Inductor Buck-Boost Converter Data Sheet*.

5.2 Interface Hardware Setup

Connect the USB2ANY adapter to your PC using the supplied USB cable. Connect the EVM connector J3 to the USB2ANY adapter using the supplied 10-pin ribbon cable. The connectors on the ribbon cable are keyed to prevent incorrect installation.

Figure 8 shows a quick adapter connection overview.

USB Interface Adaptor Quick Connection Diagram

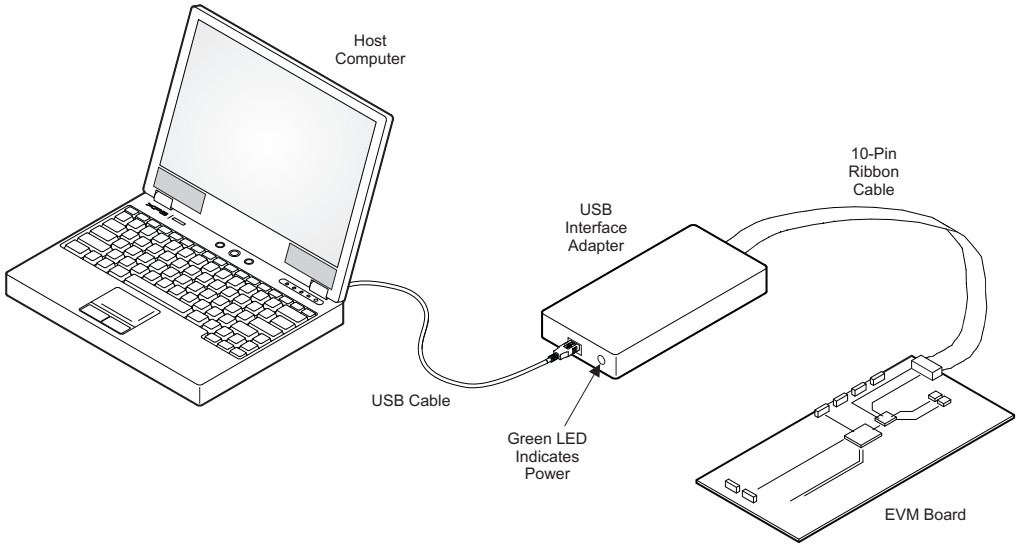

Figure 8. Quick Connection Overview

5.3 User Interface Operation

Upon startup, the GUI automatically connects to the EVM. If not, click on the Connect button in the lower left corner of the GUI window. The following sections give short overview of the three main GUI screens.

5.3.1 Home Screen

The Home screen gives a short overview of the TPS6381x devices. To start evaluating the device, click on the Start button or on the Settings or Register Map icons on the left side of the GUI window.

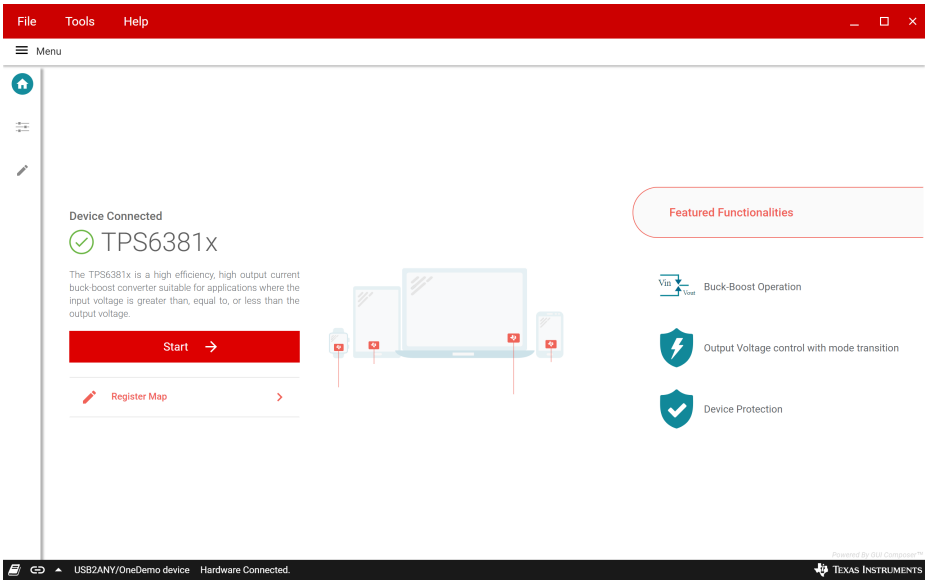

Figure 9. GUI Home Screen

5.3.2 Settings Screen

The Settings screen provides control over the output voltage and operating modes of the TPS6381x.

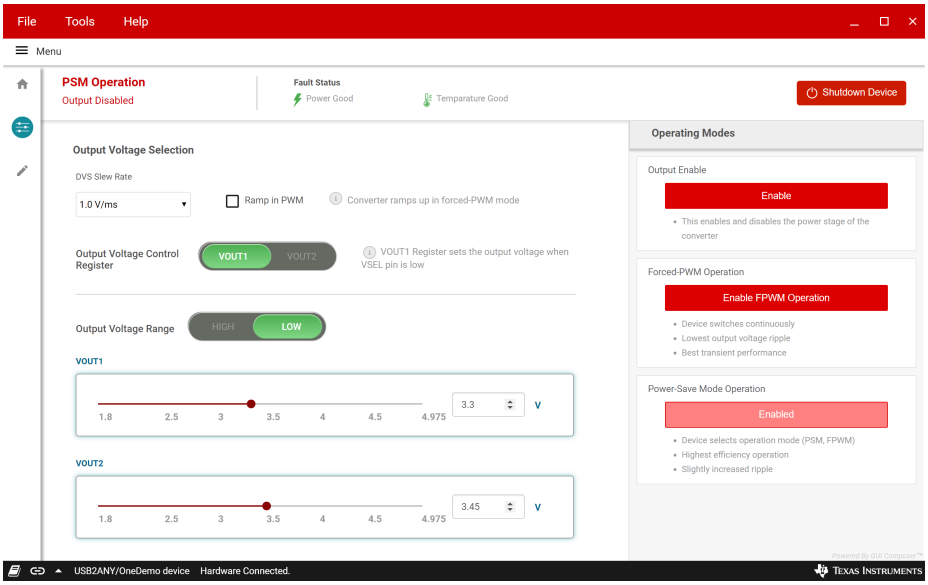

Figure 10. GUI Settings Screen

5.3.3 Register Map Screen

The Register Map screen shows a register-wise view of all parameters. Here, single registers can be read or written to the device (if applicable). Refer to Section 6 for a detailed description of the TPS6381x registers.

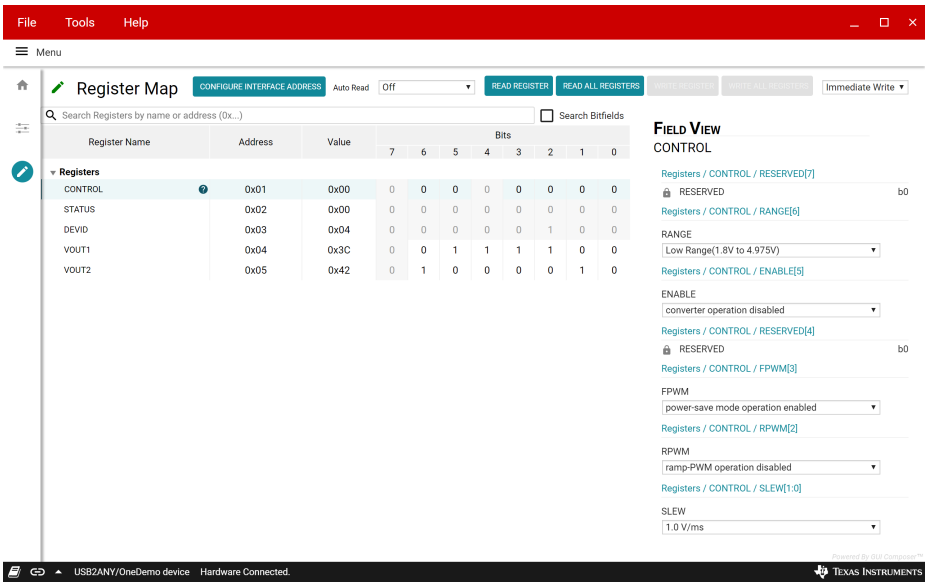

Figure 11. GUI Register Map Screen

6 Register Map

Table 4 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 4 must be considered as reserved locations and the register contents must not be modified.

Table 4. Device Registers

Address	Acronym	Register Name	Section
1h	CONTROL	Control	Go
2h	STATUS	Status	Go
3h	DEVID	Device Identity	Go
4h	VOUT1	Output Voltage 1	Go
5h	VOUT2	Output Voltage 2	Go

6.1 CONTROL Register (Address = 1h) [reset = X]

Table 5 shows the CONTROL register.

Return to Summary Table.

This register configures the device. This register is volatile, so it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 5. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	This bit is reserved for future use and must be programmed to 0.
6	RANGE	R/W	0b	This bit selects the output voltage range. 0b = low range (1.8 V to 4.975 V) 1b = high range (2.025 V to 5.2 V)
5	ENABLE	R/W	X	This bit enables and disables the converter. In the TPS63810 the reset value of this bit is 1. In the TPS63811 the reset value of this bit is 0. 0b = converter is disabled 1b = converter is enabled
4	RESERVED	R/W	0b	This bit is reserved for future use and must be programmed to 0.
3	FPWM	R/W	0b	This bit controls forced-PWM operation. 0b = forced-PWM operation disabled 1b = forced-PWM operation enabled
2	RPWM	R/W	0b	This bit controls ramp-PWM operation. 0b = ramp-PWM disabled 1b = ramp-PWM enabled
1-0	SLEW	R/W	00b	These bits control the slew rate of the converter when the output voltage setting is changed to a new value. 00b = 1 V/ms 01b = 2.5 V/ms 10b = 5 V/ms 11b = 10 V/ms

6.2 STATUS Register (Address = 2h) [reset = 0h]

Table 6 shows the STATUS register.

Return to Summary Table.

This register contains the device status. A read operation to this register clears the status bits. This register is volatile, so it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 6. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved
1	TSD	R	0b	This bit shows the status of the thermal shutdown function. This bit is cleared if the STATUS register is read when the overtemperature condition no longer exists. 0b = temperature good 1b = an overtemperature event was detected
0	$\overline{PG}$	R	0b	This bit shows the status of the output power good comparator. This bit is cleared if the STATUS register is read when the power-not-good condition no longer exists. 0b = power good 1b = a power-not-good event was detected

6.3 DEVID Register (Address = 3h) [reset = 4h]

Table 7 shows the DEVID register.

Return to Summary Table.

This register identifies the die revision of the device.

Table 7. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MANUFACTURER	R	0000b	These bits identify the manufacturer (0000b = Texas Instruments).
3-2	MAJOR	R	01b	These bits identify the major die revision. 00b = A (initial silicon) 01b = B (first major revision) 10b = C (second major revision) 11b = D (third major revision)
1-0	MINOR	R	00b	These bits identify the minor die revision. 00b = 0 (initial silicon) 01b = 1 (first minor revision) 10b = 2 (second minor revision) 11b = 3 (third minor revision)

6.4 VOUT1 Register (Address = 4h) [reset = 3Ch]

Table 8 shows the VOUT1 register.

Return to Summary Table.

This register sets the device output voltage when the VSEL pin is low. This register is volatile, so it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 8. VOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6-0	VOUT1	R/W	0111100b	These bits set the output voltage of the converter when the VSEL pin is low. When the RANGE bit = 0, the output voltage in volts is 1.8 + (VOUT1 × 0.025). When the RANGE bit = 1, the output voltage in volts is 2.025 + (VOUT1 × 0.025).

6.5 VOUT2 Register (Address = 5h) [reset = 42h]

Table 9 shows the VOUT2 register.

Return to Summary Table.

This register sets the device output voltage when the VSEL pin is high. This register is volatile, so it loses its contents if the voltage on the VIN pin becomes less than the UVLO threshold or a low logic level is applied to the EN pin.

Table 9. VOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6-0	VOUT2	R/W	1000010b	These bits set the output voltage of the converter when the VSEL pin is low. When the RANGE bit = 0, the output voltage in volts is 1.8 + (VOUT2 × 0.025). When the RANGE bit = 1, the output voltage in volts is 2.025 + (VOUT2 × 0.025).

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2019) to A Revision	Page
• Replaced TPS63810 with TPS6381x	1
• Added TPS63811 to the user's guide	1
• Updated images through user's guide	1
• Removed pre-production note	1
• Edited Section 1	3
• Added "and EN pin voltage divider" to Section 1.3	3
• Added TPS63811EVM bill of materials	9
• Changed the link to the register map	12
• Removed the pre-production note and errata list	12

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265