User's Guide

TPS54331 Step-Down Converter Evaluation Module User's Guide

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Trademarks

1 Introduction

This user's guide contains background information for the TPS54331 as well as support documentation for the TPS54331EVM-232 evaluation module (HPA232). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54331EVM-232.

1.1 Background

The TPS54331 DC/DC converter is designed to provide up to a 3-A output from an input voltage source of 3.5 V to 28 V. Table 1-1 gives the rated input voltage and output current range for the evaluation module. This evaluation module is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54331 regulator. The switching frequency is internally set at a nominal 570 kHz. The high-side MOSFET is incorporated inside the TPS54331 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54331 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54331 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 30 V for the TPS54331EVM-232.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54331EVM-232	V_{IN} = 7 V to 28 V	0 A to 3 A

1.2 Performance Specification Summary

Table 1-2 provides a summary of the TPS54331EVM-232 performance specifications. Specifications are given for an input voltage of V_{IN} = 15 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54331EVM-232 is designed and tested for V_{IN} = 10 V to 35 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54331EVM-232 and Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
VIN voltage range			7	15	28	V
Output voltage set point				3.3		V
Output current range	V_{IN} = 7 V to 28 V		0		3	A
Line regulation	I_O = 1.5 A, V_{IN} = 7 V–28 V			±0.2%		
Load regulation	V_{IN} = 14 V, I_O = 0 A to 3 A			±0.15%		
Load transient response	I_O = 0.75 A to 2.25 A	Voltage change		–100		mV
		Recovery time		160		µs
	I_O = 2.25 A to 0.75 A	Voltage change		100		mV
		Recovery time		160		µs
Loop bandwidth	V_{IN} = 25 V, I_O = 1 A			25.0		kHz
Phase margin	V_{IN} = 25 V , I_O = 1 A			58		°
Input ripple voltage	I_O = 3 A			200		mVpp
Output ripple voltage	I_O = 3 A			10		mVpp
Output rise time				3.5		ms
Operating frequency				570		kHz
Maximum efficiency	V_{IN} = 10 V, V_O = 5 V, I_O = 0.75 A			91.6%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54331. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVMs, change the value of resistor R6. Changing the value of R6 can change the output voltage above 0.8 V. The value of R6 for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{1.221\ V}{V_O - 1.221\ V} \quad (1)$$

Table 1-3 lists the R6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on time is greater than 150 ns, and the maximum duty cycle is less than 93%. The values given in Table 1-3 are standard values, not the exact value calculated using Table 1-3.

Table 1-3. Output Voltages Available

Output Voltage (V)	R_2 Value (kΩ)
1.8	8.25
2.5	4.75
3.3	3.24
5	1.96

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54331EVM-232 and evaluation modules. The section also includes test results typical for the evaluation modules and covers the following:

- Efficiency
- Output voltage regulation
- Load transients
- Loop response
- Output ripple
- Input ripple
- Start-up

2.1 Input and Output Connections

The TPS54331EVM-232 is provided with input and output connectors and test points as shown in Table 2-1. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J4 through a pair of 20 AWG wires. The maximum load current capability must be 3 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the VIN input voltages with TP2 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP6 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN (see Table 1-1 for VIN range)
J2	2-pin header for enable. Connect EN to ground to disable, open to enable.
J3	2-pin header for slow-start monitor and GND
J4	VOUT, 3.3 V at 3-A maximum
TP1	VIN test point at VIN connector
TP2	GND test point at VIN
TP3	PH test point
TP4	Test point between voltage divider network and R3. Used for loop response measurements.
TP5	Output voltage test point at OUT connector
TP6	GND test point at OUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.6 A–1 A and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54331EVM-232 at an ambient temperature of 25°C.

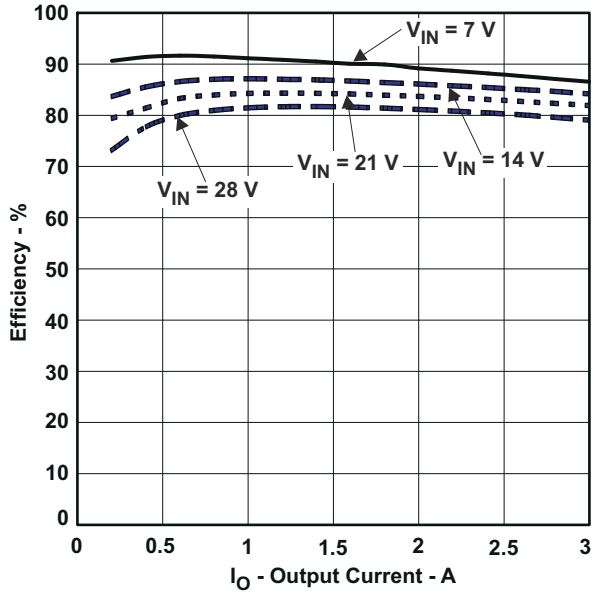

Figure 2-1. TPS54331 Efficiency

Figure 2-2 shows the efficiency for the TPS54331EVM-232 at lower output currents between 0.01 A and 0.20 A at an ambient temperature of 25°C.

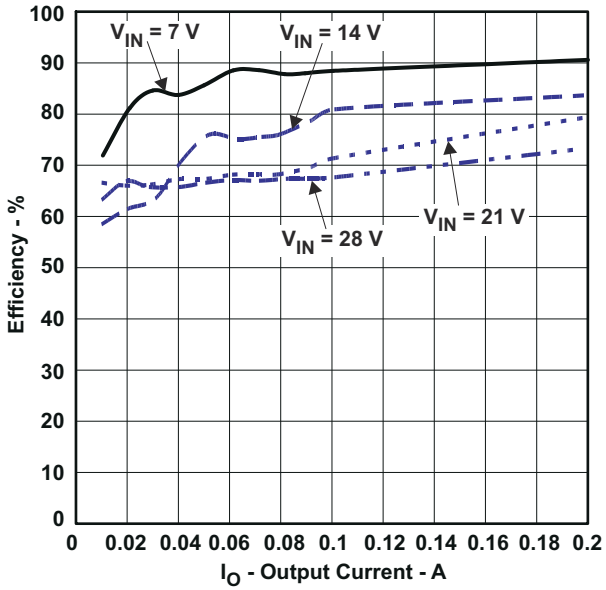

Figure 2-2. TPS54331 Low Current Efficiency

The efficiency can be lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the MOSFETs.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the TPS54331EVM-232 load regulation.

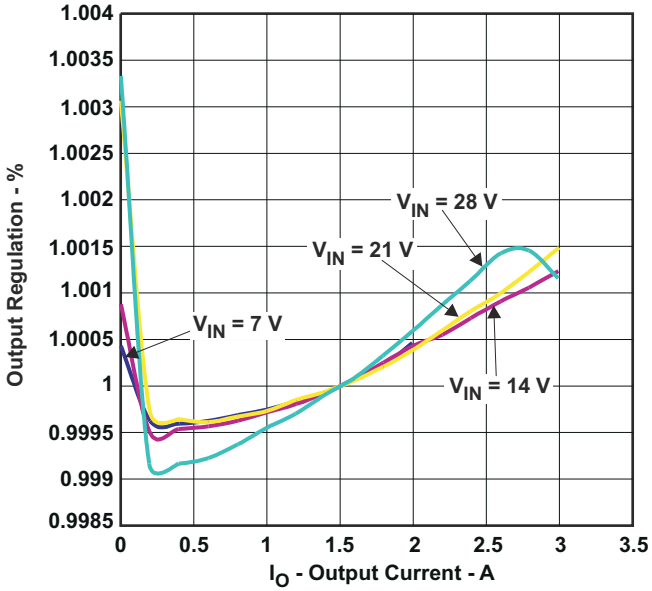

Figure 2-3. TPS54331 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the TPS54331EVM-232 line regulation.

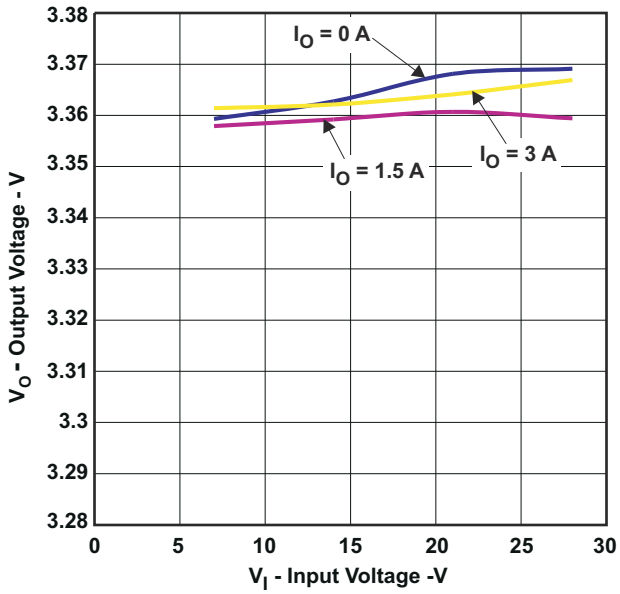

Figure 2-4. TPS54331 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54331EVM-232 response to load transients. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

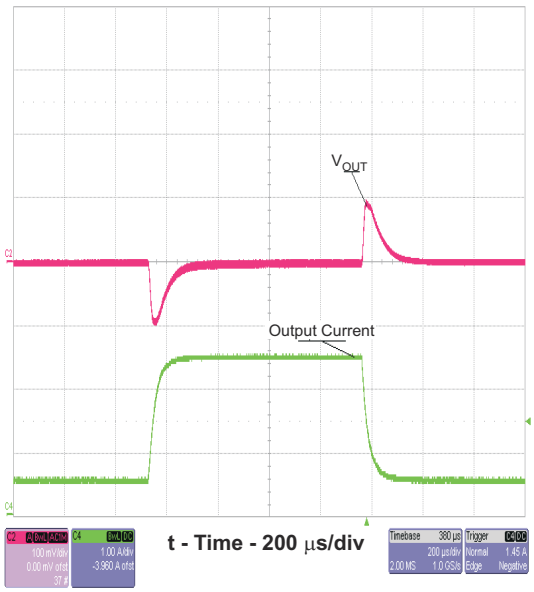

Figure 2-5. TPS54331 Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54331EVM-232 loop response characteristics. Gain and phase plots are shown for VIN voltage of 15 V. Load current for the measurement is 1.5 A.

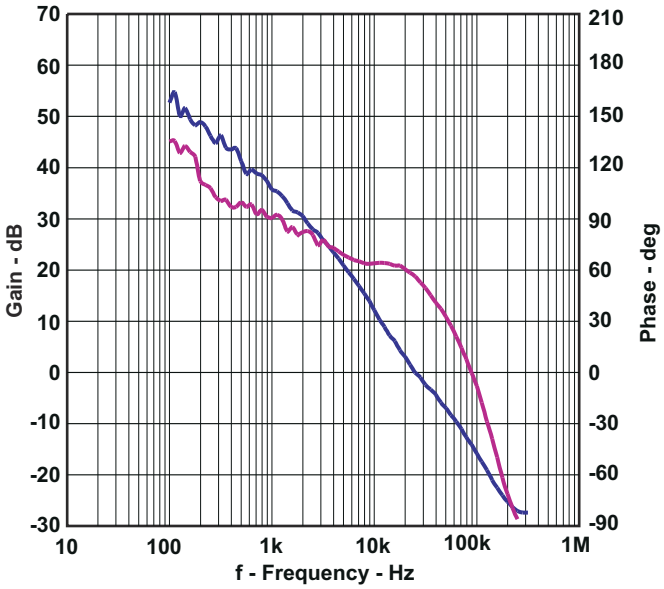

Figure 2-6. TPS54331 Loop Response

2.7 Output Voltage Ripple

Figure 2-7 shows the TPS54331EVM-232 output voltage ripple. The output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.Figure 2-7

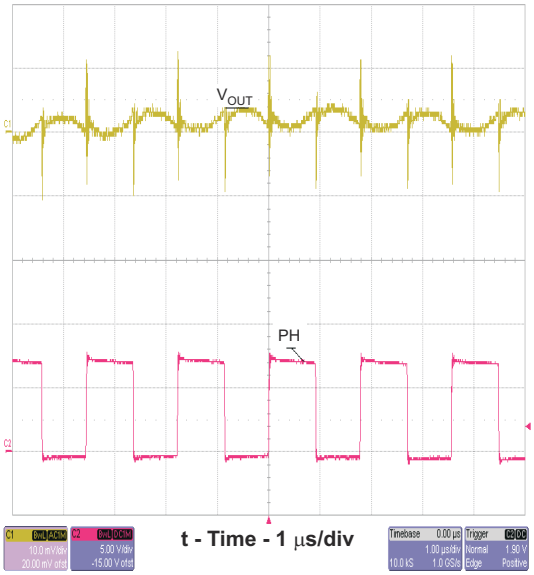

Figure 2-7. TPS54331 Output Ripple

2.8 Input Voltage Ripple

Figure 2-8 shows the TPS54331EVM-232 input voltage ripple. The output current for each device is at full rated load of 3 A.

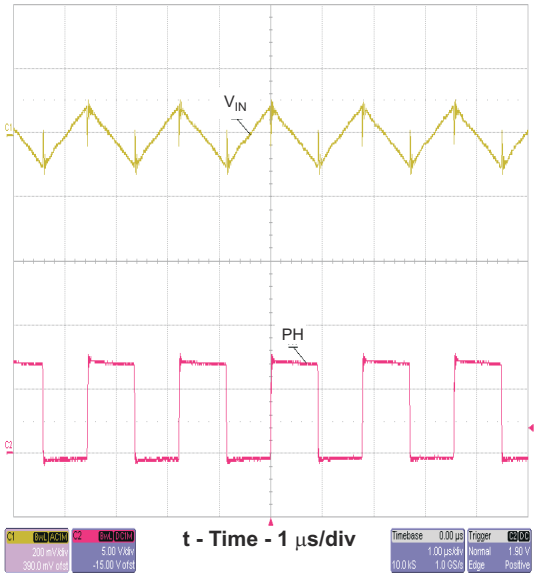

Figure 2-8. TPS54331 Input Ripple

2.9 Powering Up

Figure 2-9 and Figure 2-10 shows the start-up waveform. In Figure 2-9, the top trace shows V_{IN}, and the bottom trace shows V_{OUT}. InFigure 2-9, the top trace shows EN (enable) whereas the bottom trace shows VOUT. Initially, the input voltage is applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage of 1.25 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate toward 0.8 V and the output voltage ramps up to the externally set value of 3.3 V.

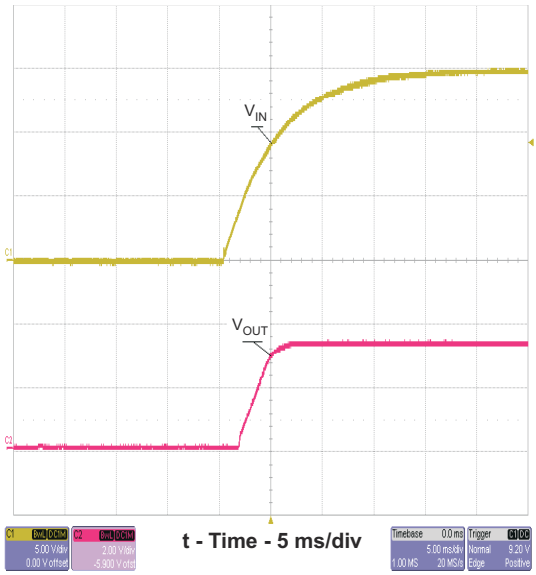

Figure 2-9. TPS54331 Start-Up Relative to V_{IN}

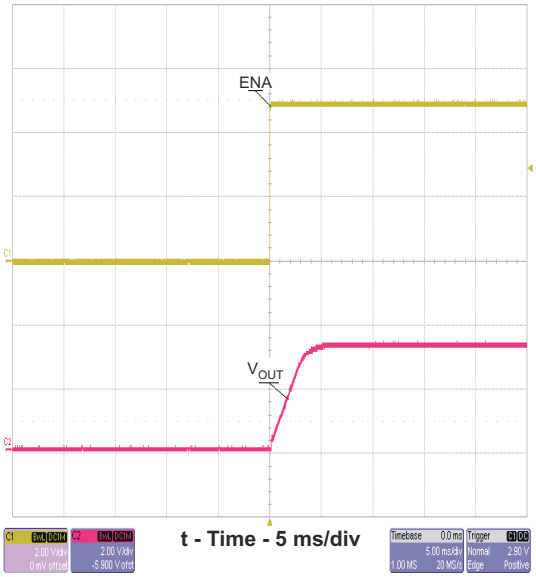

Figure 2-10. TPS5331 Start-Up Relative to Enable

3 Board Layout

This section provides a description of the TPS54331EVM-232, board layout, and layer illustrations.

3.1 Layout

Figure 3-1 through Figure 3-3 show the TPS54331EVM-232 board layout. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for VIN, OUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54331 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including four vias directly under the TPS54331 device to provide a thermal path from the top-side ground traces to the bottom-side ground plane.

The input decoupling capacitors (C1, C2, and C3) and bootstrap capacitor (C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper VOUT trace past the output capacitor C3. For the TPS54331, an additional input bulk capacitor can be required, depending on the EVM connection to the input supply.

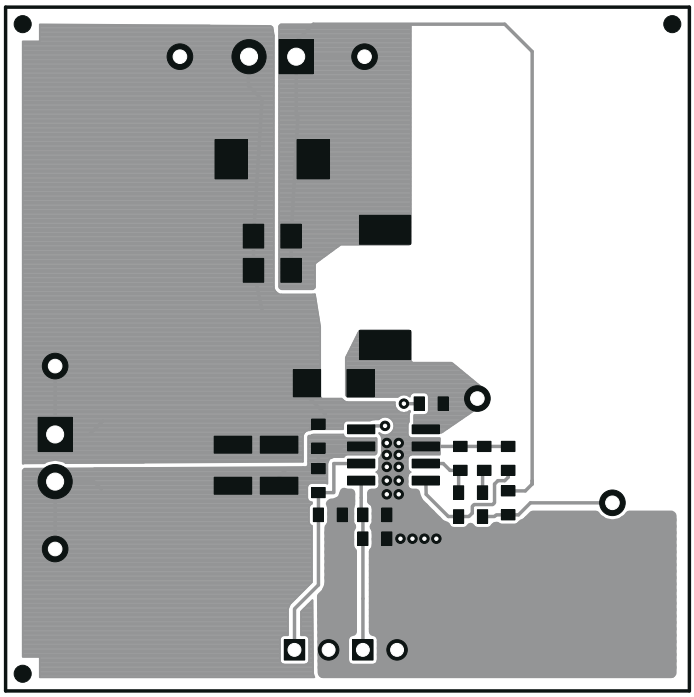

Figure 3-1. Top-Side Layout

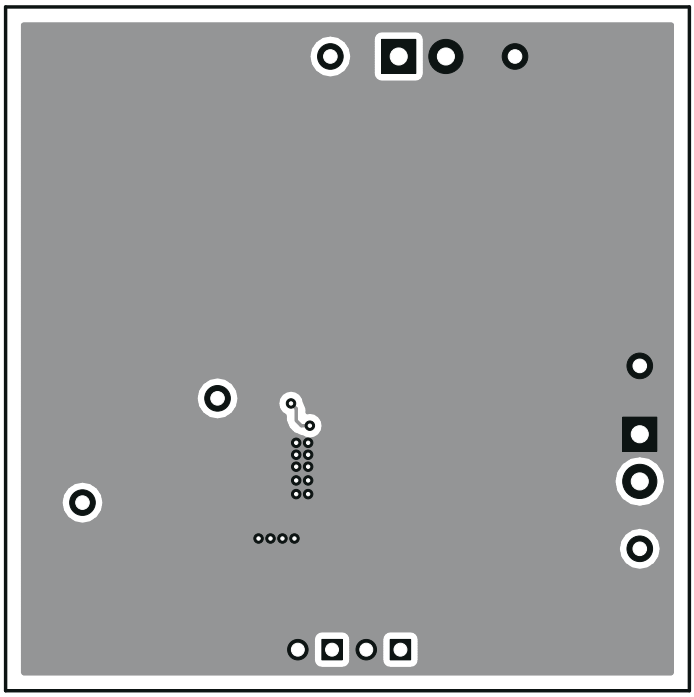

Figure 3-2. Bottom-Side Layout (Looking From Top Side)

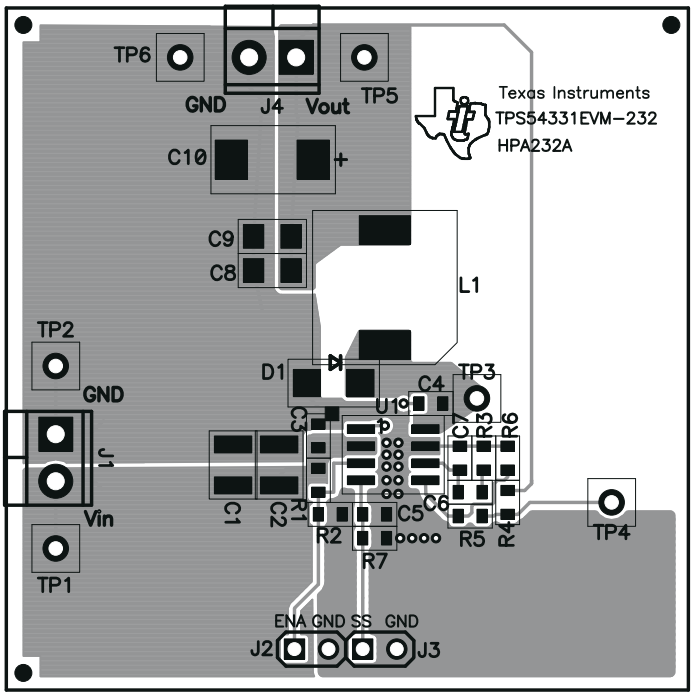

Figure 3-3. Top-Side Assembly

4 Schematic and Bill of Materials

This section presents the TPS54331EVM-232 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54331EVM-232.

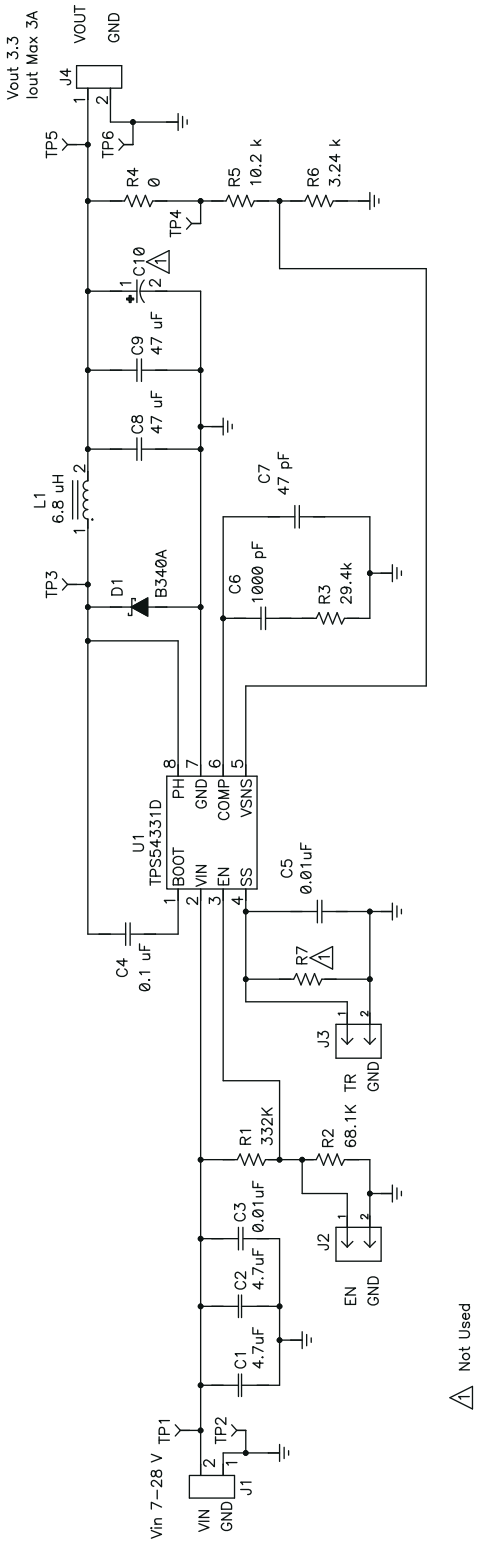

Figure 4-1. TPS54331EVM-232 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54331EVM-232..

Table 4-1. TPS54331EVM-232 Bill of Materials

Count	Ref Des	Value	Description	Size	Part Number	Mfr
2	C1, C2	4.7 µF	Capacitor, Ceramic, 50 V, X7R, 20%	1210	Std	Std
0	C10			7343(D)	Std	Std
1	C3	0.01 µF	Capacitor, Ceramic, 50 V, X7R, 10%	0603	Std	Std
1	C4	0.1 µF	Capacitor, Ceramic, 16 V, X7R, 10%	0603	Std	Std
1	C5	0.01 µF	Capacitor, Ceramic, 16 V, X7R, 10%	0603	Std	Std
1	C6	1000 pF	Capacitor, Ceramic, 16 V, X7R, 10%	0603	Std	Std
1	C7	47 pF	Capacitor, Ceramic, 16 V, X7R, 10%	0603	Std	Std
2	C8, C9	47 µF	Capacitor, Ceramic, 6.3, X5R, 20%	1206	C3216X5R0J476MT	TDK
1	D1	B340A	Diode, Schottky, 3 A, 40 V	SMA	B340A	Diodes Inc
2	J1, J4	ED1514	Terminal Block, 2-pin, 6 A, 3.5 mm	0.27 × 0.25 inch	ED1514	OST
2	J2, J3	PTC36SAAN	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	
1	L1	6.8 µH	Inductor, SMT, 3.84 A, 35 mΩ	0.406 × 0.409	CDRH103RNP-6R8	Sumida
1	R1	332 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	68.1 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	29.4 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	10.2 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	3.24 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7		Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	TP1, TP3, TP5	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
3	TP2, TP4, TP6	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
1	U1	TPS5433xD	IC, DC-DC Converter, 28 V, 3 A	SO-8	TPS54331D	TI
1	—		PCB, HPA232	2.0" × 2.0" × 0.062"	HPA232	Any
2	—		Shunt, 100-mil, Black	0.100	929950-00	3M

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2008) to Revision A (October 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2

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