TPS65053EVM-217

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1 Introduction

The Texas Instruments TPS65053EVM-217 evaluation module (EVM) enables designers to easily evaluate the operation and performance of the TPS65053 PMIC for applications that are powered with one Li Ion or Li Polymer cell and require multiple power rails. The TPS65053 contains two highly efficient step-down switching converters, three low dropout (LDO) linear regulators and a voltage monitor /RESET\ output.

2 Setup

This chapter describes the jumpers and connectors on the EVM, as well as how to properly connect, set up, and use the TPS65053EVM-217.

2.1 Input/Output Connector Descriptions

J1 - VLDO1

This is the positive output for the VLDO1 LDO linear regulator. This output is externally adjustable for the TPS65053 and comes preset to 1.6 V. The VLDO1 output is capable of supplying up to 400 mA.

J2 - GND

This is the return connection for the VLDO1 output rail.

J3 - VLDO2

This is the positive output for the VLDO2 LDO linear regulator. This output is externally adjustable for the TPS65053 and comes preset to 3.3 V. The VLDO2 output is capable of supplying up to 200 mA.

J4 - GND

This is the return connection for the VLDO2 output rail.

J5 - VLDO3

This is the positive output for the VLDO3 LDO linear regulator. This output is fixed for the TPS65053 at 1.3 V. The VLDO3 output is capable of supplying up to 200 mA.

J6 - GND

This is the return connection for the VLDO3 output rail.

J7 - VOUT DCDC1

This is the positive output for VDCDC1 step-down converter. This output is externally adjustable for the TPS65053 and comes preset to 2.85 V. VDCDC1 is capable of sourcing up to 1 A.

J8 - GND

This is the return connection for the VDCDC1 output rail.

J9 - VIN

This is the positive input voltage connection to the converter. The EVM operates from any supply voltage between 2.5 V and 6.0 V. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission and input voltage droop.

J10 - GND

This is the input return connection for the input power supply.

J11 - VOUT DCDC2

This is the positive output for VDCDC2 step-down converter. This output is externally adjustable for the TPS65053 and comes preset to 1.8 V. VDCDC2 is capable of sourcing up to 600 mA.

J12 - GND

This is the return connection for the VDCDC2 output rail.

TP1 -/RESET

TP1 allows the user to monitor /RESET output. The /RESET output goes high 100 ms after the THRESHOLD input exceeds 1 V. /RESET goes low when the THRESHOLD input falls below 1 V. On the EVM, the /RESET circuitry monitors the input voltage. The threshold is set to a 3.3-V input.

JP1 - MODE Input

JP1 is used to select between the forced PWM and Power Save mode (PSM) operation for the switching converters. Place a shorting bar in the PSM position to select the Power Save mode. In this mode, PFM is used for light loads, and PWM is used for heavier loads. Place a shorting bar in the PWM position to force PWM operation at all loads.

JP2 - EN_LDO1

JP2 is used to enable the VLDO1 output. Place a shorting bar in the ON position to turn the VLDO1 LDO converter on. Place the shorting bar in the OFF position to turn the VLDO1 LDO converter off.

JP3 - EN_DCDC2

JP3 is used to enable the VDCDC2 output. Place a shorting bar in the ON position to turn the VDCDC2 step-down converter on. Place a shorting bar in the OFF position to turn VDCDC2 converter off.

JP4 - EN_DCDC1

JP4 is used to enable the VDCDC1 output. Place a shorting bar in the ON position to turn the VDCDC1 step-down converter on. Place a shorting bar in the OFF position to turn VDCDC1 converter off.

JP5 - EN_LDO2

JP5 is used to enable the VLDO2 output. Place a shorting bar in the ON position to turn the VLDO2 LDO converter on. Place the shorting bar in the OFF position to turn the VLDO2 LDO converter off.

JP6 - EN_LDO3

JP6 is used to enable the VLDO3 output. Place a shorting bar in the ON position to turn the VLDO3 LDO converter on. Place the shorting bar in the OFF position to turn the VLDO1 LDO converter off.

2.2 EVM Setup

2.2.1 EVM Factory Configuration

The EVM is configured to provide the following nominal operating conditions:

- Input Voltage: 2.5 V to 6.0 V
- Output Voltage: See Table 1
- Maximum Load Current: See Table 2

Table 1. EVM Preset Output Voltage

Output	TPS65053EVM
VDCDC1	1.85 V
VDCDC2	1.8 V
VLD01	1.6 V
VLD02	3.3 V
VLD03	1.3 V

Table 2. Maximum Load Current

Output	TPS65053EVM
VDCDC1	1 A
VDCDC2	600 mA
VLD01	400 mA
VLD02	200 mA
VLD03	200 mA

2.3 Operation

1. Configure all EVM jumpers to factory settings shown in Table 3.
2. Connect the input voltage return to J2.
3. Connect the positive input voltage to J1.
4. Connect all loads to the outputs.
5. Turn on input voltage.

Table 3. Factory EVM Jumper Settings

Jumper	Shunt Location
	TPS65053EVM
JP1	Between PWM and MODE
JP2	Between ON and EN_LDO1
JP3	Between ON and EN_DCDC2
JP4	Between ON and EN_DCDC1
JP5	Between ON and EN_LDO2
JP6	Between ON and EN_LDO3

3 Board Layout

This chapter provides the TPS65053EVM-217 board layout and illustrations.

3.1 Layout

Figure 1, Figure 2, and Figure 3 show the board layout for the TPS65053EVM-217 PWB.

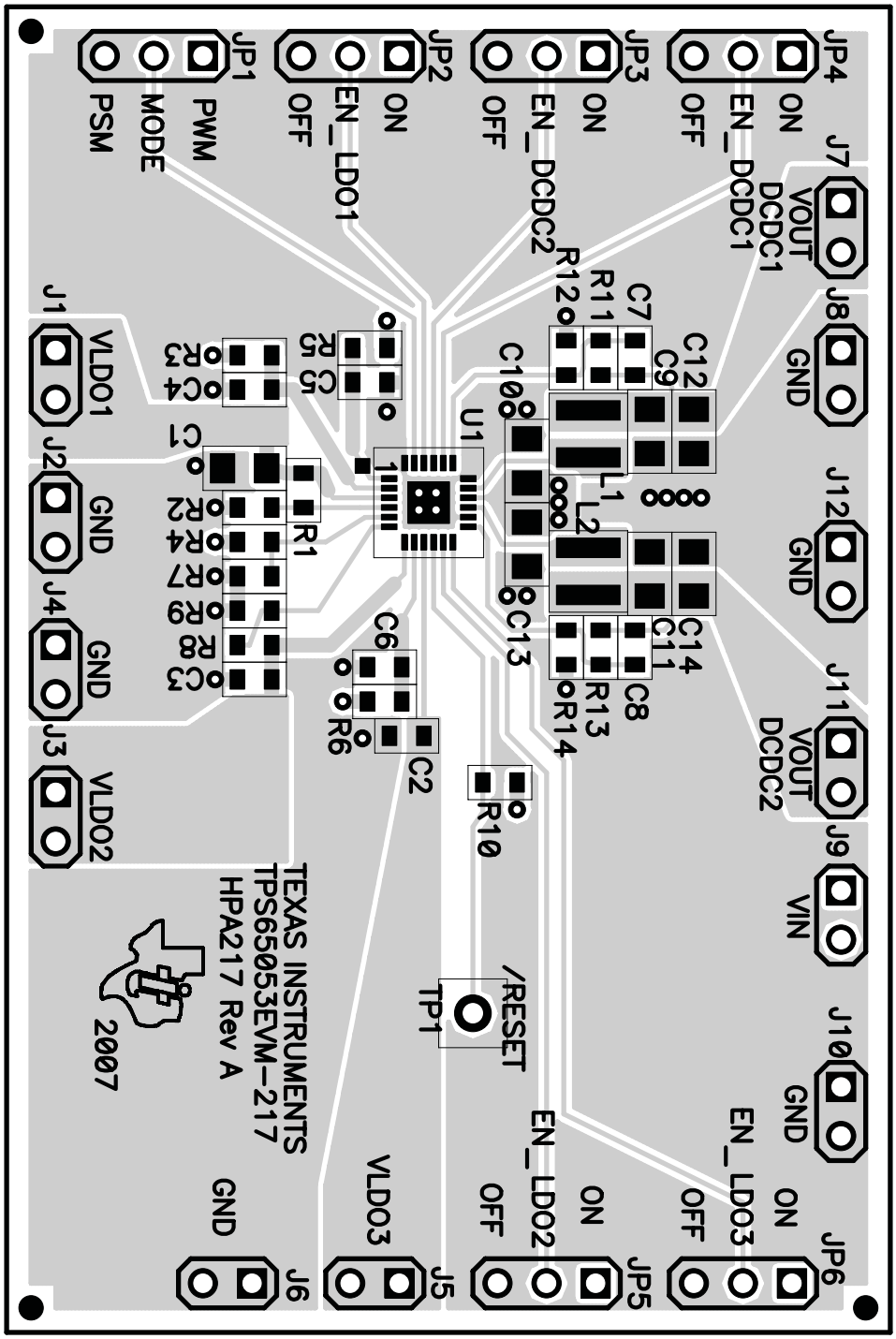

Figure 1. Assembly Layer

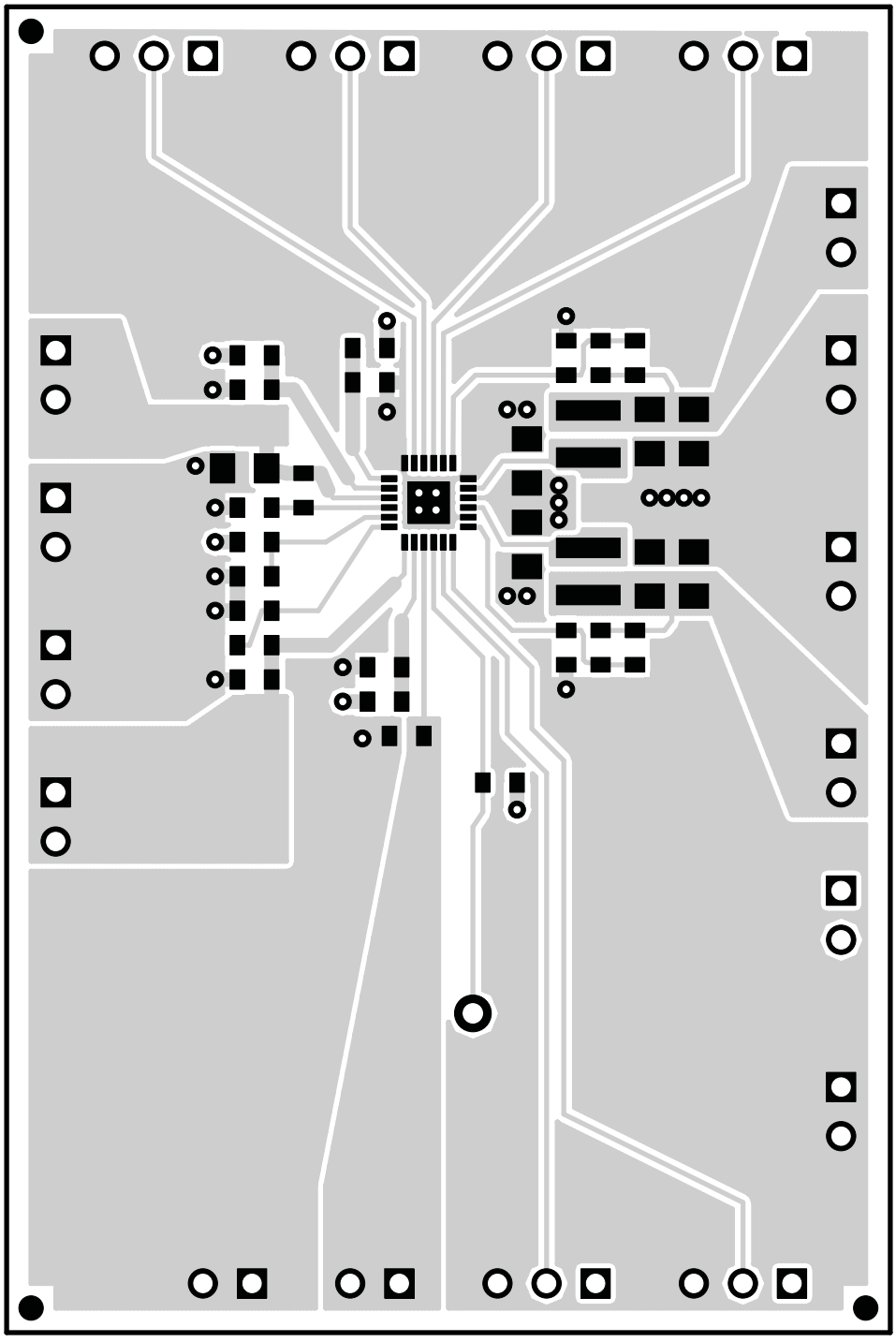

Figure 2. Top Layer Routing

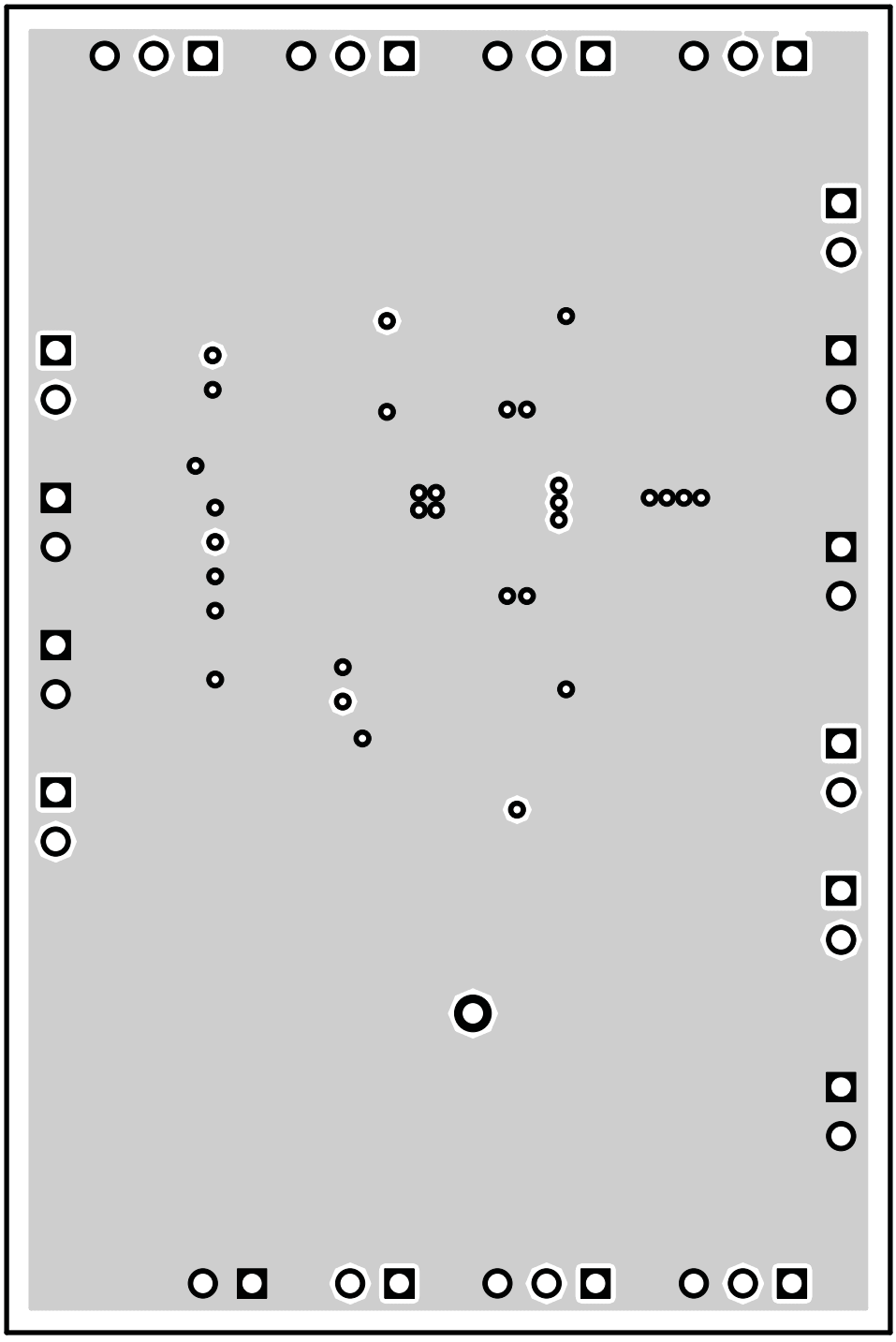

Figure 3. Inner Layer 2 Routing

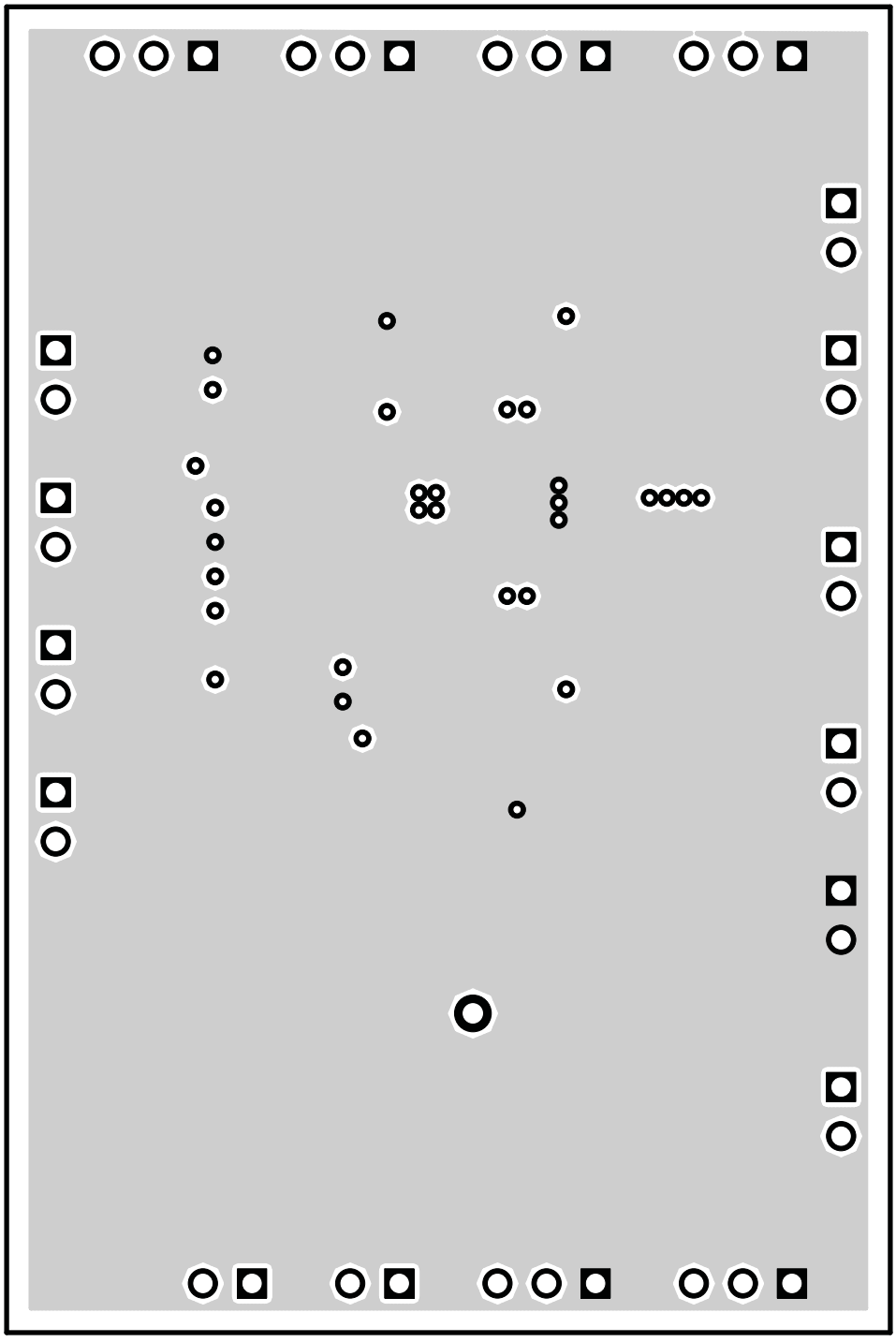

Figure 4. Inner Layer 3 Top Layer Routing

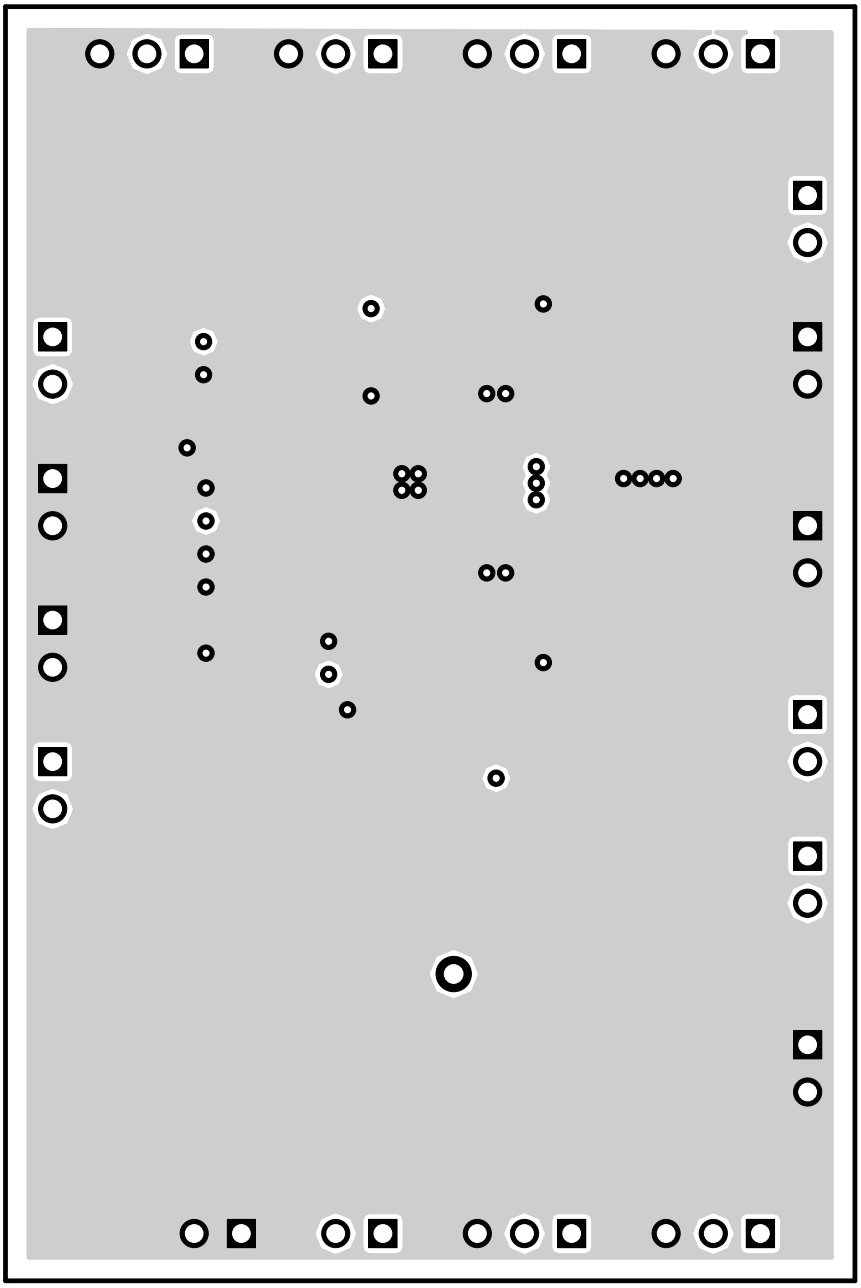

Figure 5. Bottom Layer Routing

4 Schematic and Bill of Materials

This chapter provides the TPS65053EVM-217 schematic and bill of materials.

4.1 Schematic

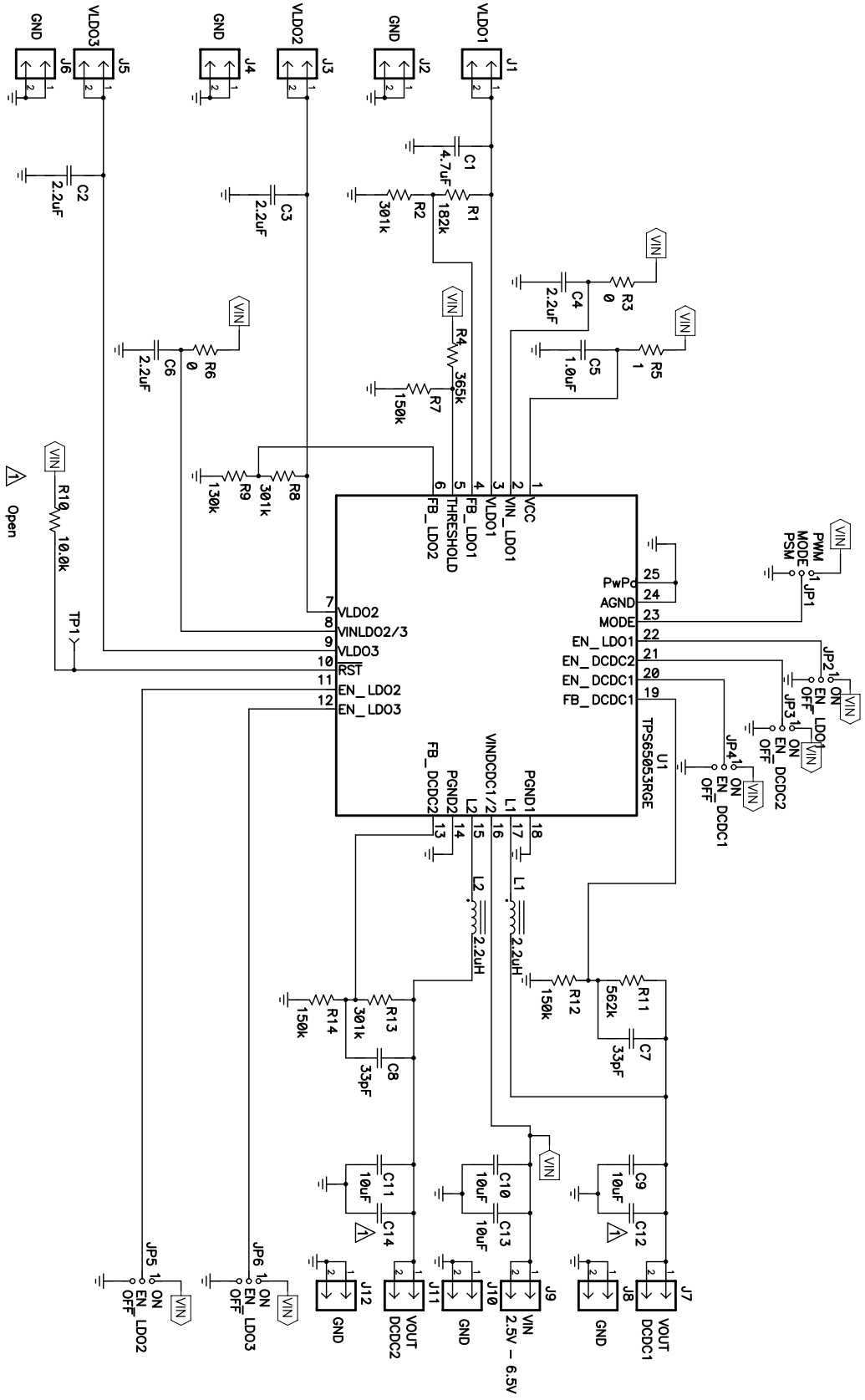

Figure 6. TPS65053EVM-217 Schematic

4.2 Bill of Materials

Table 4. TPS65053EVM-217 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	4.7 µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM219R61A475KE19D	muRata
0	C12,C14	Open	Capacitor, Ceramic	0805		
4	C2, C3, C4, C6	2.2 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	GRM188R61A225KE34D	muRata
1	C5	1.0 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	C1608X7R1C105K	TDK
2	C7, C8	33 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H330J	TDK
4	C9, C10, C11, C13	10 µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	muRata
12	J1–J12		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
6	JP1–JP6		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
2	L1, L2	2.2 µH	Inductor, SMT, 1.5A, 110milliohm	0.118 ×0.118	LPS3015-222ML	Coilcraft
1	R1	182 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R11	562 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R2, R8, R13	301 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R6	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R4	365 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	1	Resistor, Chip, 1/16W, 5%	0603	Std	Std
3	R7, R12, R14	150 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	130 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	TP1		Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keystone
1	U1		IC, 2.25 MHz Dual Step-down Converter With 3 Low Input Voltage LDOs	QFN24	TPS65053RGE	TI
1	- -		PCB, 2.7 in × 1.8 in × 0.062 in		HPA217	Any
6	- -		Shunt, 100mil, Black	0.100	929950-00	3M

Related Documentation From Texas Instruments

TPS65053 data sheet (SLVS754)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 6 V and the output voltage range of 0.6 V to V_{INXX}.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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