PGA5807, 8-Channel, High-Bandwidth, Analog Front-End Evaluation Module

This user's guide gives a general overview of the PGA5807 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the PGA5807 analog front-end. The PGA5807 EVM provides a platform for evaluating the ADC under various signal, clock, reference, and ADC output formats.

Contents

List of Figures

List of Tables

1 Quick View of Evaluation Setup

Figure 1 is an overview of the evaluation setup that includes the PGA5807 EVM, TSW1400 data capturing card, external equipment, personal computer (PC), and software requirements.

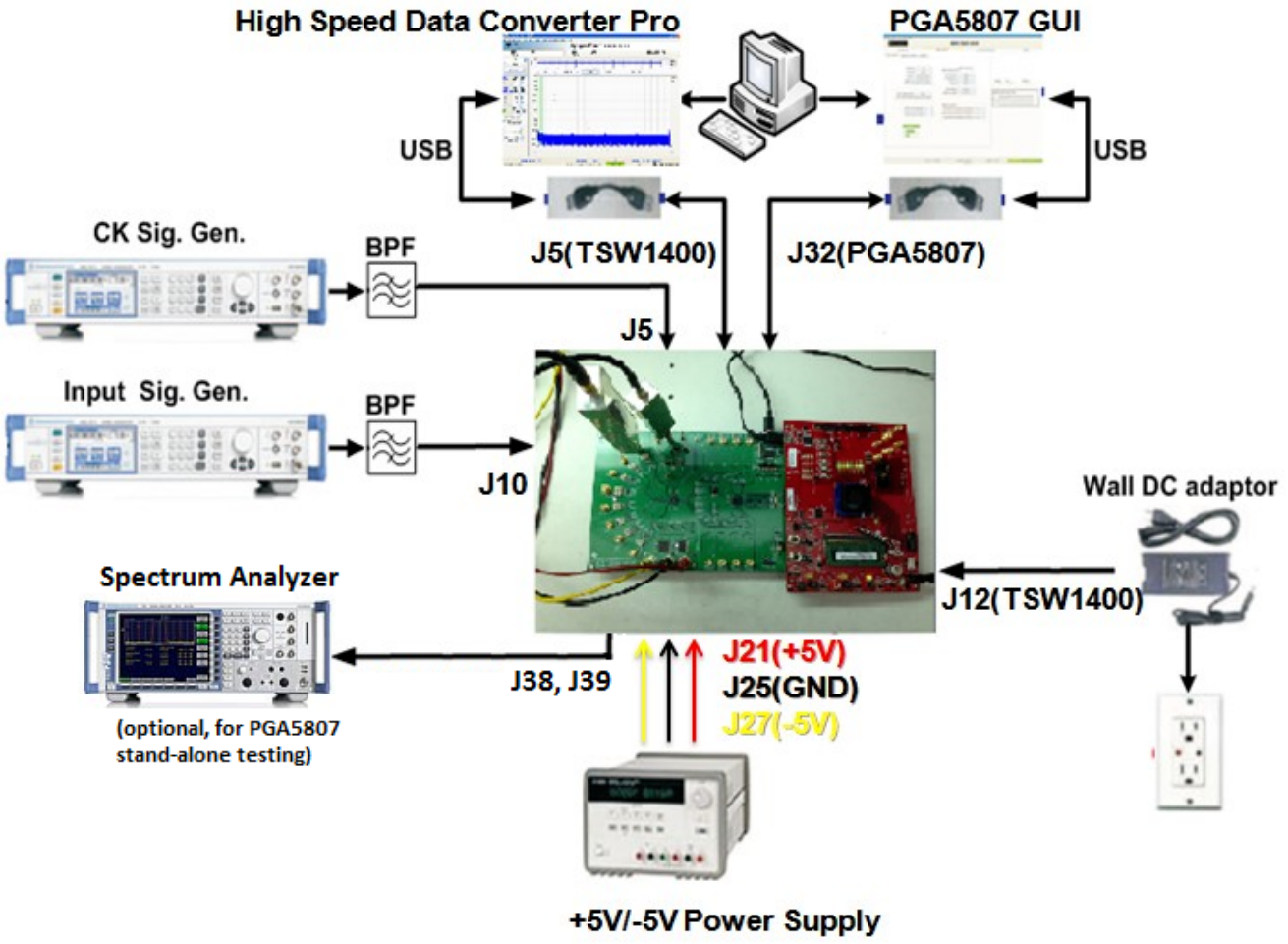


Figure 1. Evaluation Setup

PGA5807 EVM: The PGA5807 EVM contains both the PGA5807 device and the ADS5296 ADC from Texas Instruments. With this, a complete signal chain can be evaluated with the output of the ADS5296 ADC being captured by the TSW1400 EVM. The EVM is configured to allow for the following without any hardware changes required: testing stand-alone PGA5807, testing stand-alone ADS5296, or testing cascaded PGA507 plus ADS5296. For more information pertaining to the ADS5296 device, see: http://www.ti.com/product/ads5296

TSW1400 EVM: The high-speed LVDS deserializer board is required for capturing data from the PGA5807 EVM and its analysis using the TSW1400 graphical user interface (GUI), called *High Speed Data Converter Pro* (*HSDCpro*). For more information pertaining to the TSW1400 EVM, see: http://focus.ti.com/docs/toolsw/folders/print/tsw1400evm.html

Equipment: Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, band-pass filters (BPF) are required in signal and clock paths to attenuate the harmonics and noise from the generators.

Power Supply: A +5-V supply powers the PGA5807 EVM through connectors **J21(+5V)** and **J25(GND)** providing power to both the PGA5807 and ADS296 devices. The positive power supply must be able to source up to 1.5 A. A –5-V (negative) supply is required to provide power to amplifiers on the EVM when testing the PGA5807 in stand-alone mode only. The negative power supply must be able to source 300 mA. The TSW1400 EVM is powered through an AC adaptor provided with its EVM kit.

USB Interface to PC: The USB connections from the PGA5807 EVM and TSW1400 EVM to the personal computer (PC) are used for communication from the GUIs to the boards. Section 2 explains the TSW1400 and PGA5807 GUI installation procedures.

2 GUI Software Installation

The PGA5807 EVM and the TSW1400 EVM both require software installations. The following two sections explain where to find and how to install the software properly. Ensure that no USB connections are made to the EVMs until after the installations are complete.

2.1 TSW1400 EVM GUI Installation (High Speed Data Converter Pro (HSDCpro))

From the Texas Instruments website, www.ti.com, search for TSW1400. Under Technical Documents, one will find a ***Software*** section from which ***High Speed Data Converter Pro GUI Installer*** can be downloaded and saved (slwc107e.zip or higher).

- Unzip the saved folder and run the installer executable to obtain the menu shown in Figure 2.
- Click the *Install* button.

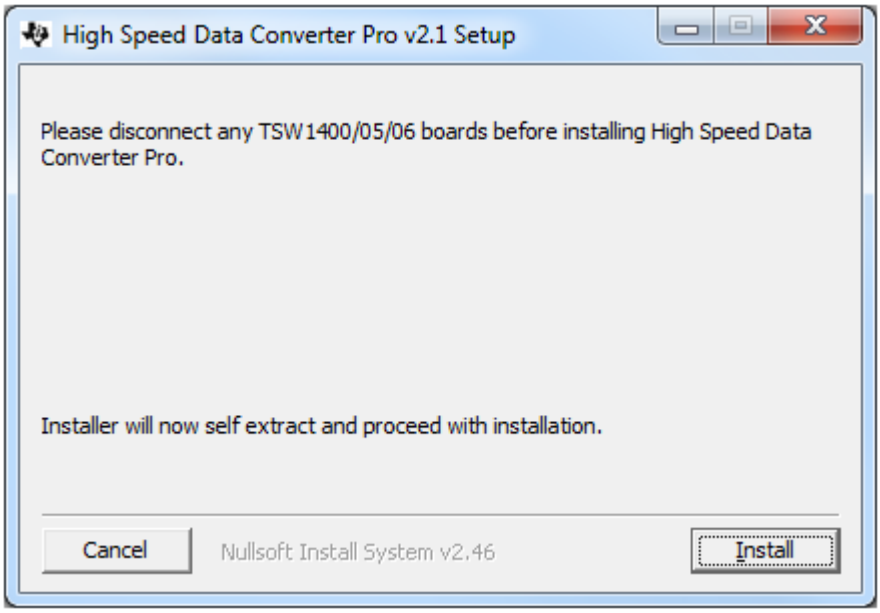


Figure 2. HSDCpro Install (a)

- Set the destination directories, or leave as default, for the TSW1400 GUI installation and press the *Next* button as shown in Figure 3.

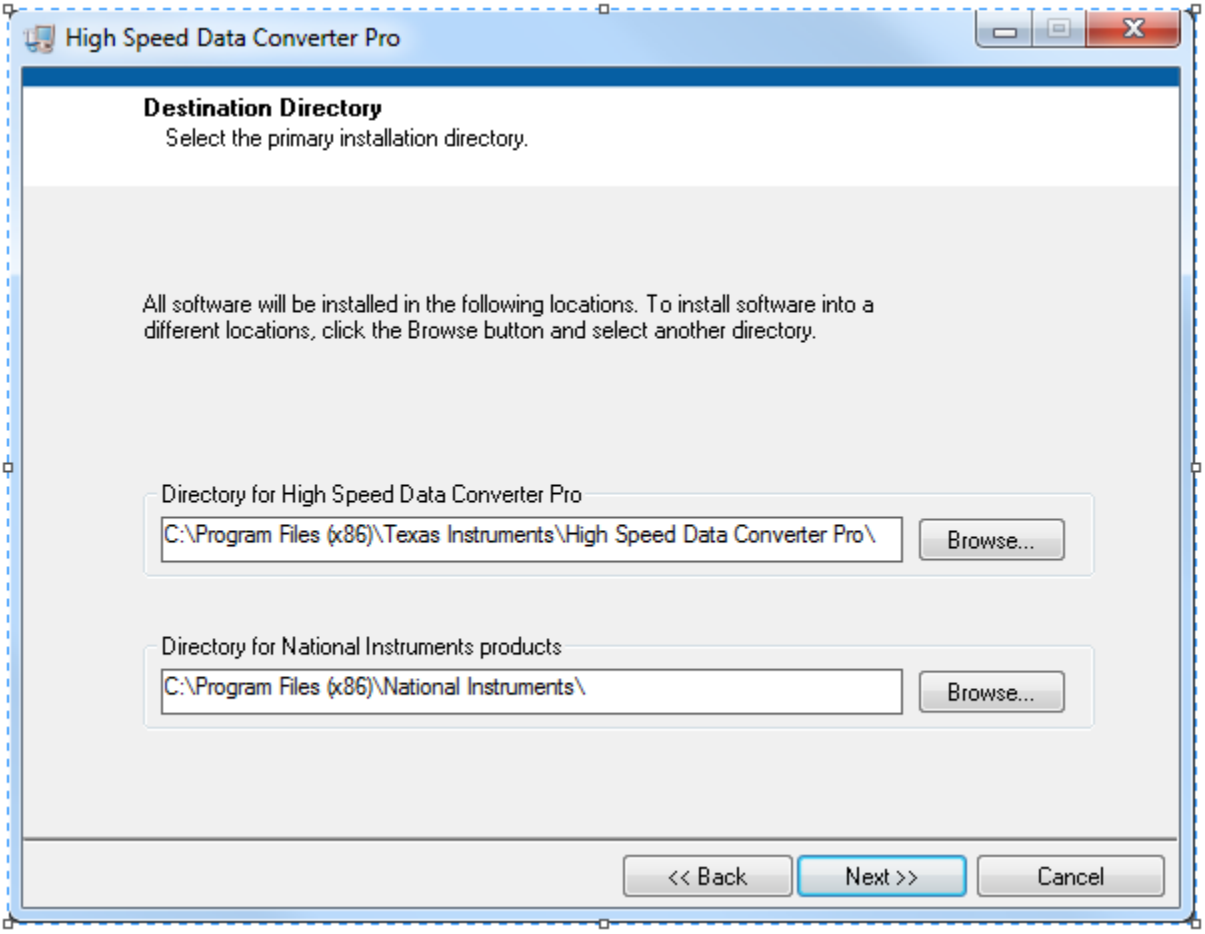


Figure 3. HSDCpro Install (b)

- Read the License Agreement from Texas Instruments and select *I accept the License Agreement* and press the *Next* button as shown in Figure 4.

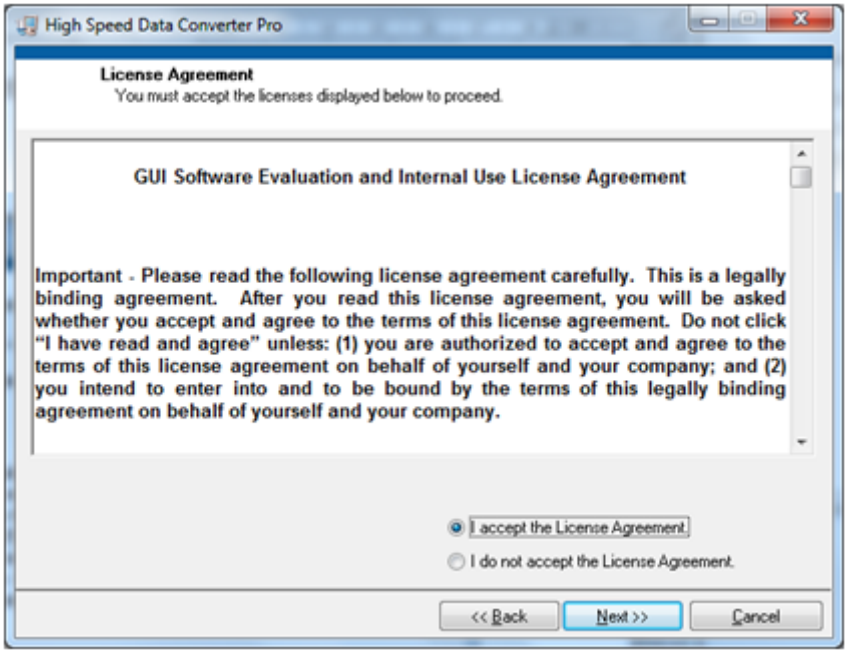


Figure 4. HSDCpro Install (c)

- Read the License Agreement from National Instruments and select *I accept the License Agreement* and press the *Next* button as in Figure 5.

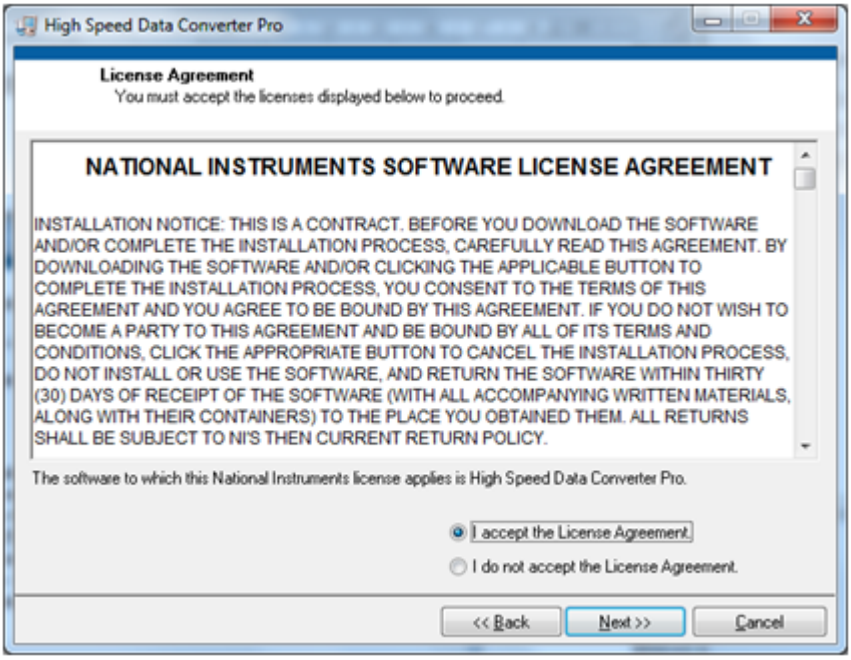


Figure 5. HSDCpro Install (d)

- Press the Next button as shown in Figure 6.

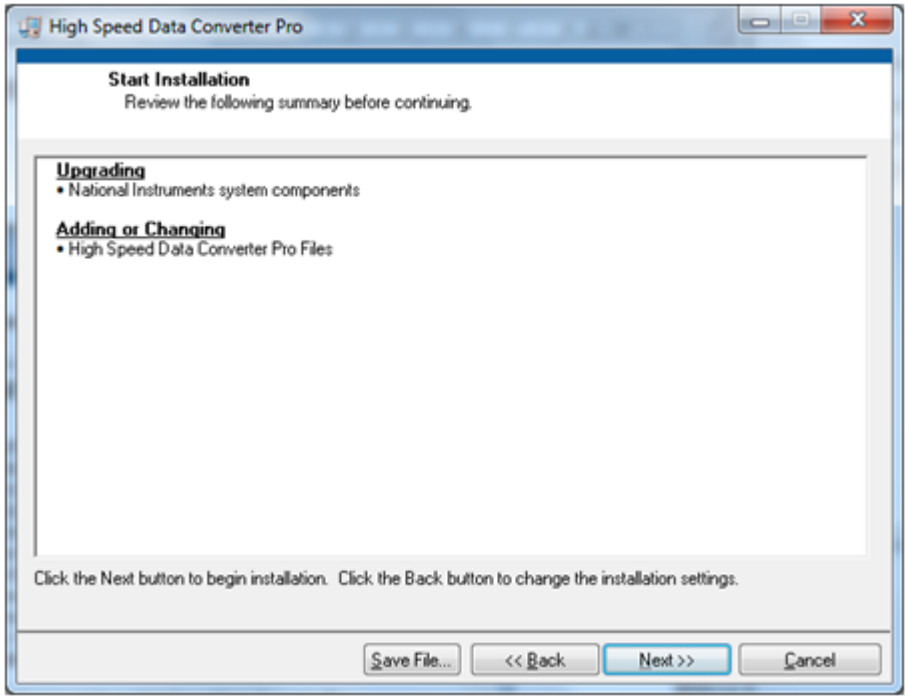


Figure 6. HSDCpro Install (e)

- The window shown in Figure 7 should appear, indicating that installation is in progress.

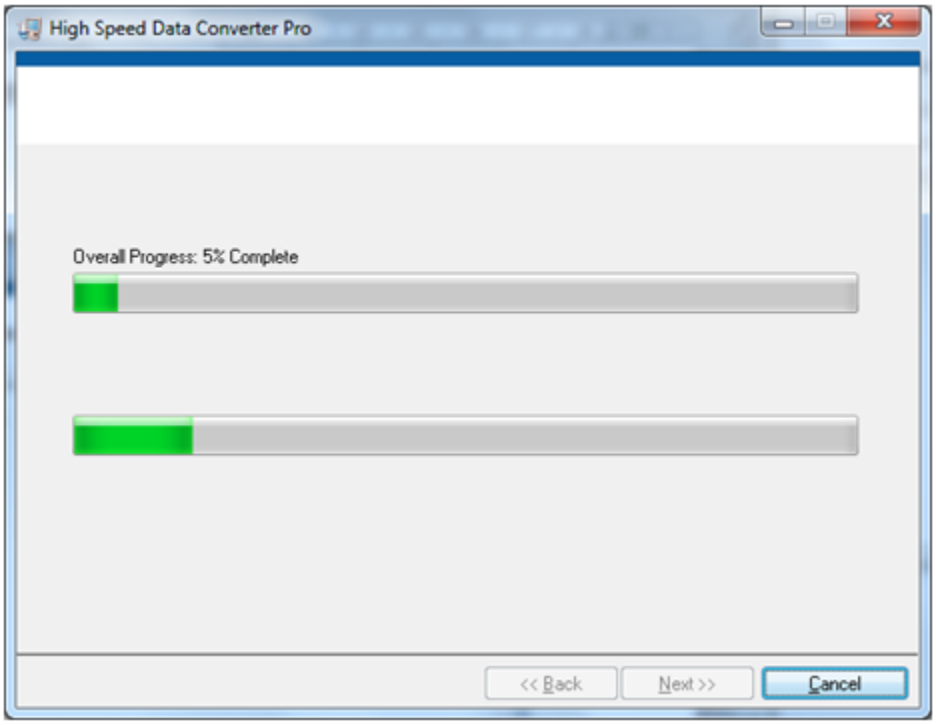


Figure 7. HSDCpro Install (f)

- The window shown in Figure 8 appears indicating *Installation Complete*. Press the *Next* button.

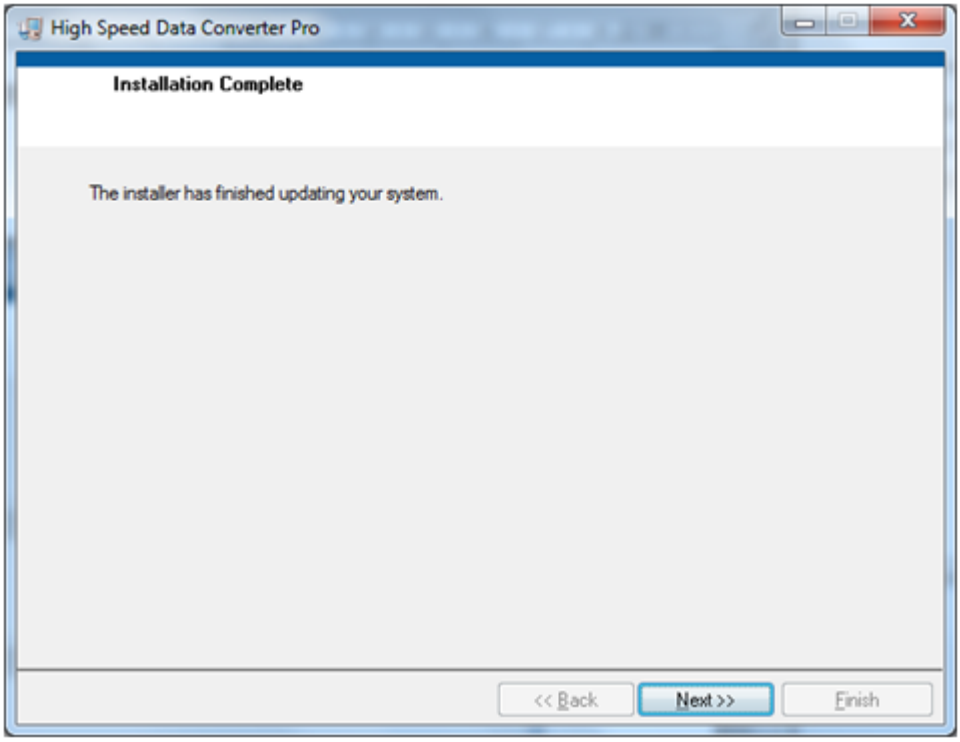


Figure 8. HSDCpro Install (g)

- The window in Figure 9 appears briefly to complete the process.

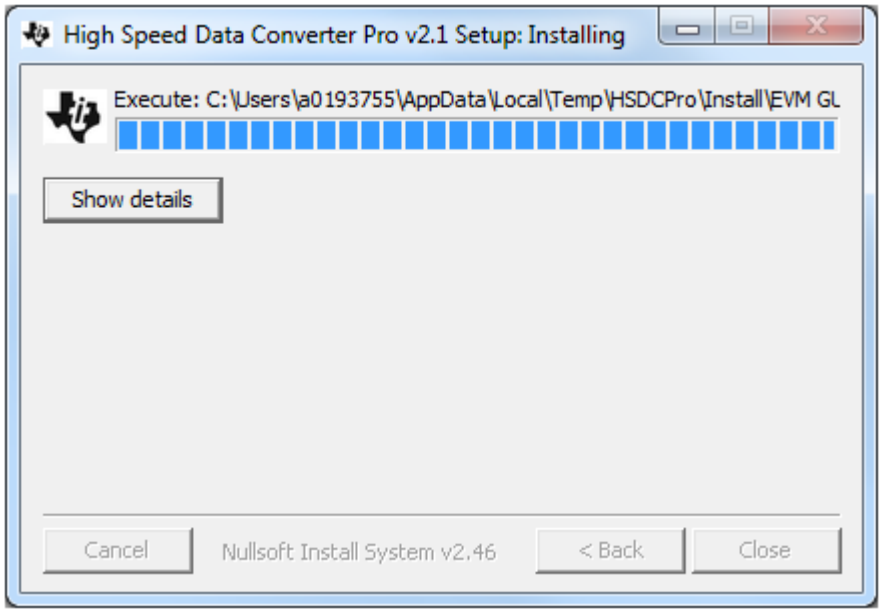


Figure 9. HSDCpro Install (h)

- As shown in Figure 10, a computer restart might be requested depending on whether or not the PC already has the National Instruments' MCR installer. If requested, hit the *Restart* button to complete the installation.

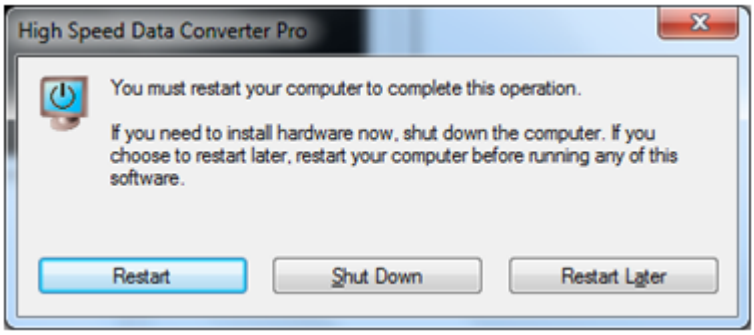


Figure 10. HSDCpro Install (i)

2.2 PGA5807 EVM GUI Installation

From the Texas Instruments website, www.ti.com, search for PGA5807EVM. Clicking on the hyperlink in the table will lead to another link titled **PGA5807 GUI Installer, v1.0**. Click on this link to download and save the zipped file (slac571.zip).

- Unzip the folder and run the *Setup.bat* file as administrator by right clicking on it and selecting *Run as administrator* as shown in Figure 11.

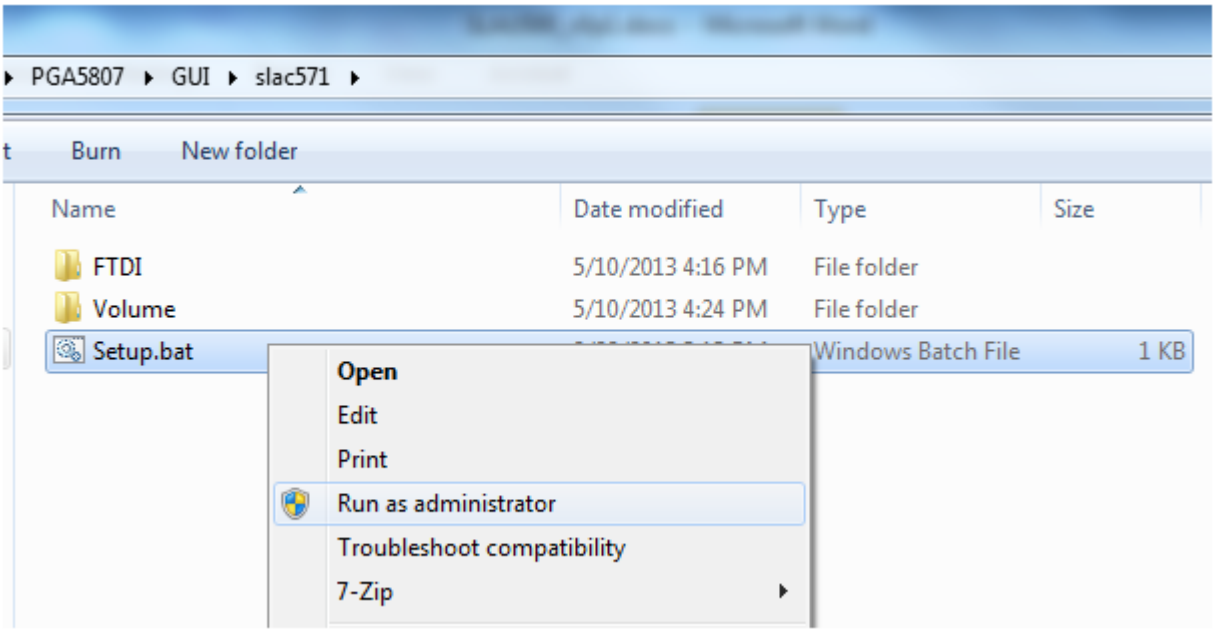


Figure 11. PGA5807 GUI Install (a)

- Set the destination directories for the PGA5807 GUI installation or leave as default and press the *Next* button as shown in Figure 12.

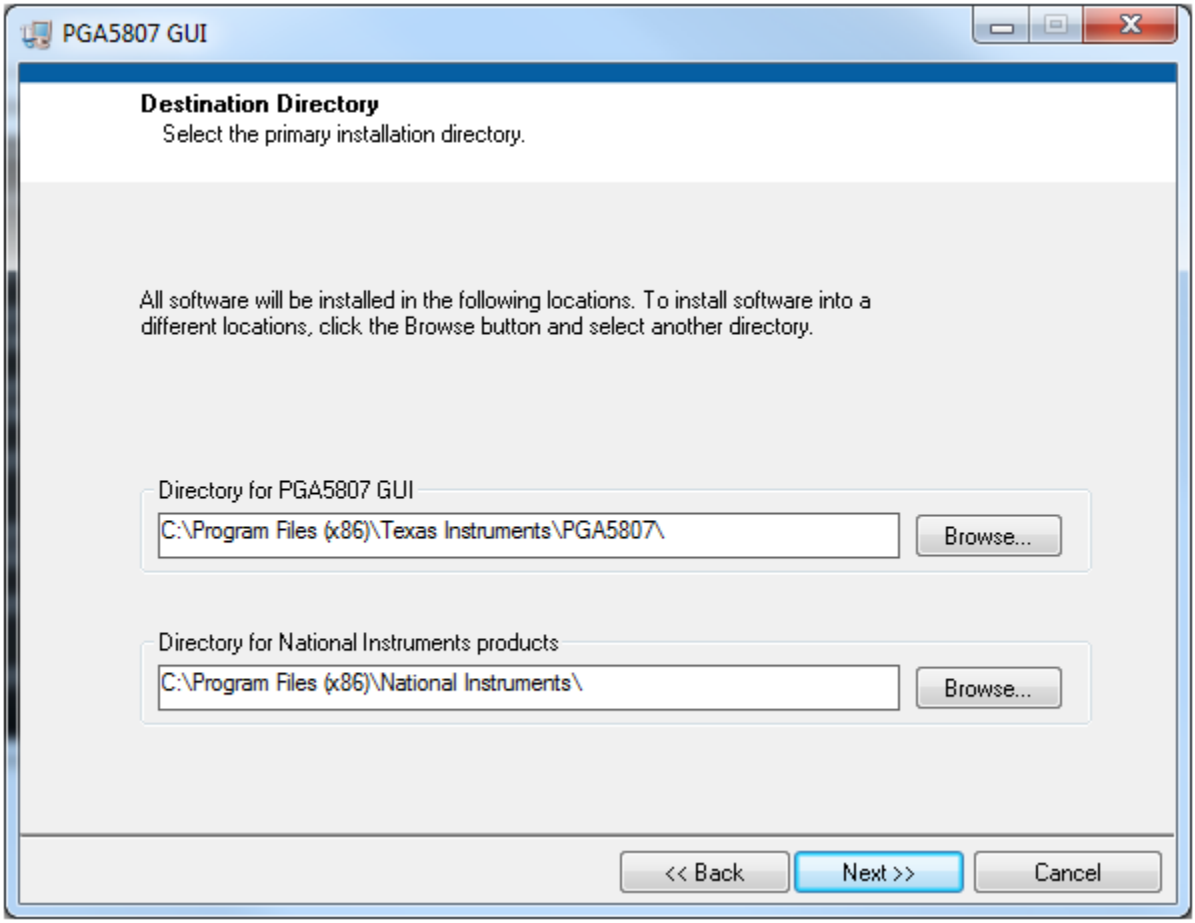


Figure 12. PGA5807 GUI Install (b)

- Read the License Agreement from Texas Instruments and select the *I accept the License Agreement* button and then press the *Next* button as shown in Figure 13.

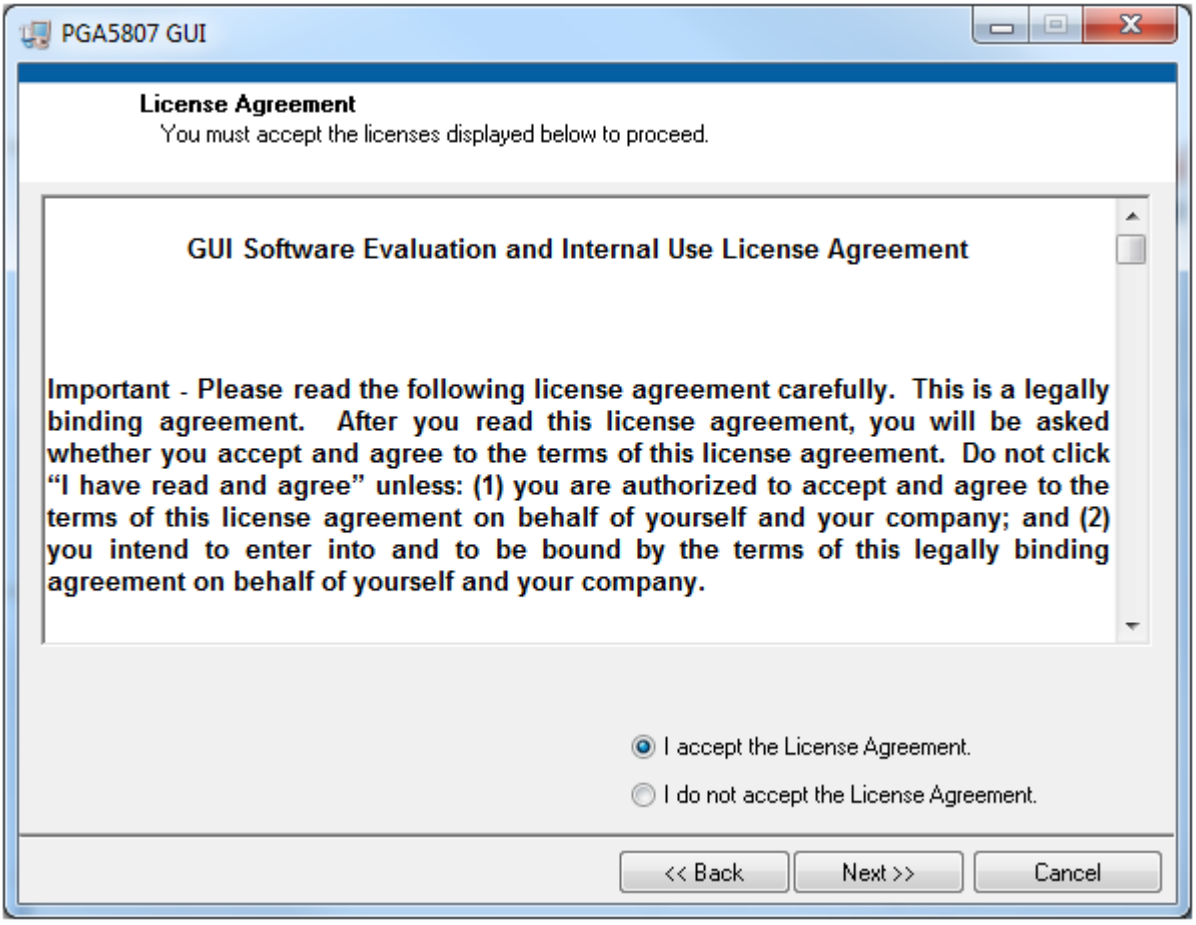


Figure 13. PGA5807 GUI Install (c)

- Read the License Agreement from National Instruments and select the *I accept the License Agreement* button and then press the *Next* button as shown in Figure 14.

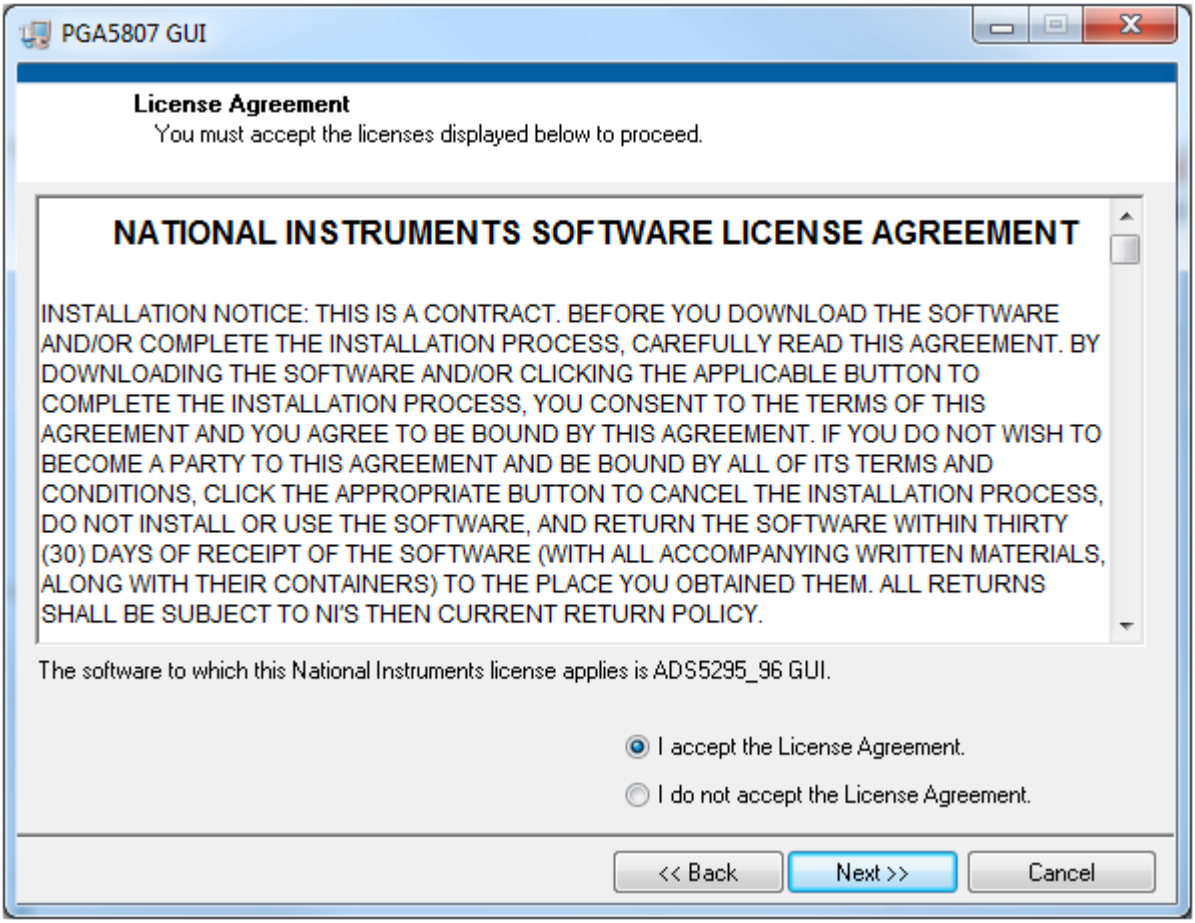


Figure 14. PGA5807 GUI Install (d)

- To begin the installation, press the *Next* button as shown in Figure 15.

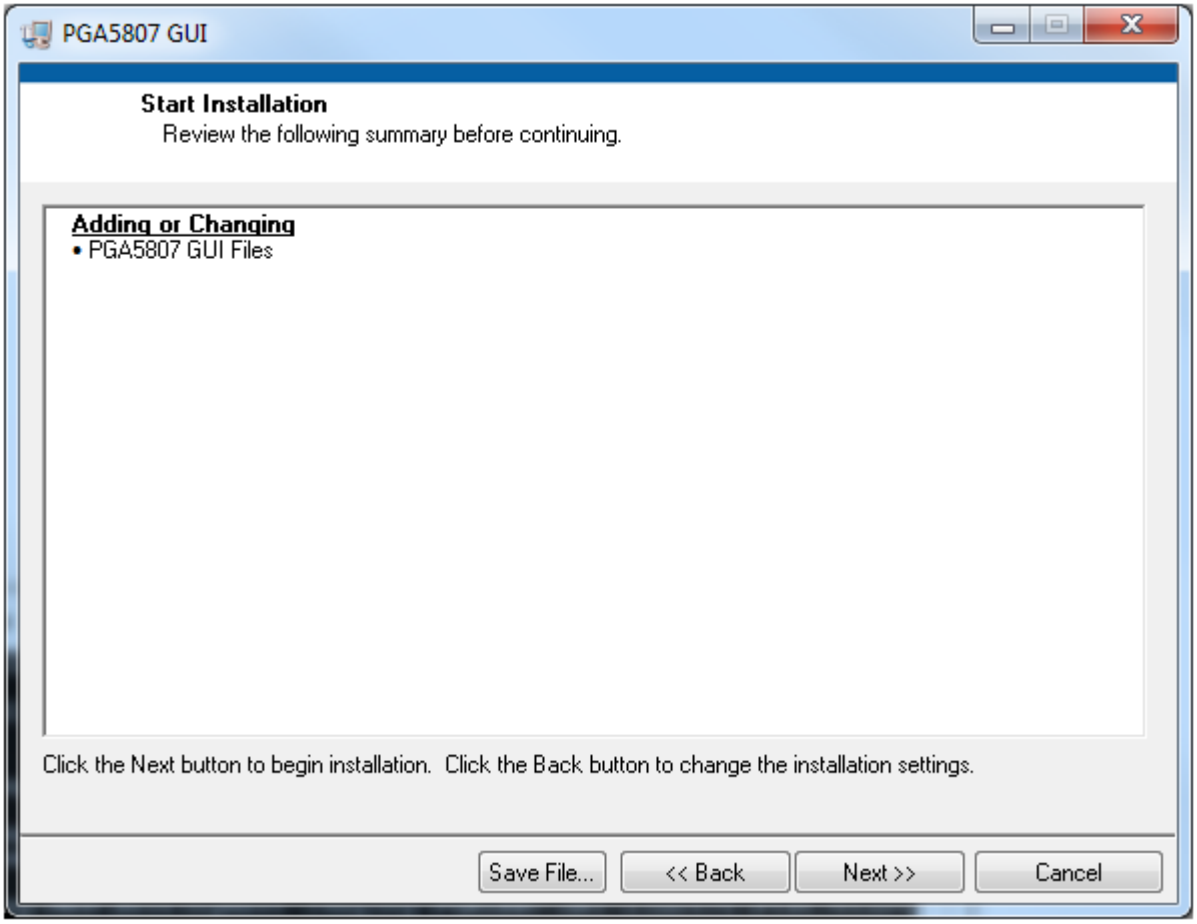


Figure 15. PGA5807 GUI Install (e)

- The window shown in Figure 16 should appear showing that installation is in progress.

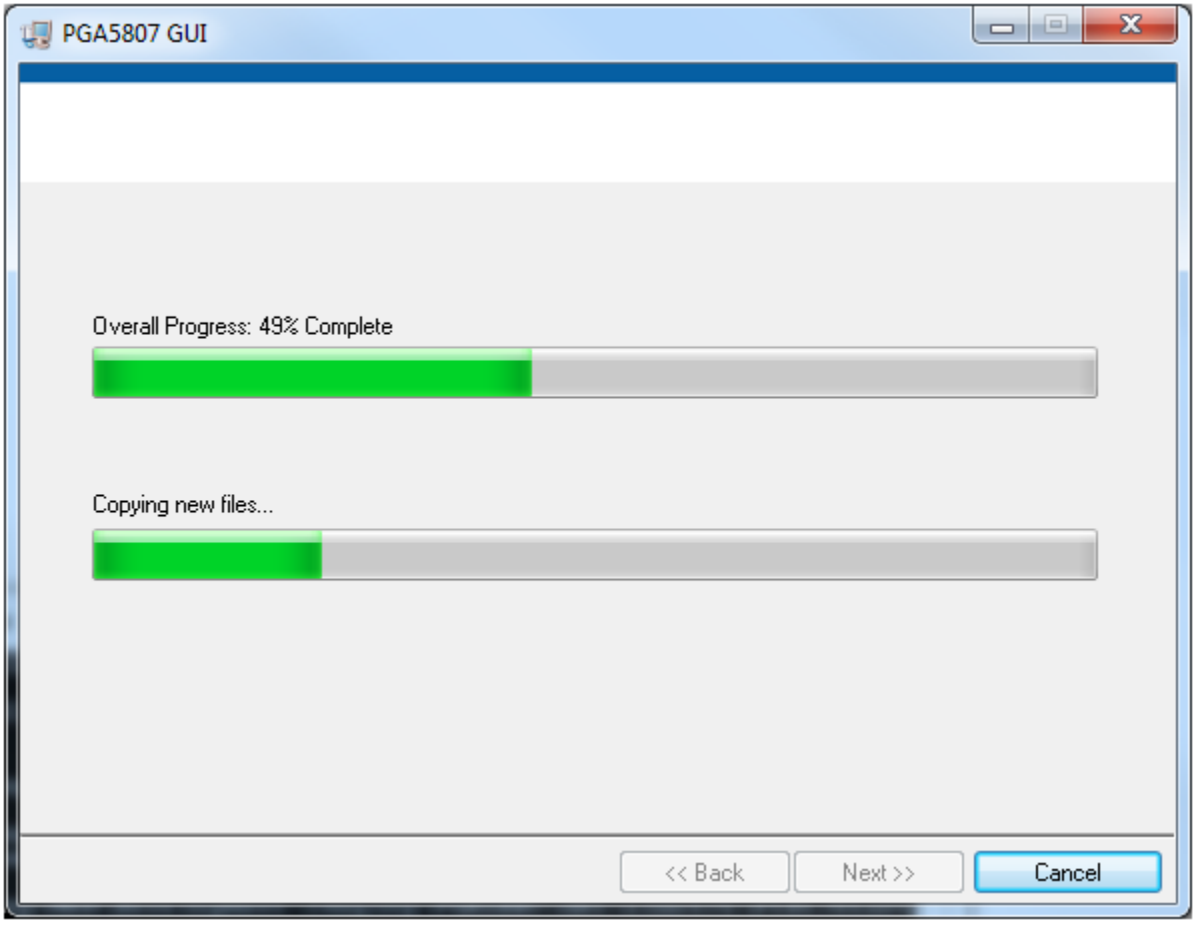


Figure 16. PGA5807 GUI Install (f)

- Upon completion of the installation, the window in Figure 17 appears. Press the *Finish* button to continue.

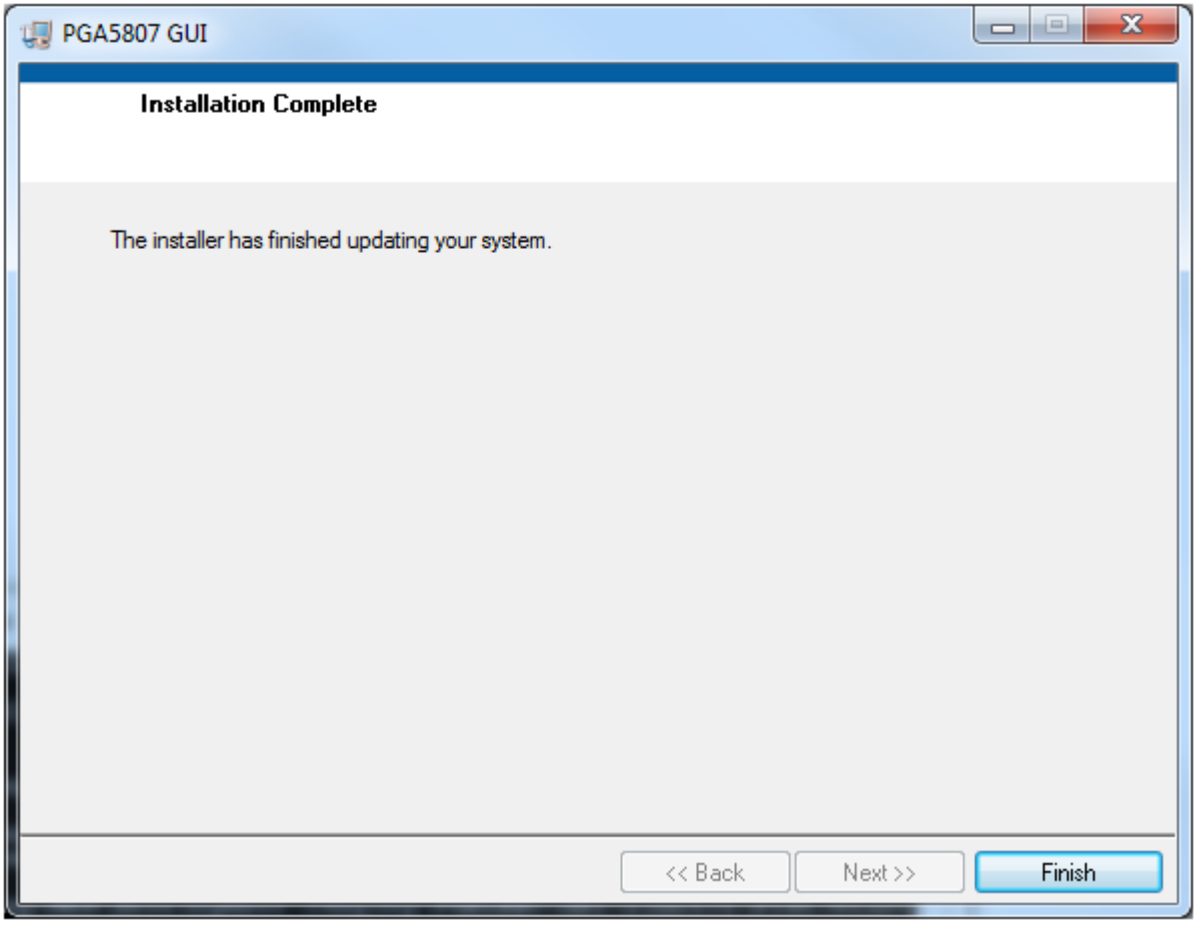


Figure 17. PGA5807 GUI Install (g)

3 Hardware and EVM Setup for Testing PGA5807

This section outlines the external connections required for PGA5807 EVM as well as the default configuration of the EVM's 3-pin headers and 0-Ω jumper resistors with an explanation of configuration options. The EVM is delivered with three unique signal path configurations available to the user with only header changes required to the EVM. These configurations are PGA5807+ADS5296 (PGA+ADC), PGA5807 only (**PGA Input/Output**), and ADS5296 only (ADC Input). Figure 18 highlights which SMAs are to be used for each configuration. (*Note: The PGA5807 output channels do not numerically match the input channels of the ADS5296, hence, there is a mapping from one to the other. The silkscreen designators are named in such a way as to describe the mapping. For instance, the signal input to channel 1 of the PGA5807 at SMA **J10** will be captured on channel 5 at the output of the ADC, hence, the designator name for SMA **J10**, **CH5 (PGA_CH1)**.*)

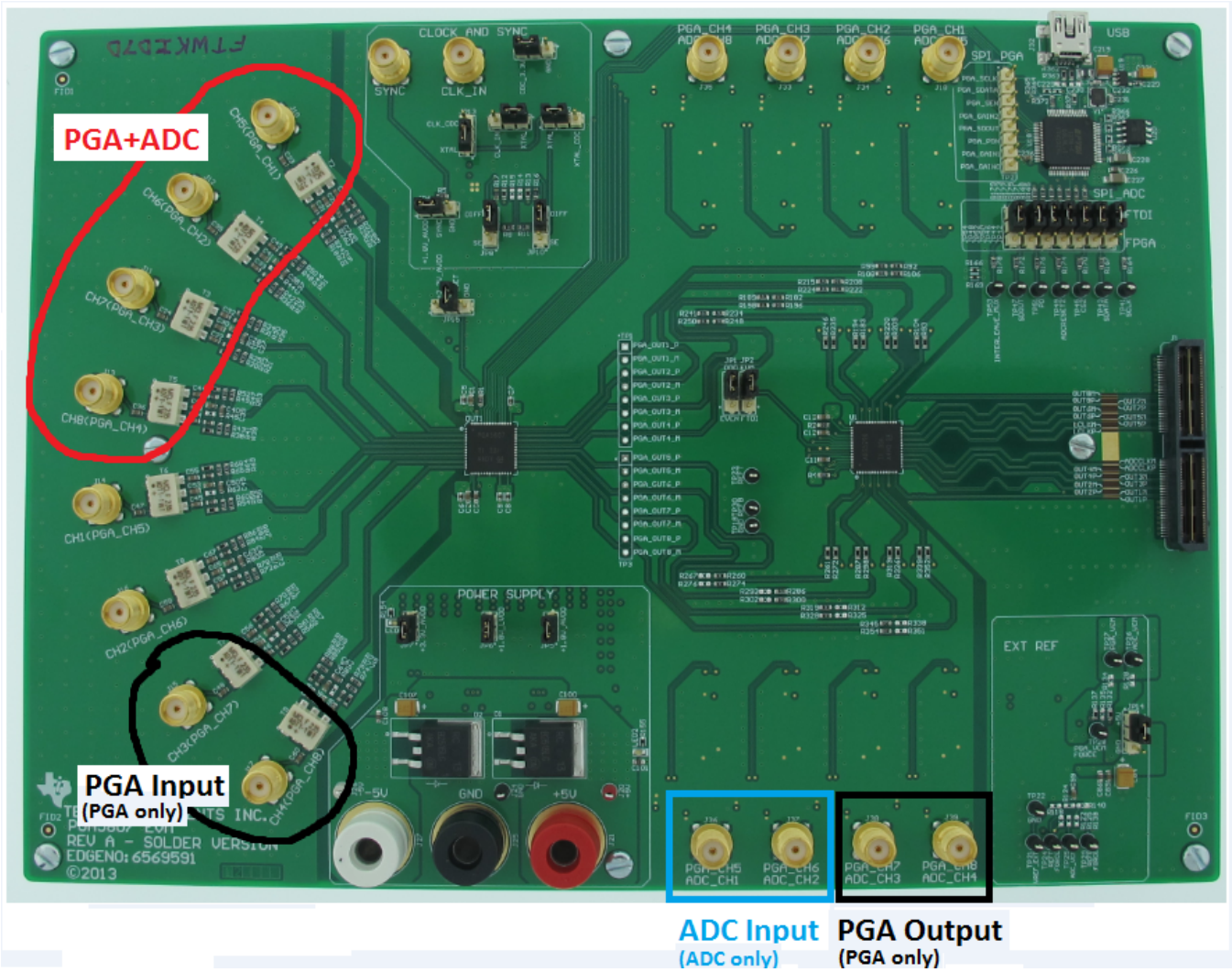


Figure 18. PGA5807 EVM Configuration

3.1 External Connections

The connections shown in Figure 19 should be made for proper hardware setup (*Note: Testing the LVDS interface between the PGA5807 EVM and the TSW1400 EVM can be performed by testing the ADS5296 which comes installed on the PGA5807 EVM. Using a RAMP test pattern function that is generated within the ADS5296 along with the on-board 80-MHz crystal oscillator (XTAL) that provides the ADC sampling clock, the LVDS interface can be tested with no signal generators required. This configuration is only recommended for testing the RAMP function as low phase noise filtered signal sources must be provided to the ADC clock input and the ADC analog inputs or PGA5807 analog inputs for measuring device performance.* ***Also, the on-board XTAL providing the sampling clock to the ADC provides a 3.3-V signal at its output. This signal level exceeds the maximum voltage rating of the ADS5296 clock input port. Therefore, if EVM jumpers are configured such that the ADC clock port is single-ended, the clock input signal will exceed the maximum voltage rating of the device. This is not a problem for evaluation purposes but could have long-term reliability consequences on the device and is, therefore, not a recommended implementation)***.

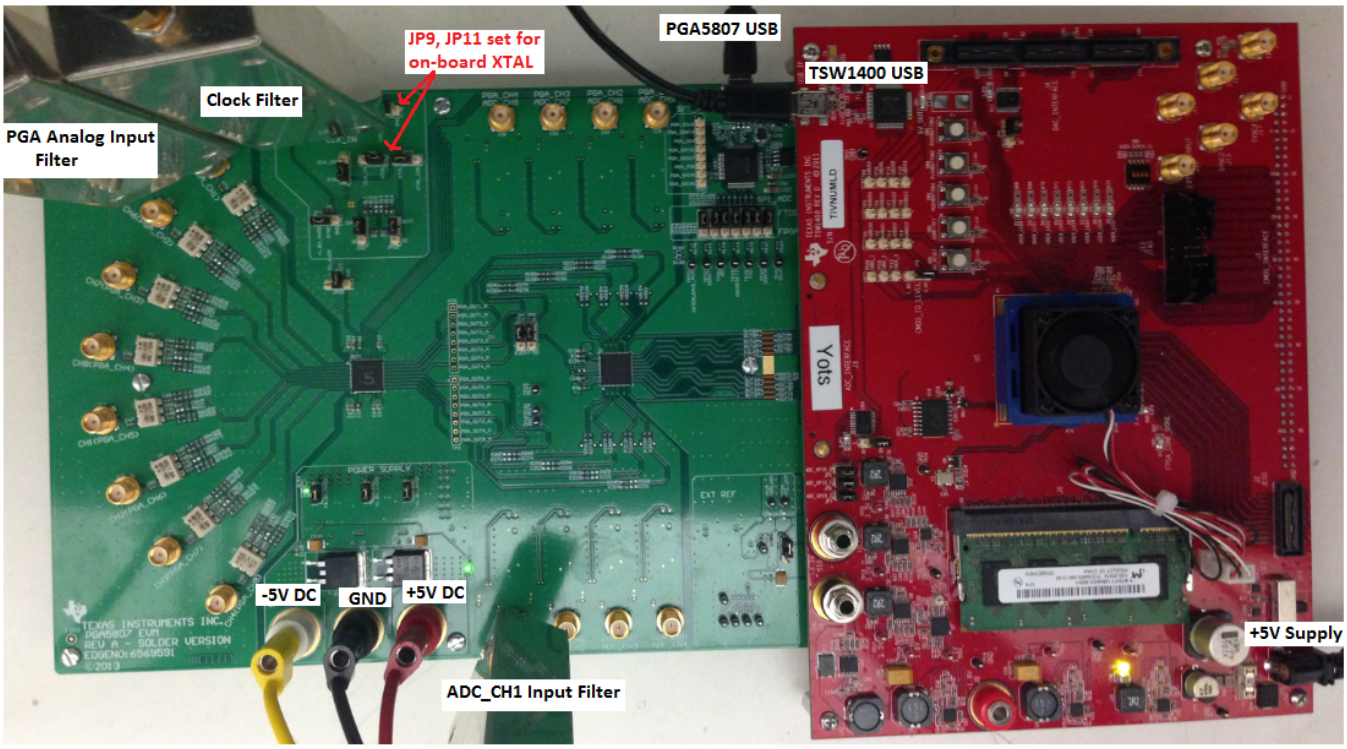


Figure 19. TSW1400 and PGA5807 Sptup

1. Mate the TSW1400 EVM at connector **J4** to the PGA5807 EVM at connector **J1** through the high-speed ADC interface connector.
2. Connect the DC +5-V output of the provided AC-to-DC power supply to **J12 (+5V_IN)** of the TSW1400 EVM and the input of the power supply cable to a 110–230 VAC source.
3. Connect +5-V DC power supply leads to connectors **J21 (+5V)** and **J26 (GND)** of the PGA5807 EVM.
4. Connect –5-V (negative) DC power supply leads to connectors **J26 (–5V)** and **J26 (GND)** of the PGA5807 EVM. (*Note: a negative supply is only needed for testing the PGA5807 in stand-alone mode where the output of the PGA5807 can be monitored at the output of on-board op-amps.*)
5. Connect the USB cable from the PC to **J32 (USB)** of PGA5807 EVM
6. Connect the USB cable from the PC to **J5 (USB_IF)** of the TSW1400 EVM. (*Note: it is recommended that the PC USB port be able to support USB2.0. If unsure, always chose the USB ports at the back of the PC chassis over ones located on the front or sides.*)
7. Supply an ADC sampling clock signal to the SMA **J5 (CLK_IN)** of the PGA5807 EVM for the ADS5296 but disable the output as the initial RAMP test does not require this clock (that is, +5dBm, 80MHz).
8. Supply an analog signal to the analog input SMA **J10**, **CH5(PGA_CH1)**, of the PGA5807 EVM (that is, –15 dBm, 5 MHz)
9. Supply an analog signal to the analog input signal to SMA **J36** labeled **PGA_CH5**, **ADC_CH1** (+15 dbm, 5 MHz). (*Note, items 8 and 9 are not required simultaneously and not required at all for the initial testing of a RAMP test pattern. As such, a single signal generator can be shared to supply both input signals*)

3.2 PGA5807 EVM Header Configuration

The PGA5807 EVM is flexible in its configurability through the use of 3 pin headers. The default configuration of the EVM is set to facilitate initial testing requiring minimal bench equipment by providing an 80-MHz ADC sampling clock from an on-board crystal oscillator (XTAL). Table 1 describes the purpose of the 3-pin headers on the EVM while Figure 20 shows the default position. With this configuration, the on-board XTAL is powered and providing an 80-MHz signal to a transformer which, in turn, provides a differential sampling clock to the DUT.

Table 1. PGA5807 EVM Header Configuration

Jumper	Default Configuration	PIN 1 Silkscreen	PIN 3 Silkscreen	Circuit	Description
JP5	short pins	1.8V_AVDD	n/a	Power supply	1.8-V analog power supply for ADS5296
JP6	short pins	1.8V_LVDD	n/a	Power supply	1.8-V digital power supply for ADS5296
JP7	short pins	3.3V_AVDD	n/a	Power supply	3.3-V power supply for PGA5807
JP9	short pins 1-2	XTAL	CLK_IN	Sampling clock	Selects ADC sampling clock source: (1) XTAL OSC. or (3) external source input to SMA J5 CLK_IN
JP11	short pins 1-2	CDC_3.3V	GND	Sampling clock	Selects Power supply for CDC chip and on-board XTAL oscillator: (1) GND or (3) +3.3V
JP12	short pins 1-2	XTAL	XTAL_CDC	Sampling clock	Selects path for XTAL osc. signal: (1) to transformer or (3) to CDC input
JP13	short pins 1-2	XTAL	CLK_CDC	Sampling clock	Selects input source to CDC input: (1) XTAL osc. or (3) external source input to SMA J5 CLK_IN
JP8	short pins 2-3	SE	DIFF	Sampling clock	Selects ADC sampling clock configuration: (1) Single-ended (3) Differential (must match JP8)
JP10	short pins 2-3	SE	DIFF	Sampling Clock	Selects ADC sampling clock configuration: (1) Single-ended or (3) Differential (must match JP10)
JP1	short pins 2-3	EVEN	ODD	INTERLEAVE_MUX	Selects analog input channels to be interleaved: (1) EVEN channels or (3) ODD channels
JP2	short pins 2-3	FTDI	EVM	INTERLEAVE_MUX	Selects source of EVEN/ODD select: (1) GUI control or (3) INTERLEAVE_MUX pin control
JP4	short pins 1-2	1.8V_AVDD	GND	SYNC	ADS5296 SYNC Pin
JP14	short pins 2-3	5V	GND	EXT_REF AMP	Selects power supply for EXT_REF AMP: (1) +5V or (3) GND

Table 1. PGA5807 EVM Header Configuration (continued)

Jumper	Default Configuration	PIN 1 Silkscreen	PIN 3 Silkscreen	Circuit	Description
JP15	Open	3.3V_AVDD	GND	PGA5807 RESET Pin	PGA5807 RESET Pin On-board Control: (1)PGA5807 is controlled by device pin; (3)PGA5807 is controlled by SPI; OPEN->RESET Pin is controlled by GUI"
JP550	short pins 1-2	ADCRESETZ	n/a	SPI	Selects ADS5296 SPI control: (1) GUI control
JP52	short pins 1-2	PD	n/a	SPI	Selects ADS5296 SPI control: (1) GUI control
JP48	short pins 1-2	SDOUT	n/a	SPI	Selects ADS5296 SPI control: (1) GUI control
JP46	short pins 1-2	CSZ	n/a	SPI	Selects ADS5296 SPI control: (1) GUI control
JP42	short pins 1-2	SCLK	n/a	SPI	Selects ADS5296 SPI control: (1) GUI control
JP44	short pins 1-2	SDATA	n/a	SPI	Selects ADS5296 SPI control: (1) GUI control
JP54	short pins 1-2	INTERLEAVE_MUX	n/a	SPI	Selects ADS5296 SPI control: (1) GUI control

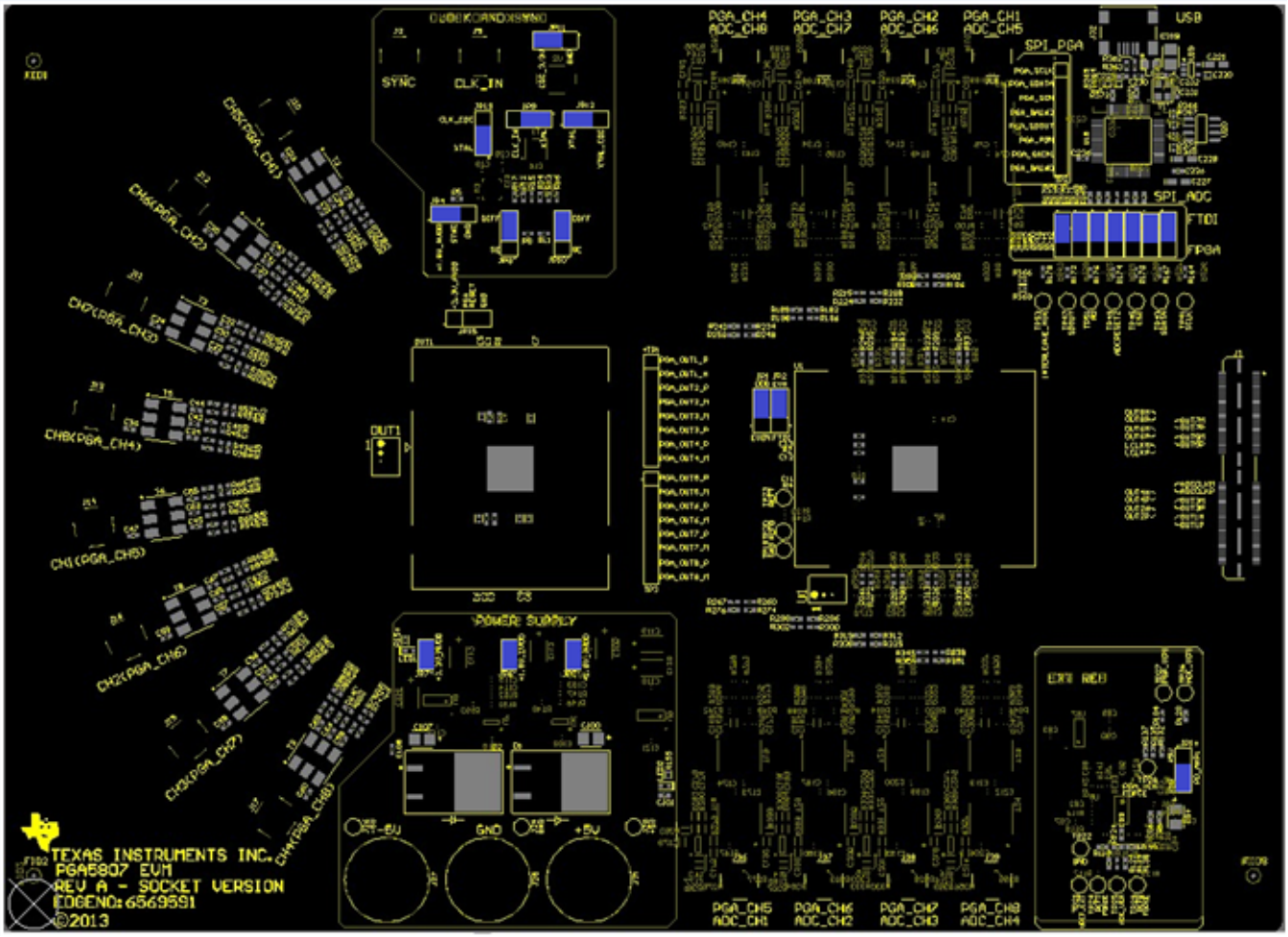


Figure 20. PGA5807 EVM Default Header Configuration

3.3 PGA5807 EVM 0-Ω Jumper Configuration

As described in the beginning of Section 3, the PGA5807 EVM is delivered with three unique signal path configurations: four channels for PGA5807+ADS5296, two channels for PGA5807 only, and two channels for ADS5296 only. Any one of these three configurations can be applied to all eight channels by changing the position of a few 0-Ω jumper resistors. As an example, Figure 21 shows one page of the EVM schematics (see Section 6 for full schematics). The table on the bottom right side of this schematic page shows which 0-Ω resistors must be installed for each configuration. The configuration pictured routes the PGA output from channel 1 to channel 5 of the ADS5296.

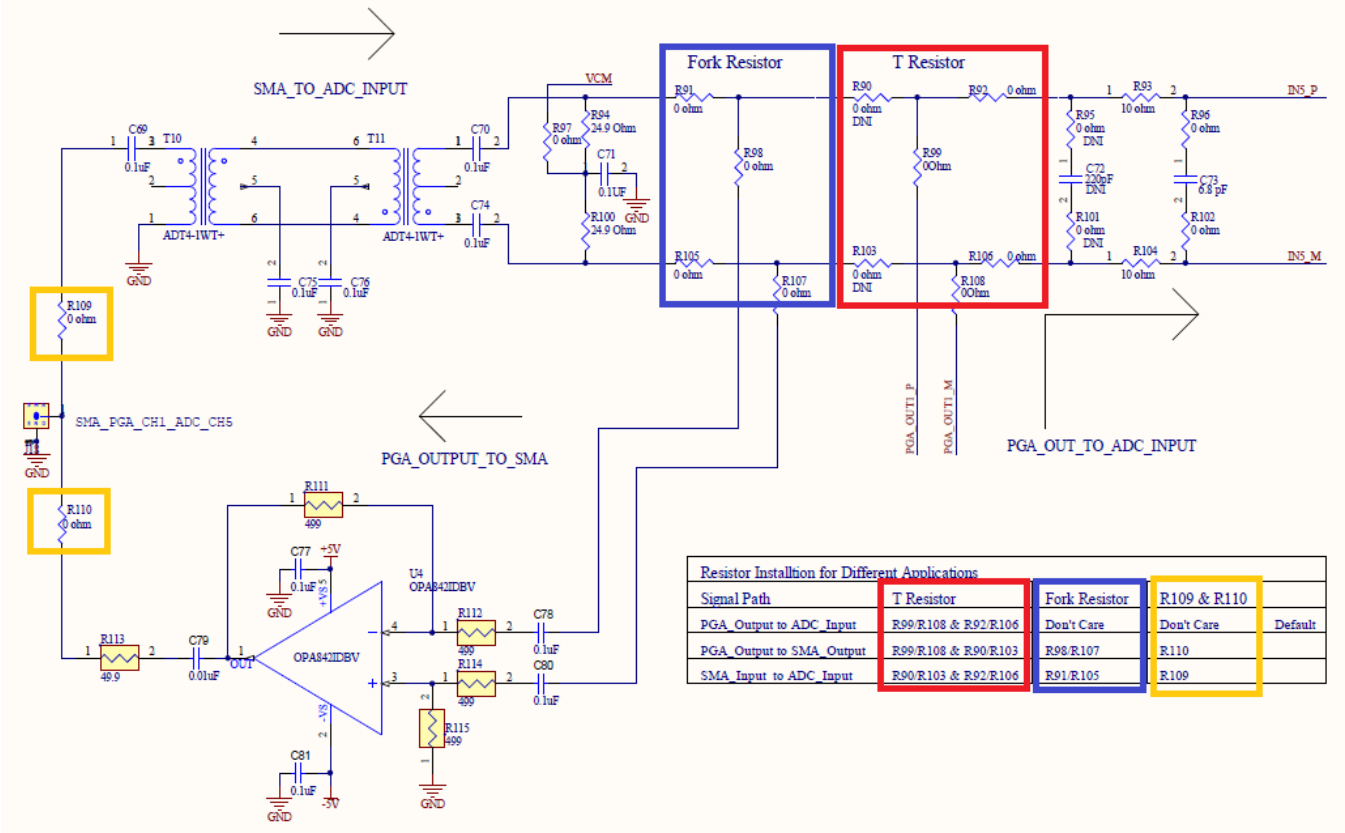


Figure 21. PGA5807 EVM Schematic 0-Ω JUmper Options

4 Testing the PGA5807 EVM

This section outlines the following three test cases with a sub-section dedicated to each case:

- Capturing a RAMP test pattern for ADS5296 only
- Capturing a sinusoidal input for ADS5296 only
- SNR/THD/Gain Test for PGA5807 + ADS5296

Only the minimal software GUI settings required to achieve the above tests will be described in this section. For a detailed explanation of the PGA5807 software GUI and all its features, please see Section 5. For a detailed explanation of the *High Speed Data Converter Pro* software GUI, please consult the TSW1400 User's Guide (SLWU079B), available on the Texas Instruments website.

4.1 TSW1400 and PGA5807 GUI Setup

1. With the setup outlined in Figure 19 established, launch the *High Speed Data Converter Pro* GUI. The GUI should automatically detect the serial number of the TSW1400 EVM, connected as shown in Figure 22. Click on *OK*.

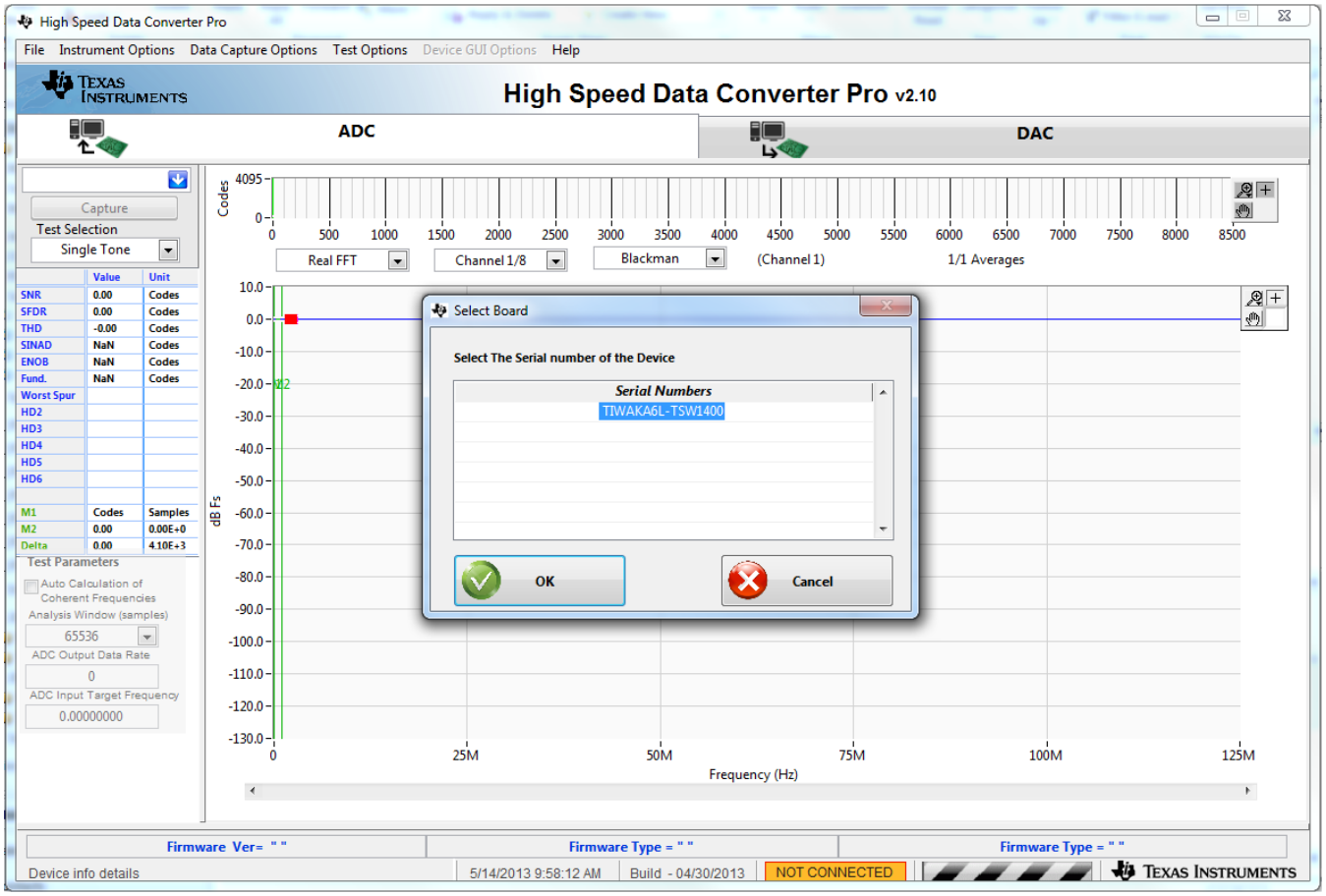


Figure 22. TSW1400 GUI Setup (a)

The message shown in Figure 23 will appear. Click **OK.**

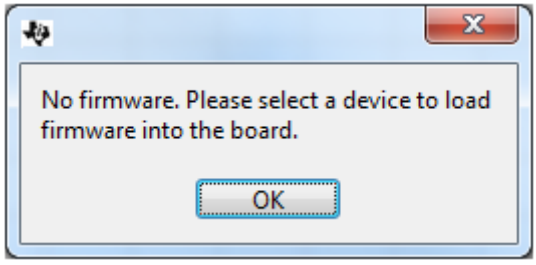


Figure 23. TSW1400 GUI Setup (b)

If instead, the message shown in Figure 24 appears, it indicates that the USB connection to the TSW1400 EVM is not present. Click *OK*, then establish a USB connection and repeat step 1.

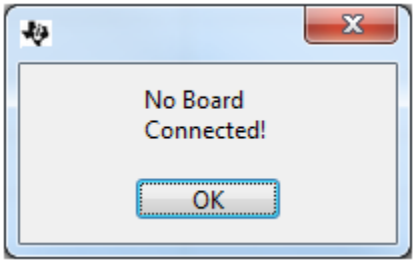


Figure 24. TSW1400 GUI Setup (c)

2. Select a device by clicking on the Blue arrow in the upper left corner of the *HSDCpro* GUI. Scroll down and select *PGA5807* as shown in Figure 25.

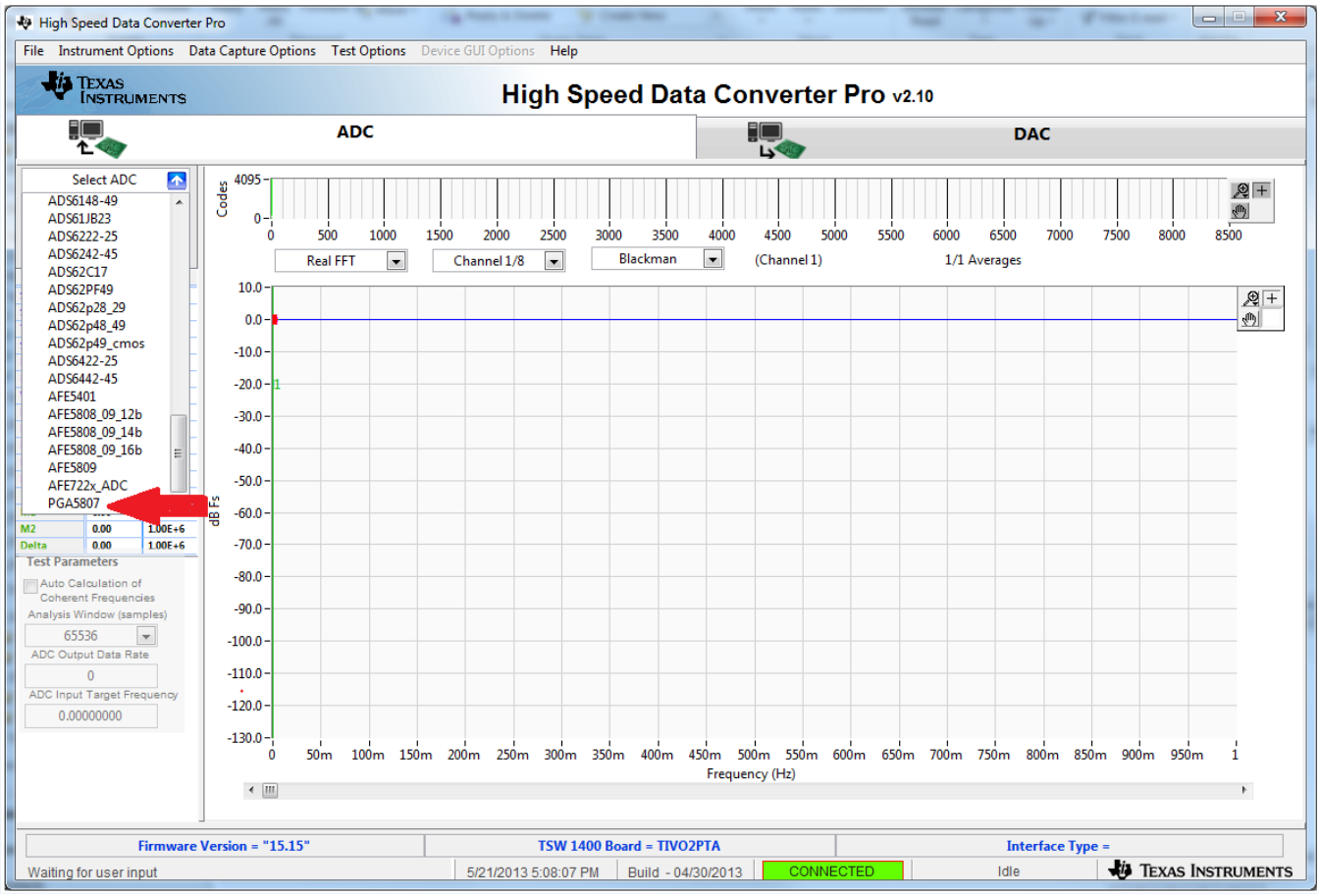


Figure 25. TSW1400 GUI Setup (d)

Click the *Yes* button to update the ADC firmware on the TSW1400 FPGA as depicted in Figure 26.

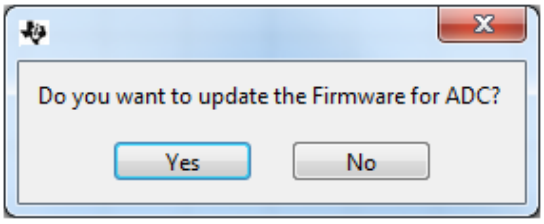


Figure 26. TSW1400 GUI Setup (e)

While the firmware is being loaded into the TSW1400 FPGA, the graphic shown in Figure 27 will appear.

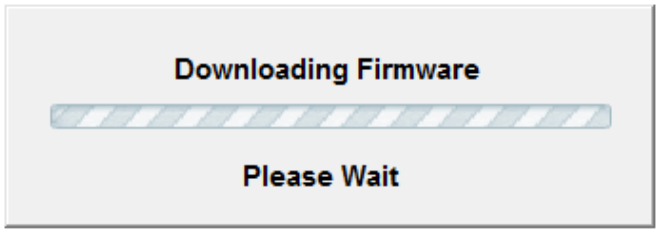


Figure 27. TSW1400 GUI Setup (f)

Once loaded, the plug-in PGA5807 GUI will appear as a new tab within the *HSDCpro* GUI as shown in Figure 28.

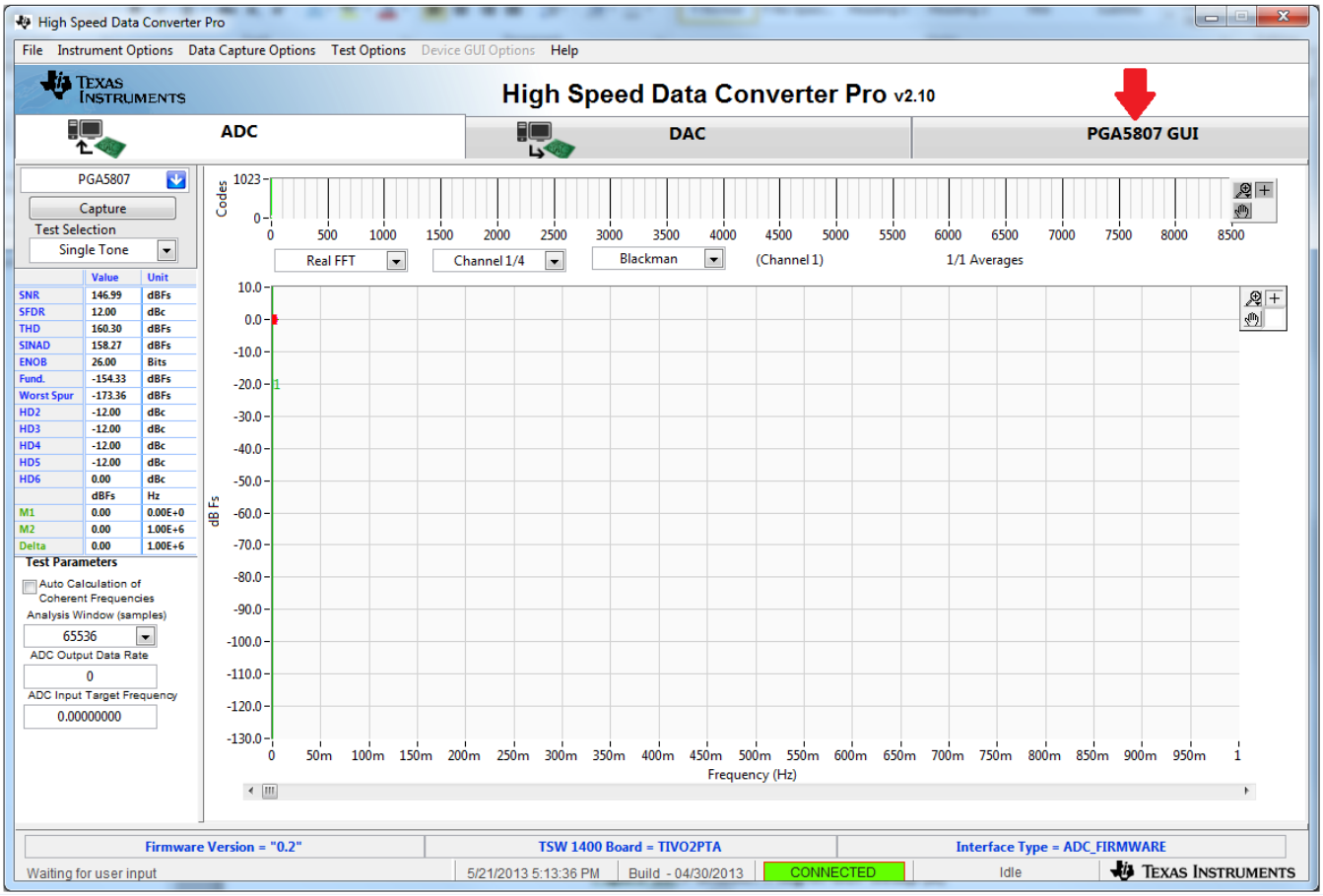


Figure 28. PGA5807 Plug-in GUI Setup

3. Click on the tab *PGA5807 GUI* to view the software GUI for the PGA5807. The GUI consists of three tabs: *Read Me First*, *PGA5807*, and *ADS5296* as shown in Figure 29.

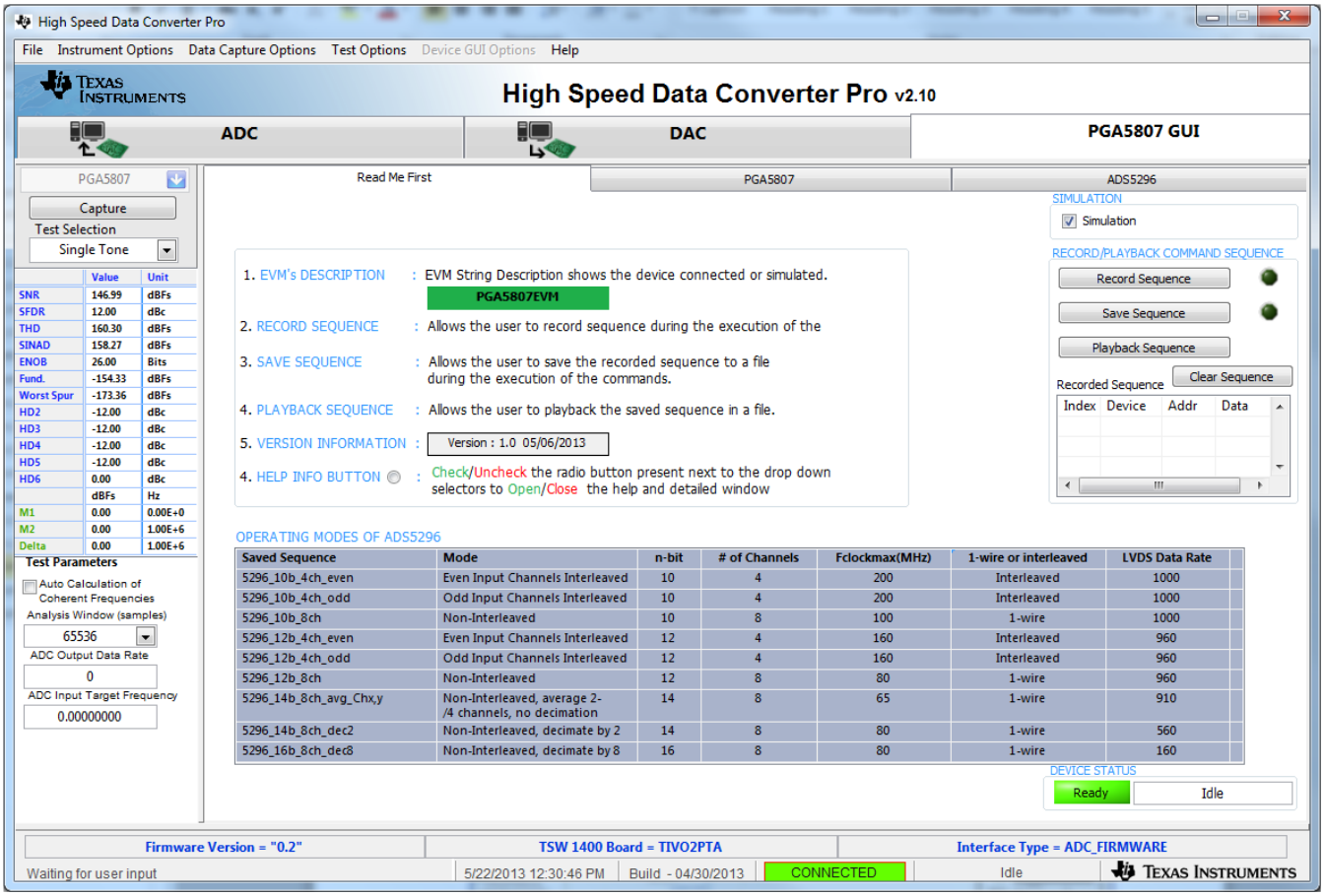


Figure 29. PGA5807 Plug-in GUI Setup (h)

As shown in Figure 30, the *PGA5807* tab contains all controls pertaining to the PGA5807 device installed on the EVM.

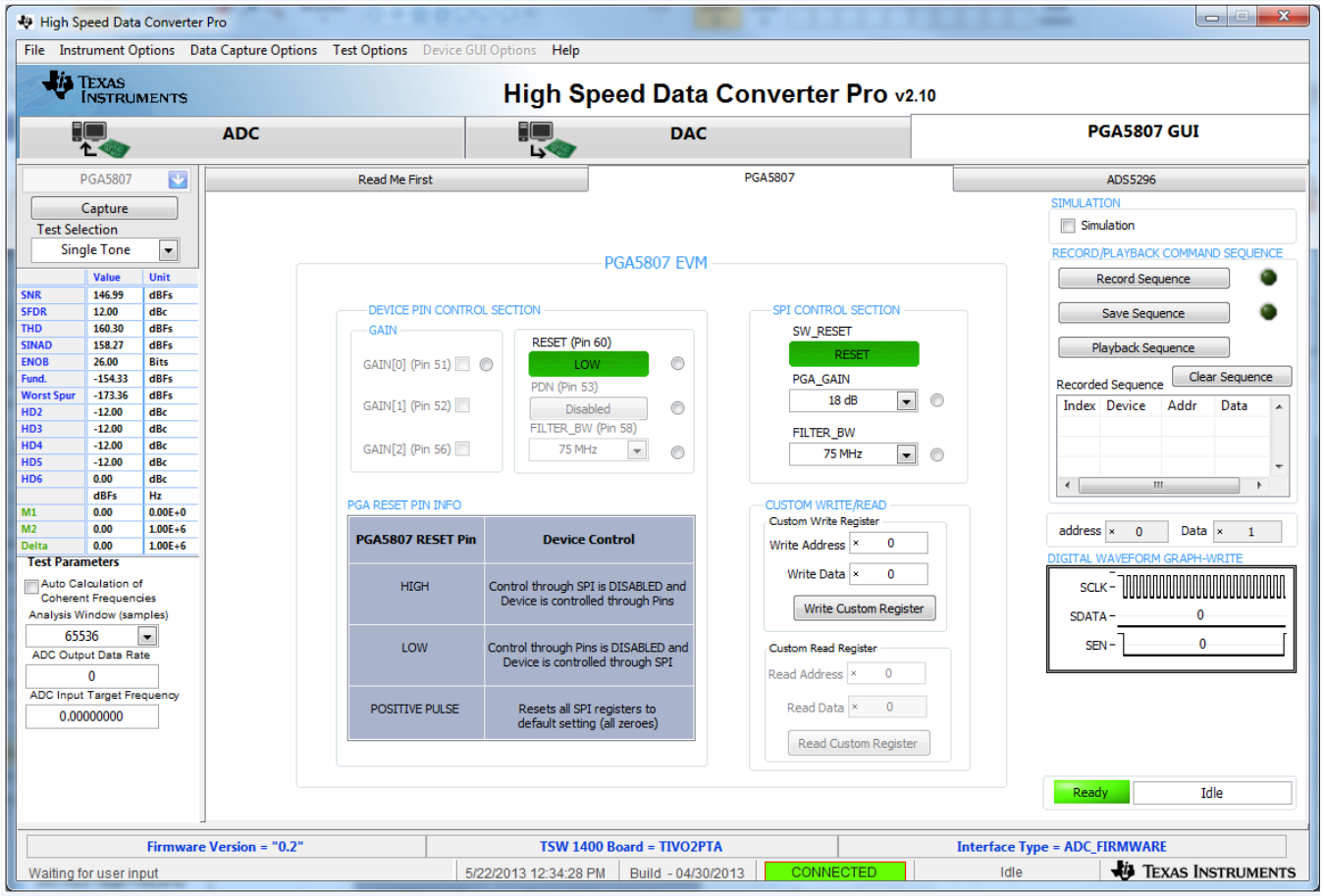


Figure 30. PGA5807 Tab in the PGA5807 GUI

As shown in Figure 31, the *ADS5296* tab contains all controls pertaining to the ADS5296 device installed on the EVM.

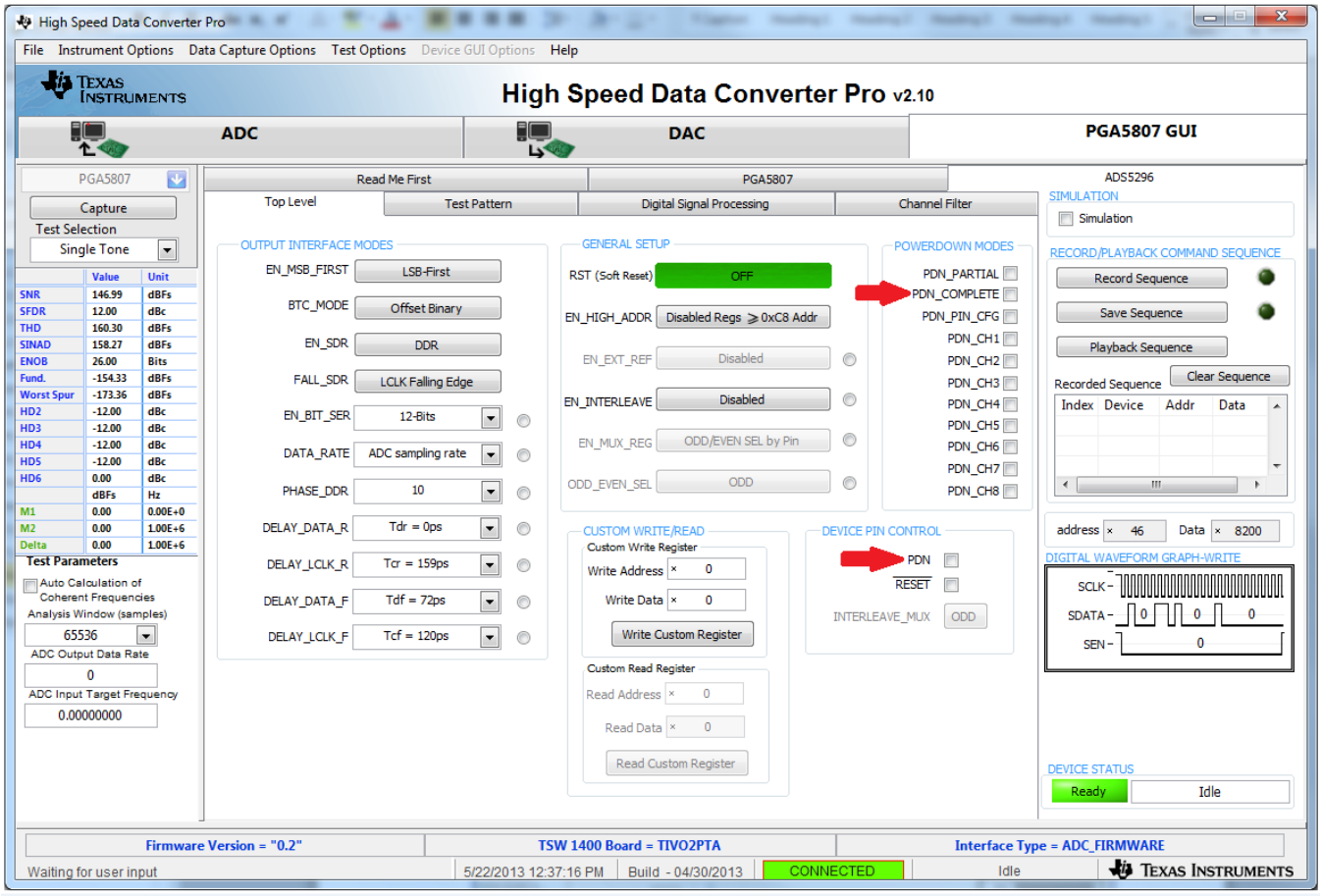


Figure 31. ADS5296 Tab of the PGA5807 GUI

4. Verify that communication between the PGA5807 EVM and the PGA5807 GUI is established by toggling either the **PDN_COMPLETE** checkbox or the **PDN** checkbox, as indicated on Figure 31. Checking either box should make +5-V power supply current drop from ~650 mA – 750 mA to ~350 mA – 450 mA. If the DC current is approximately 480 mA, with both power down boxes unchecked, it indicates that the ADS5296 is not receiving the sampling clock. Please ensure that the 3-pin headers are configured as described in Section 3.2. Before continuing, ensure that both power down boxes are left unchecked. At this point, the GUI is confirmed to be communicating correctly with the EVM and testing can begin.

4.2 Capturing a RAMP Test Pattern

As described in Section 3.1, the LVDS interface between the PGA5807 EVM and the TSW1400 EVM can be tested using the default EVM configuration and minimal bench equipment.

1. Within the *ADS5296* tab, press on the sub-tab labeled *Test Pattern* and select **RAMP PATTERN** within the **TEST_PATT** menu as shown in Figure 32.

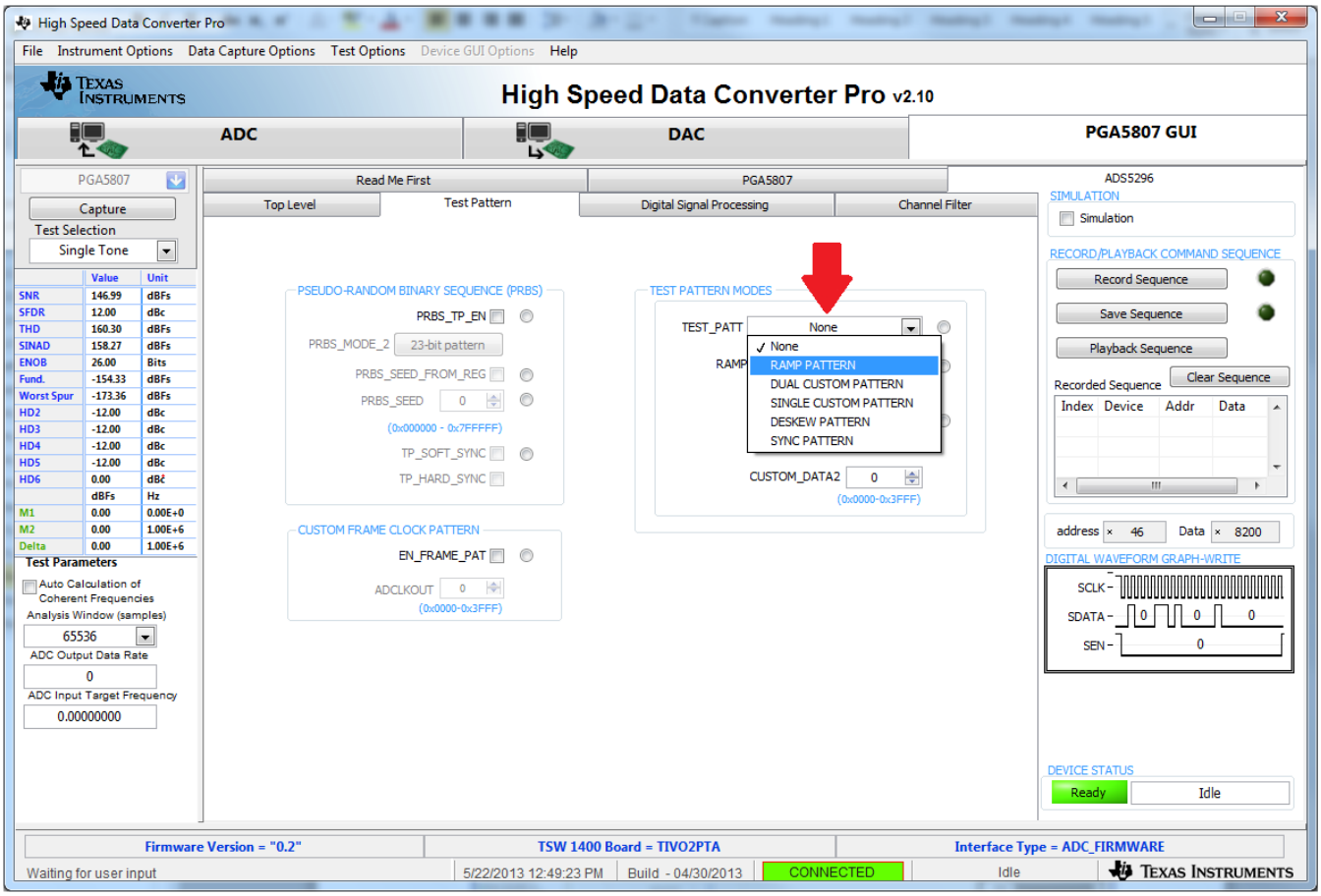


Figure 32. ADS5296 Setup for RAMP Test

2. Perform the following steps highlighted in Figure 33:
   (a) Press the *ADC* tab in *HSDCpro*
   (b) Change the plot type from *Real FFT* to *Codes*
   (c) Enter *80M* in the field labeled *ADC Output Data Rate*
   (d) Press the *Capture* button

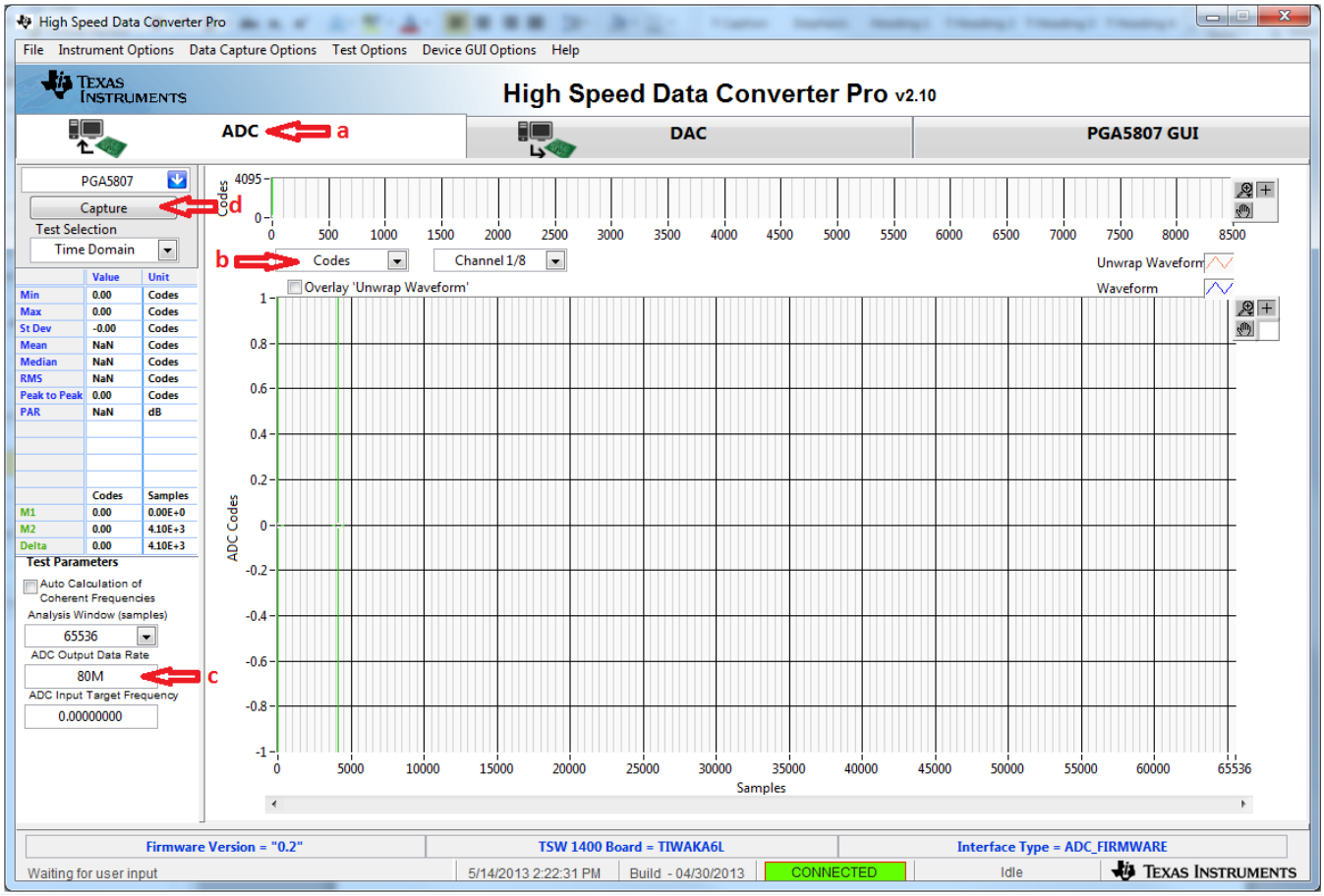


Figure 33. HSDCpro GUI Setup for RAMP Test

3. The saw tooth waveform should be captured and displayed as in Figure 34.

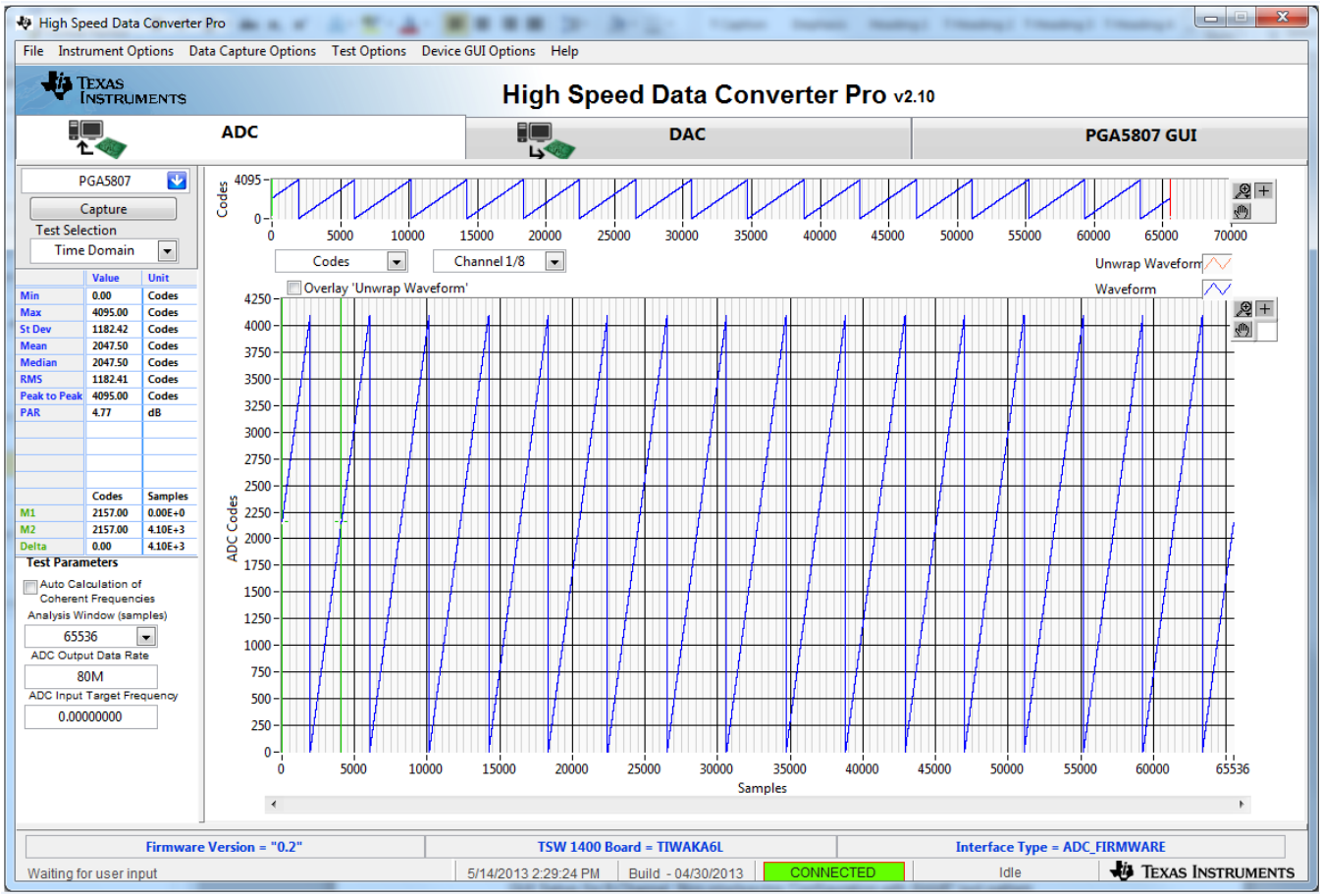


Figure 34. RAMP Capture

4. By default, *Channel 1/8* is the first channel displayed. Use the drop-down menu shown in Figure 35 to view all 8 channels and confirm that a saw tooth waveform has been captured. Also confirm, in the menu to the left side, that the min code is 0 and the max code is 4095, corresponding to a 12-bit ADC.

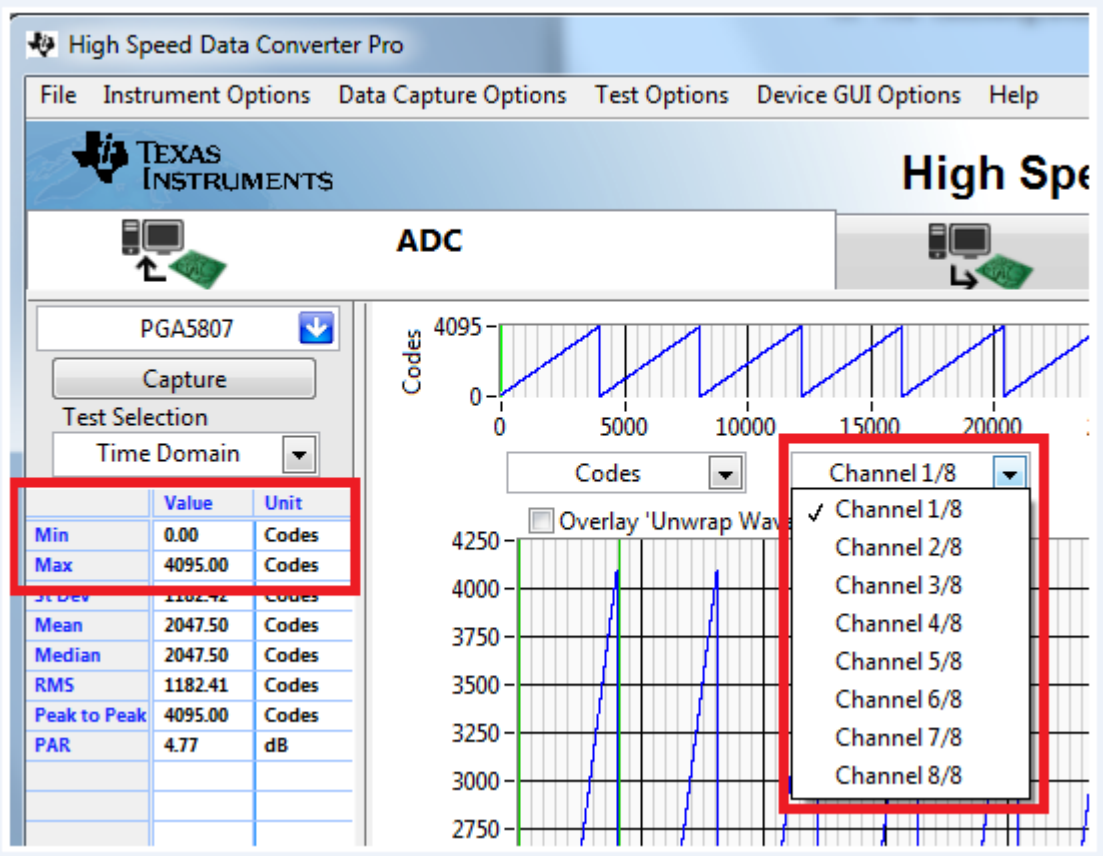


Figure 35. RAMP Capture by Channel

5. Zooming into the waveform, as shown in Figure 36, is recommended to ensure that the RAMP waveform increments 1 ADC code for each subsequent sample.

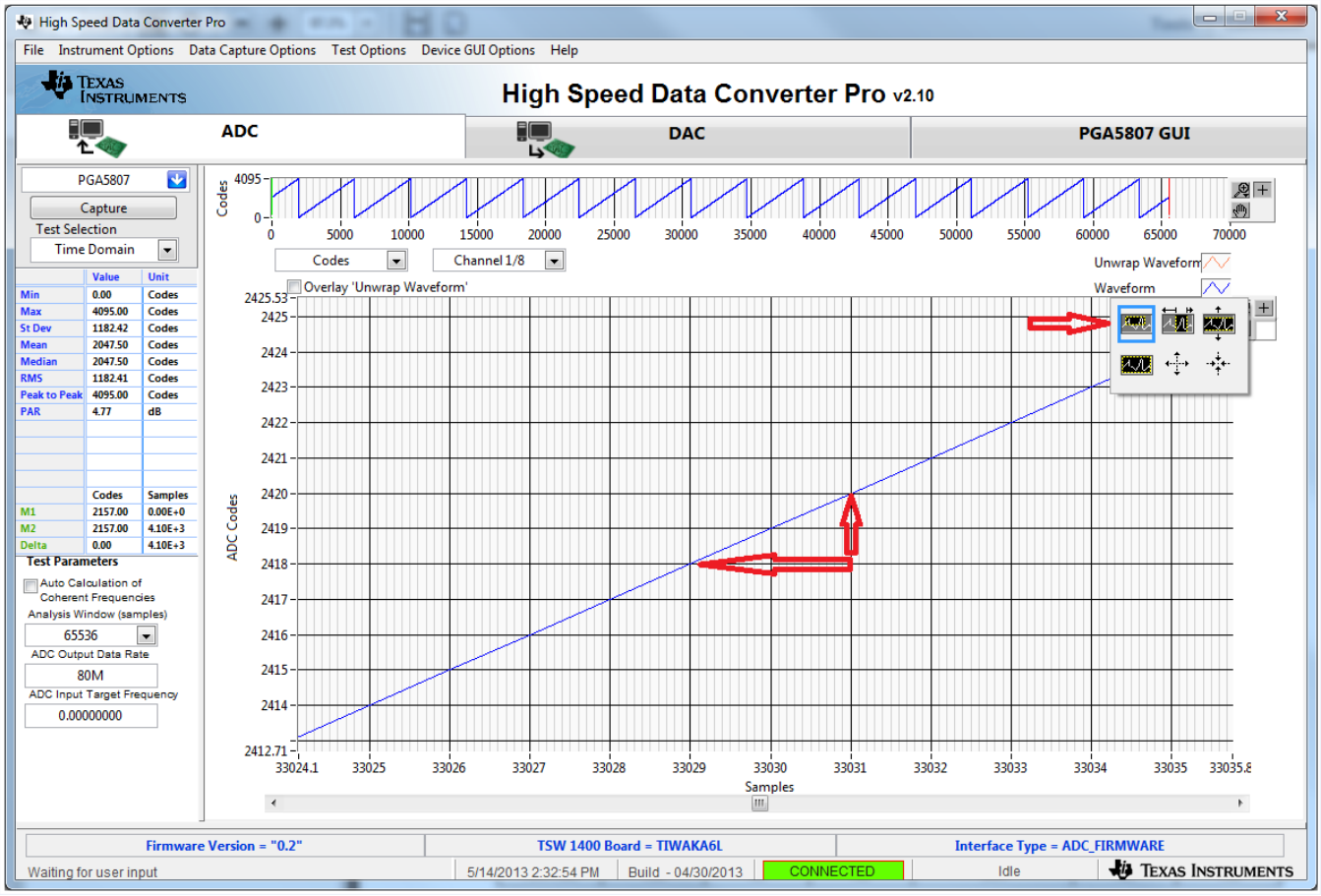


Figure 36. Zoom on RAMP Capture

6. Reset the ADS5296 so that the RAMP test pattern is off as shown in Figure 37.

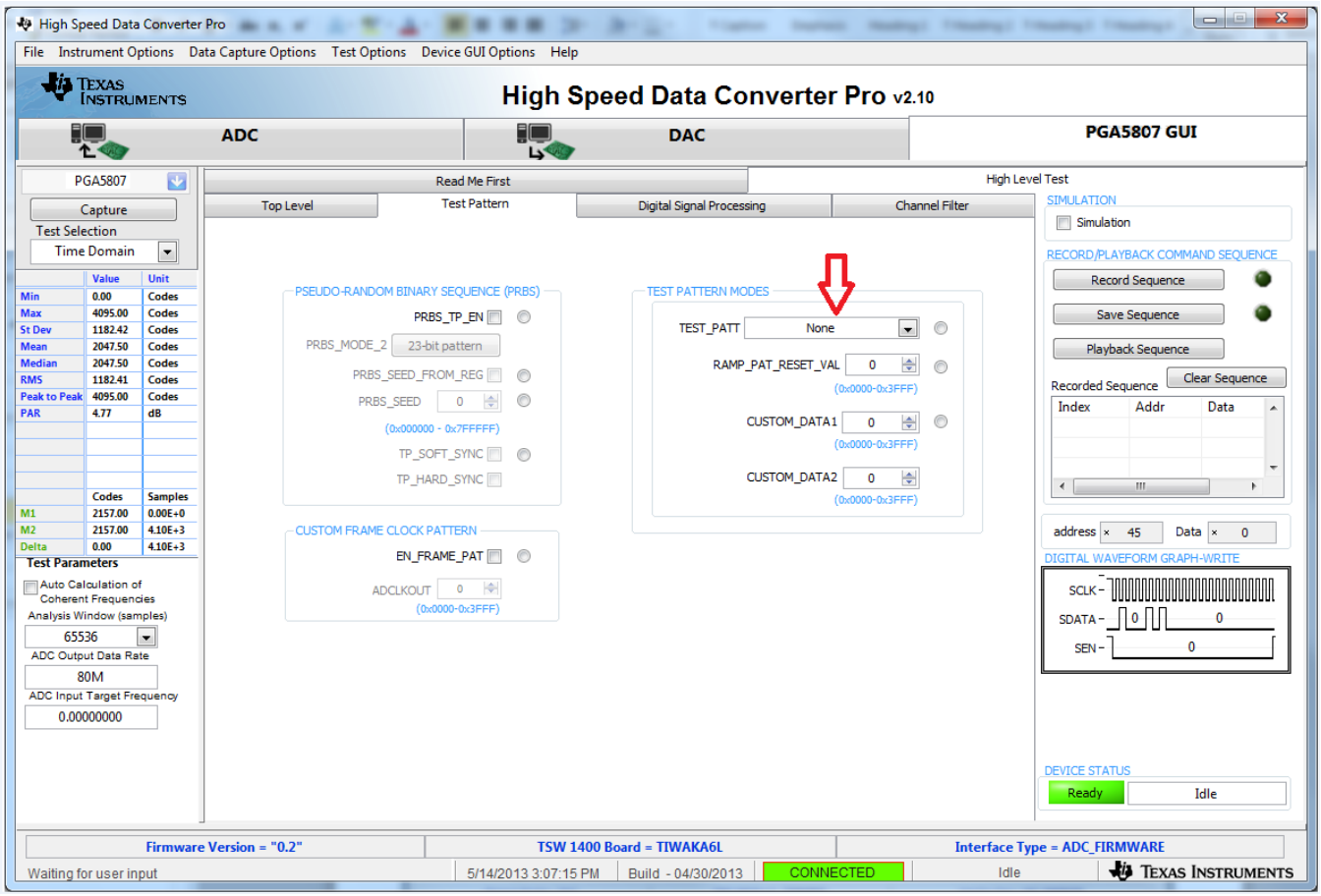


Figure 37. Turn off RAMP Test Pattern

4.3 Capturing Sinusoidal Input for ADS5296 Only

This section describes the necessary steps to reconfigure the EVM and test setup for capturing a sinusoidal input the ADS5296.

1. The RAMP test described in Section 4.2 was performed using an 80-MHz on-board crystal oscillator (XTAL) for the sampling clock. This clock cannot be used to measure performance of the device as it is not phase locked to the input signal. The XTAL should be disabled by moving jumper **JP11** from the position labeled **CDC_3.3V** to the position labeled **GND** in the silkscreen. Also, **JP9** must change position from **XTAL** to **CLK_IN** in the silkscreen to enable the SMA **J5 CLK_IN**. Figure 38 and Figure 39 show the jumper positions before and after this change, respectively.

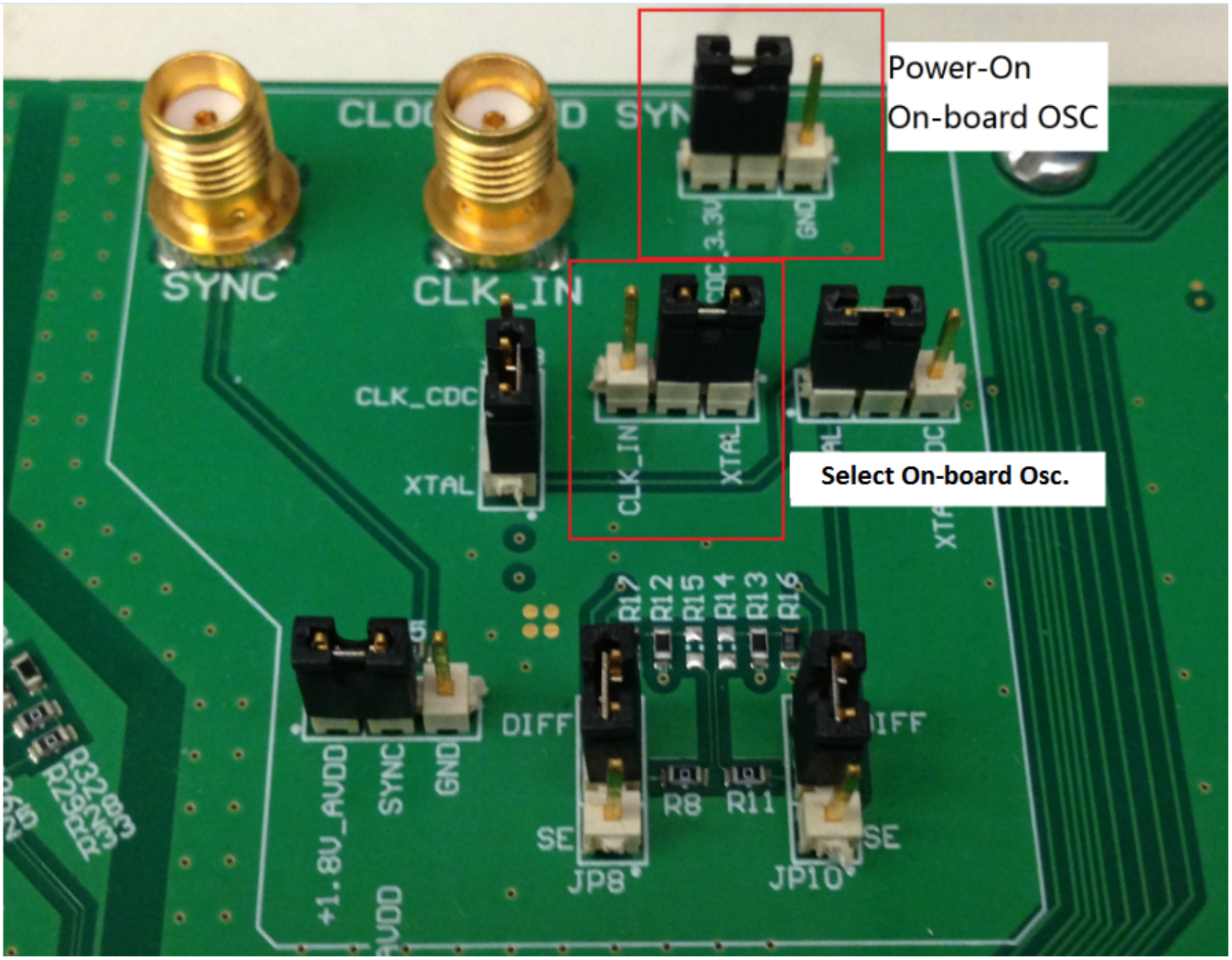


Figure 38. Jumper JP11 and JP9 Positions for Enabled XTAL (default)

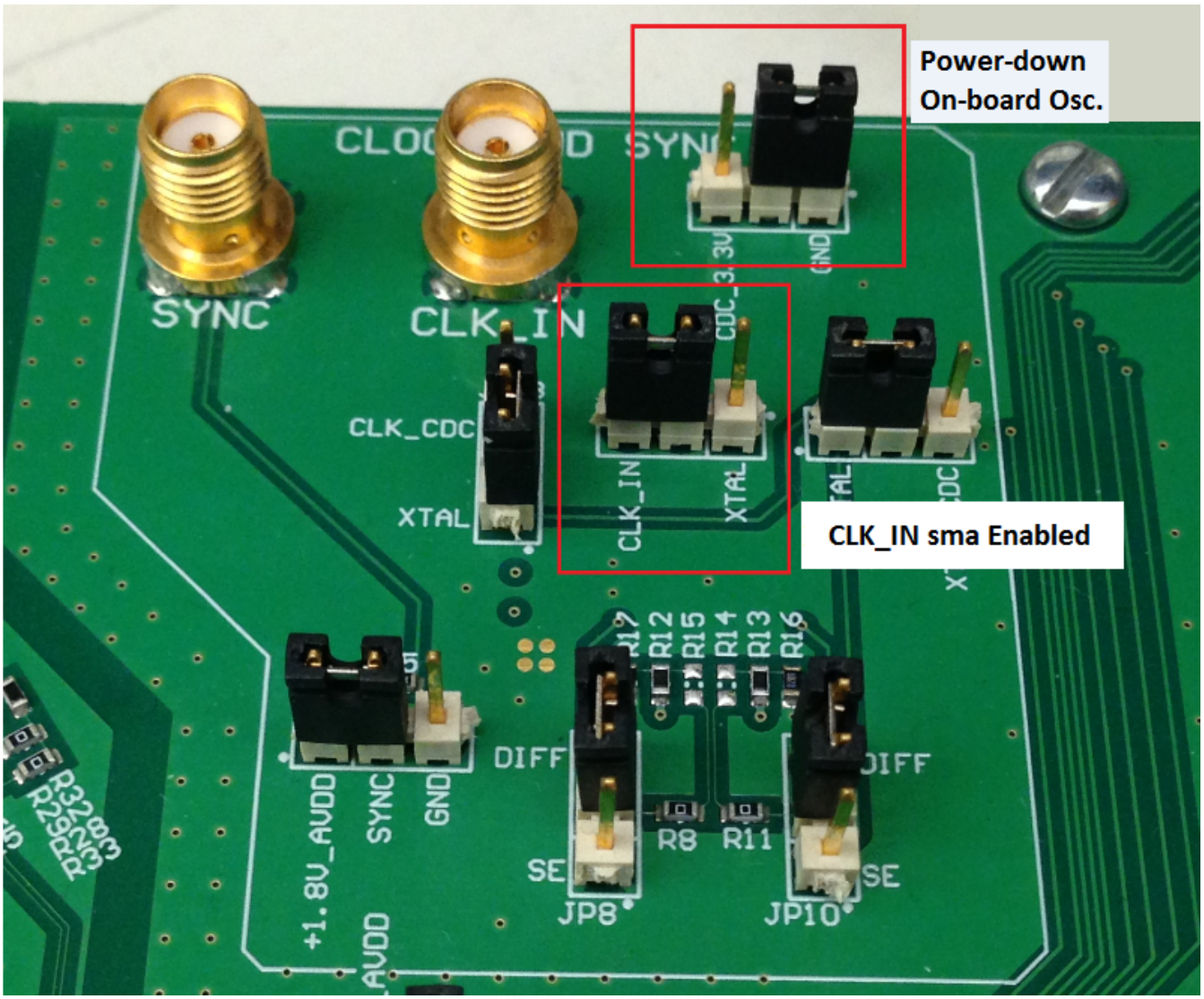


Figure 39. Jumper JP11 and JP9 Positions for Disabled XTAL

2. With the setup established in Figure 40, perform the following steps:
   (a) Enable the signal generator providing the sampling clock to SMA **J5** labeled **CLK_IN** (+5 dBm, 80 MHz)
   (b) Enable the signal generator providing the input signal to SMA **J36** labeled **PGA_CH5, ADC_CH1** (+15 dbm, 10 MHz). For high-performance results the instrument should have low phase noise and low harmonic distortion. In addition, a filter is recommended on the input.
   (c) The two signal generators in items (a) and (b) above should be phase locked so that coherency is established. This is achieved connecting the two via a BNC cable. One instrument will provide 10-MHz output while the other instrument will receive 10-MHz input.

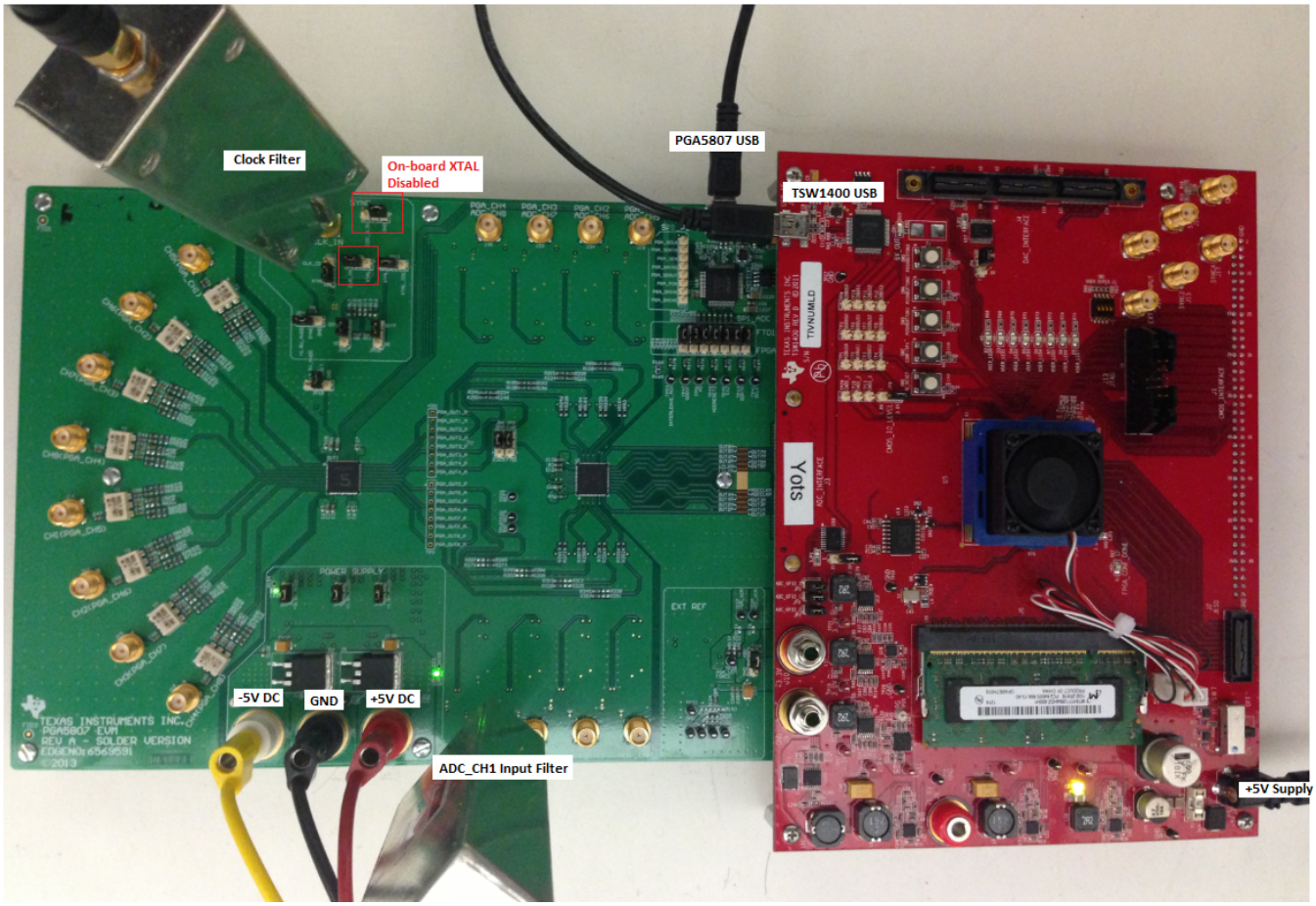


Figure 40. PGA5807 EVM Setup for ADS5296 Only Testing

3. Click on the *ADC* tab and perform the following steps as illustrated in Figure 41.
   (a) In the box labeled *ADC Input Target Frequency* input **5M**
   (b) In the drop down menus set *Real FFT*, *Channel 1/8*, *Rectangular*
   (c) Check the box labeled *Auto Calculation of Coherent Frequencies* (Note: the *ADC Input Target Frequency* box will automatically be updated with the required coherent frequency)
   (d) Change the frequency on the signal generator providing the analog input signal to match the value shown in the *ADC Input Target Frequency* box (**4.99633789MHz**)
   (e) Press the *Capture* button

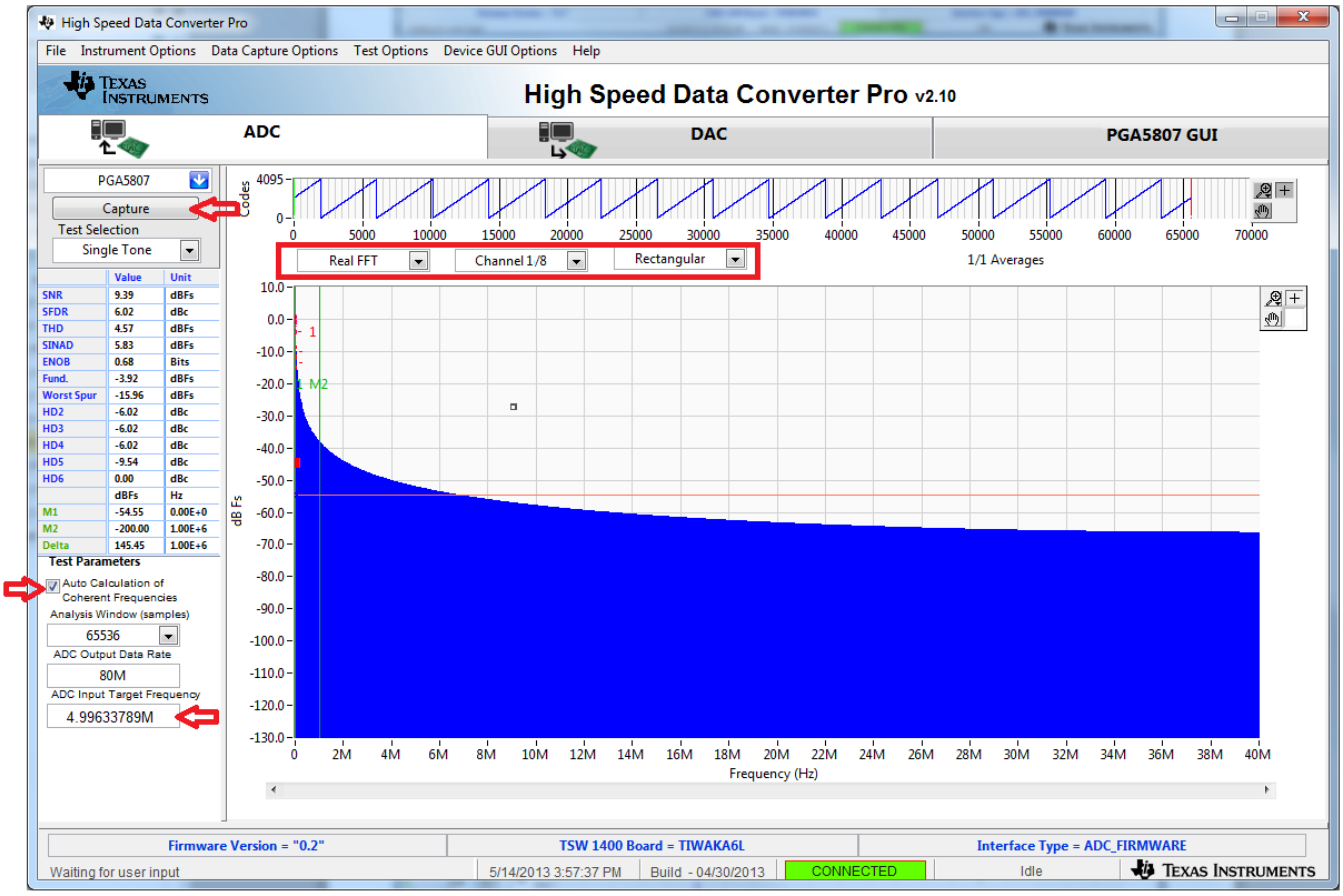


Figure 41. HSDCpro GUI Setup

4. The plot will update as shown in Figure 42. Take note of the *Fund.* value in the left panel highlighted in RED in Figure 42. This value is dependent on the signal level set on the signal generator feeding the input signal to **J36**. It also depends on cable loss and filter insertion loss which can vary among parts. If needed, reset the signal amplitude (level) until the *Fund.* value is approximately –1.0 dBFs, as this is the condition for which the datasheet specifications are set. The input level was iteratively adjusted to achieve –1.0 dBFs as seen in Figure 42.

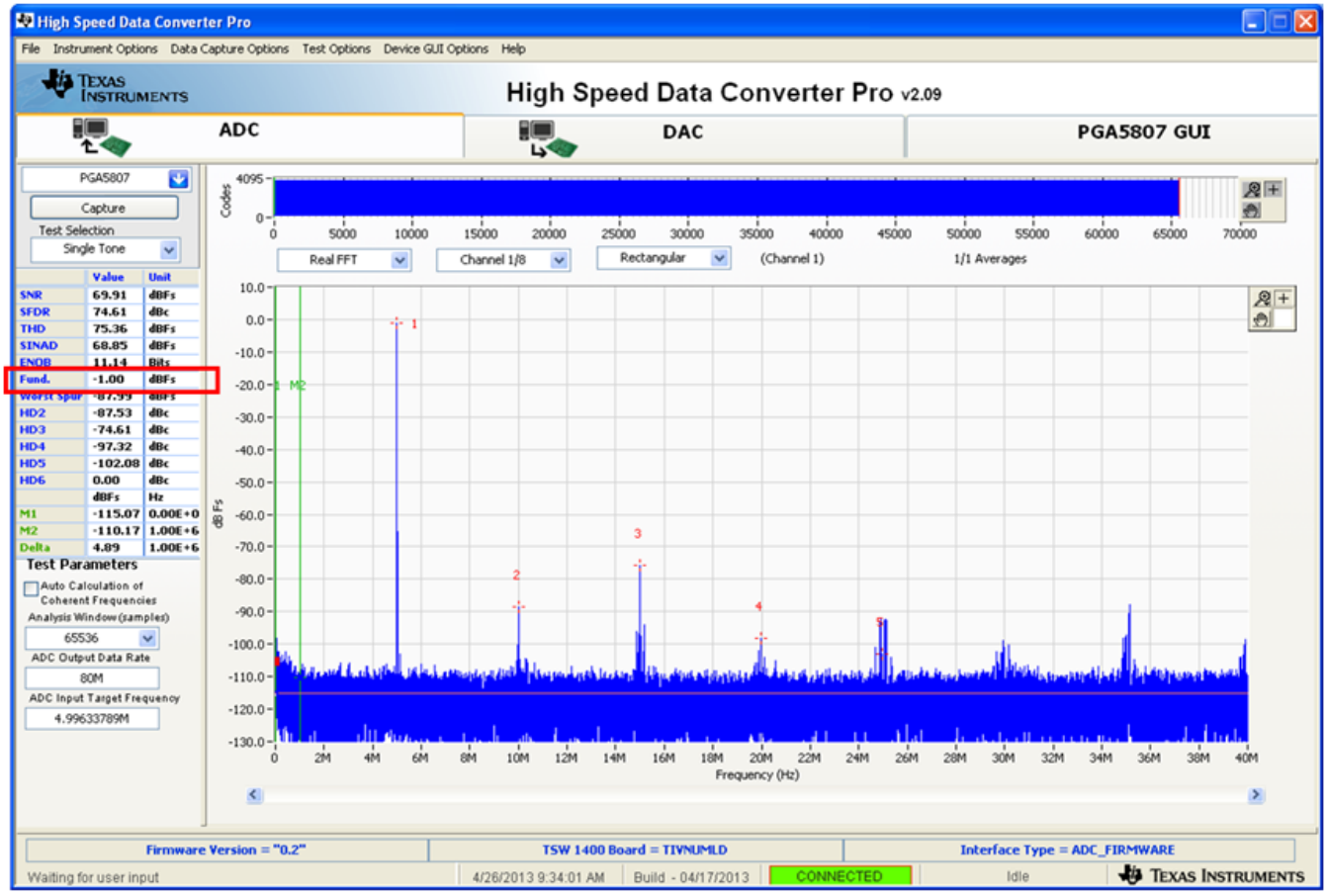


Figure 42. ADS5296 Only Sinusoidal Capture 1

4.4 SNR, THD, and Gain Test for PGA5807 + ADS5296

This section describes the necessary steps for capturing a sinusoidal signal through the PGA5807 and ADS5296 signal path and measuring signal-to-noise ratio (SNR), the total harmonic distortion (THD), and the gain.

1. Setup the EVM as shown in Figure 43 by performing the following steps:
   (a) Connect a filtered signal generator to SMA **J10** labeled **CH5(PGA_CH1)**(–15 dBm, 4.99633789MHz)
   (b) Connect a filtered signal generator to **J5** labeled **CLK_IN** (+5 dbm, 80 MHz).
   (c) The two signal generators in items (a) and (b) above should be phase locked. This is achieved by connecting the two via a BNC cable. One instrument will provide 10-MHz output while the other instrument will receive 10-MHz input.

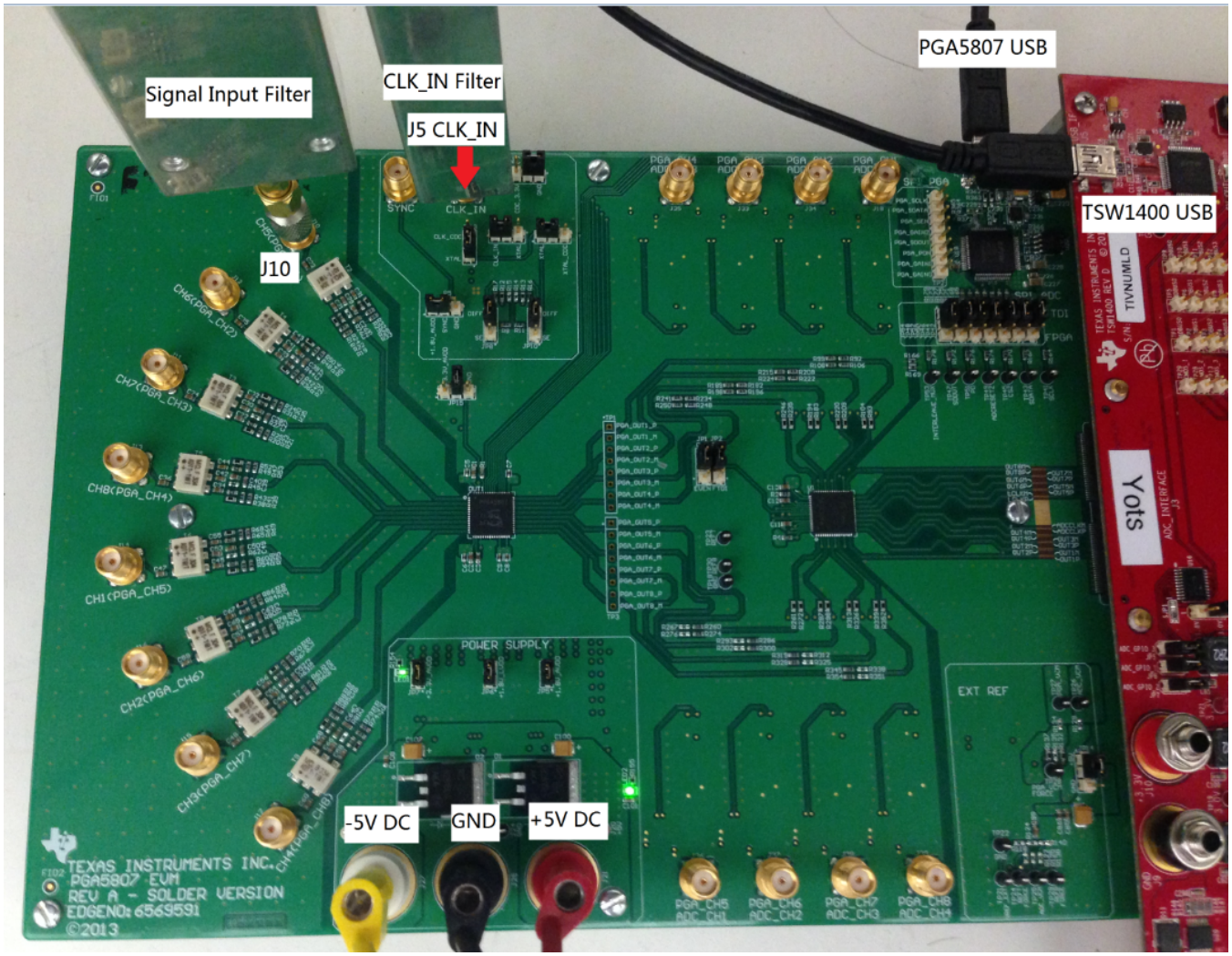


Figure 43. PGA5807 + ADS5296 Gain Test Setup

2. Click on the PGA5807 tab as shown in Figure 44.
   (a) The default state for **PGA_GAIN** is **18dB** (*Note, The PGA5807 gain and filter bandwidth can be set in one of two ways: through the SPI or through dedicated device pins. Both options are available through the software GUI as seen by sections DEVICE PIN CONTROL SECTION and SPI CONTROL SECTION. By setting the **RESET** pin LOW, the PGA5807 is controlled by SPI. By setting the **RESET** pin HIGH, the PGA5807 is controlled through device pins.*)

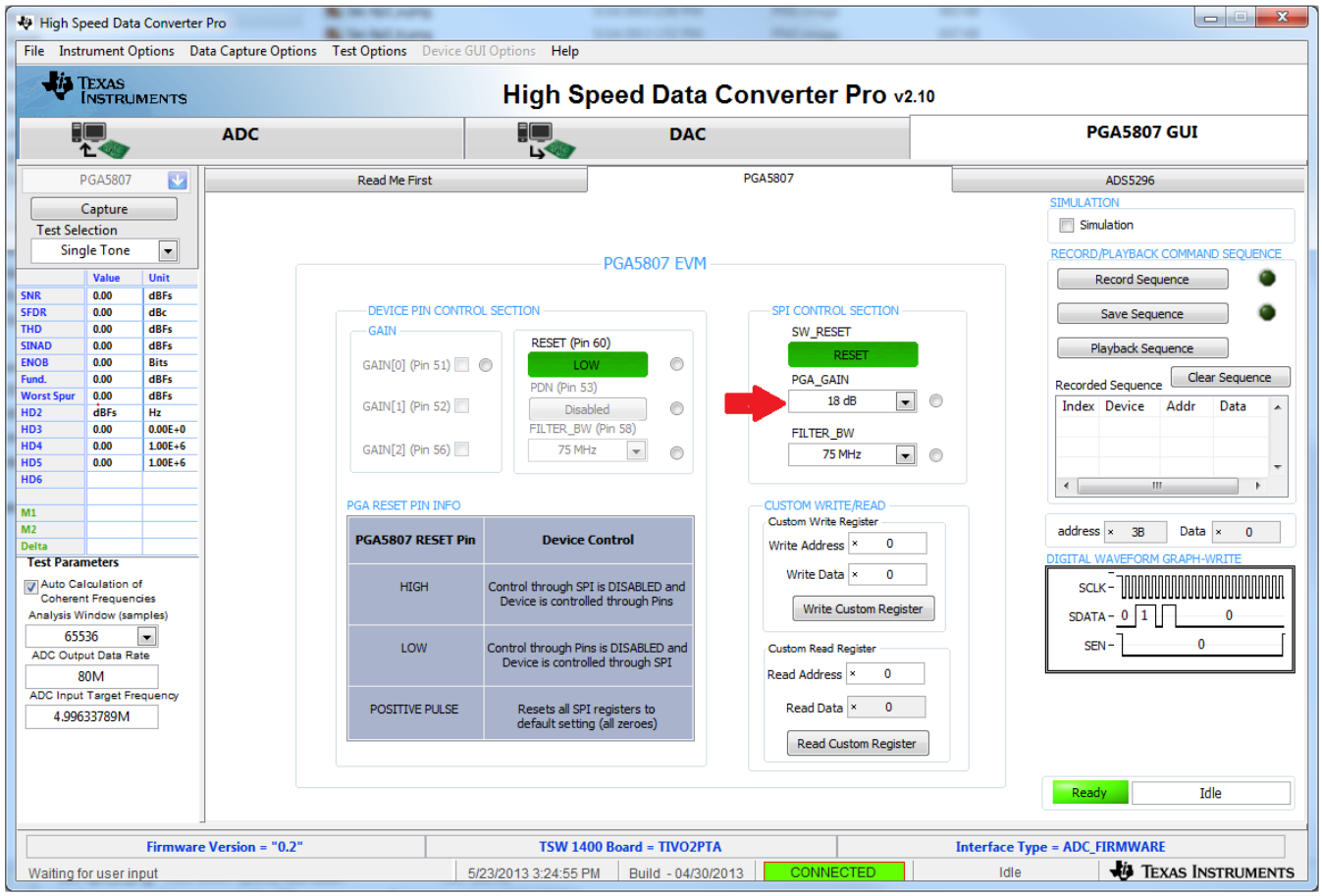


Figure 44. PGA5807 GUI Setup for PGA5807+ADS5296 1

3. Click on the *ADC* tab and press *Capture* to see result similar to Figure 45. Take note of the *Fund.* value in the table to the left. In a similar manner to that described in Section 4.3, the input signal amplitude to the PGA5807 should be adjusted and a re-capture done iteratively until the *Fund.* value is approximately –1.0 dBFs. As –1.0 dBFs is the ADC level at which datasheet specifications are set, the *SNR* and *THD* of the signal chain can be taken from the table to left at this value of *Fund.*

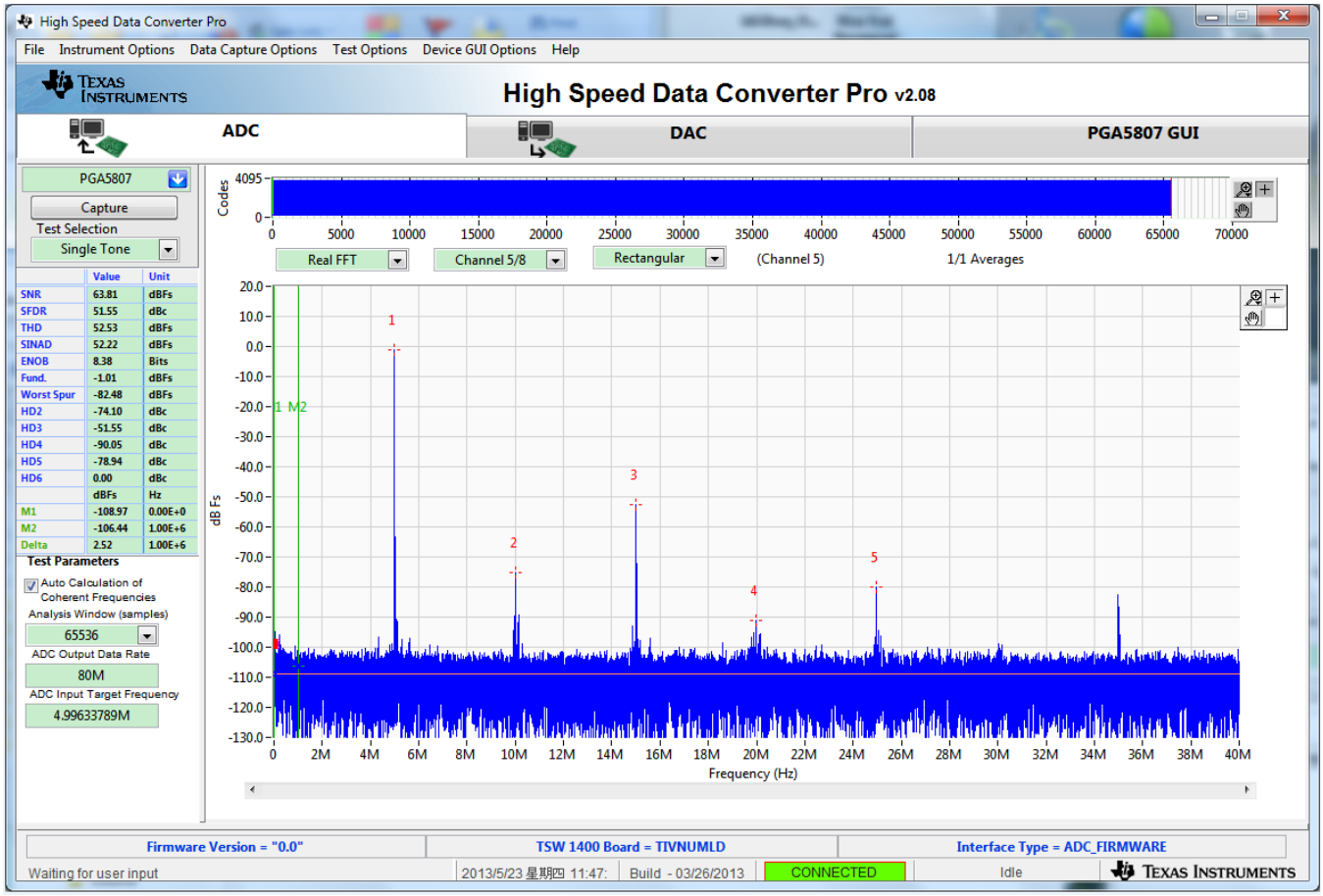


Figure 45. PGA5807+ADS5296 SNR, THD, Gain Test Capture 1

4. Return to the *PGA5807* tab and change the *PGA_GAIN* in the *SPI CONTROL SECTION* to *0 dB* as shown in Figure 46.

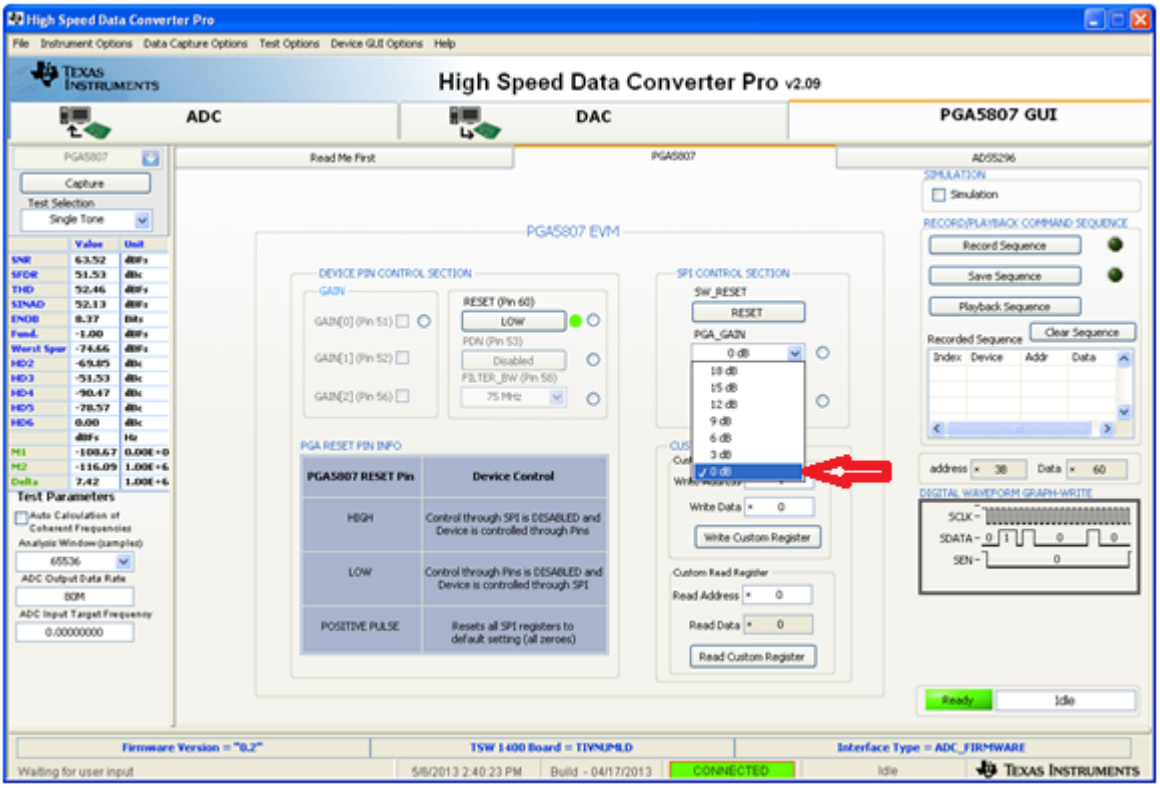


Figure 46. PGA5807 GUI Setup for PGA5807+ADS5296 SNR, THD, Gain Test 2

5. Clicking on the *ADC* tab and pressing *Capture* results in Figure 47. Take the difference in the *Fund.* value shown here to the previous capture. This difference should equal the difference in *PGA_GAIN* values between the two captures, or 18 dB. In this example, the difference is 17.4 dB.

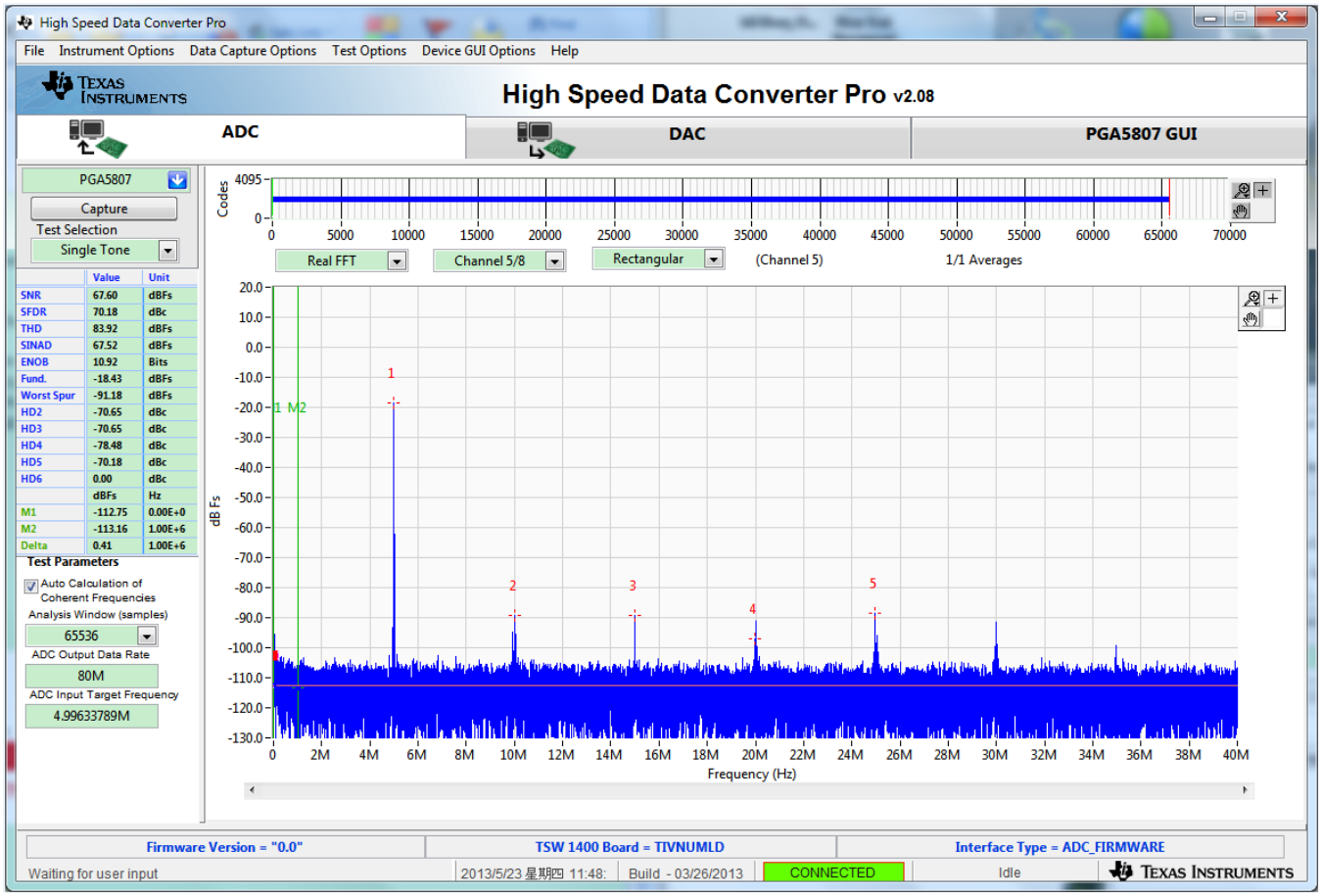


Figure 47. PGA5807+ADS5296 Gain Test Capture 2

6. The same gain test can be performed using the device pins to set the gain instead of the SPI. At the *PGA5807* tab, change the state of the **RESET (Pin 60)** control to *HIGH*. This will disable the *SPI CONTROL SECTION* and enable the *DEVICE PIN CONTROL SECTION* as shown in Figure 48.

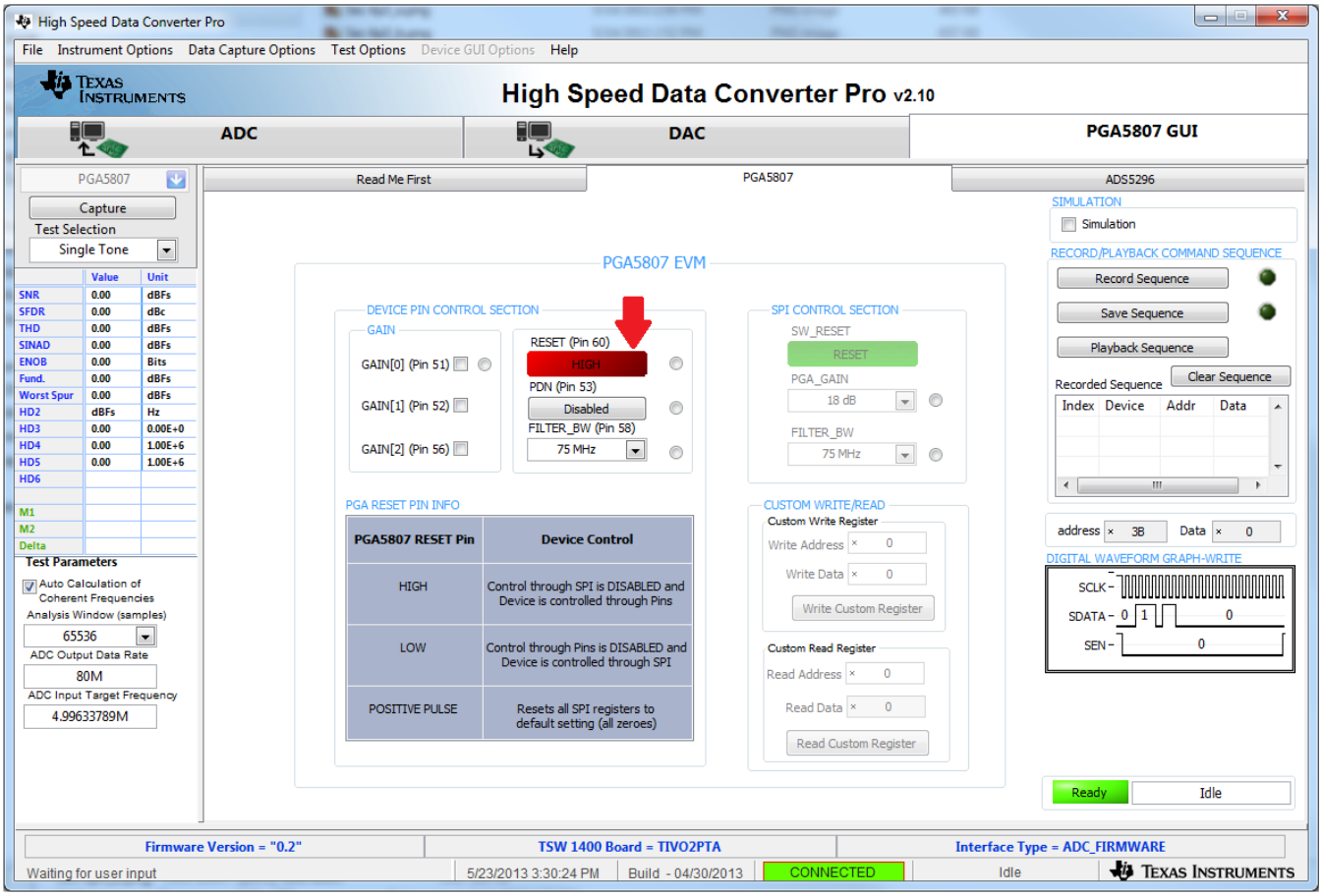


Figure 48. PGA5807 GUI Setup for PGA5807+ADS5296 Gain Test 3

7. Click on the *ADC* tab and press the *Capture* button to see the result shown in Figure 49.

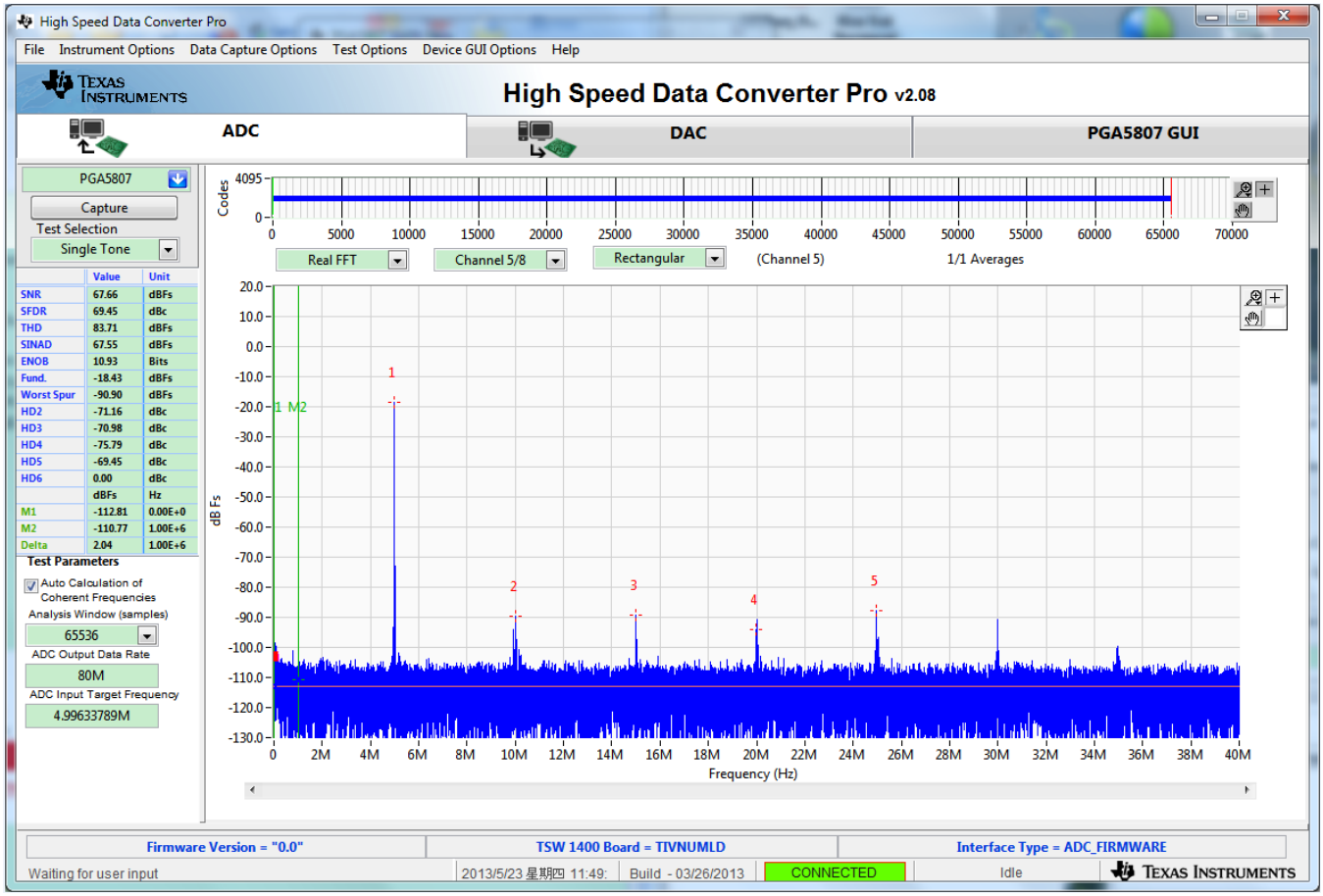


Figure 49. PGA5807+ADS5296 Gain Test Capture 3

8. Return to the *PGA5807* tab and change the **GAIN[x]** values in the *DEVICE PIN CONTROL SECTION* to *18dB* as shown in Figure 50.

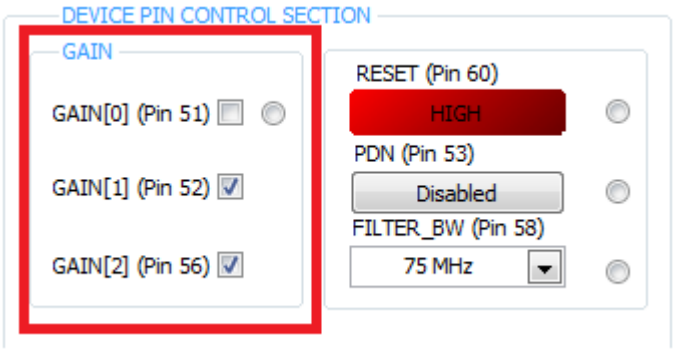


Figure 50. PGA5807 GUI Setup for PGA5807+ADS5296 Gain Test 4

9. Click on the *ADC* tab and press the *Capture* button to see the result shown in Figure 51. Again, take the difference in the *Fund.* value shown here to previous capture. This difference should equal the differerence in **GAIN[x]** value that was set, or 18dB.

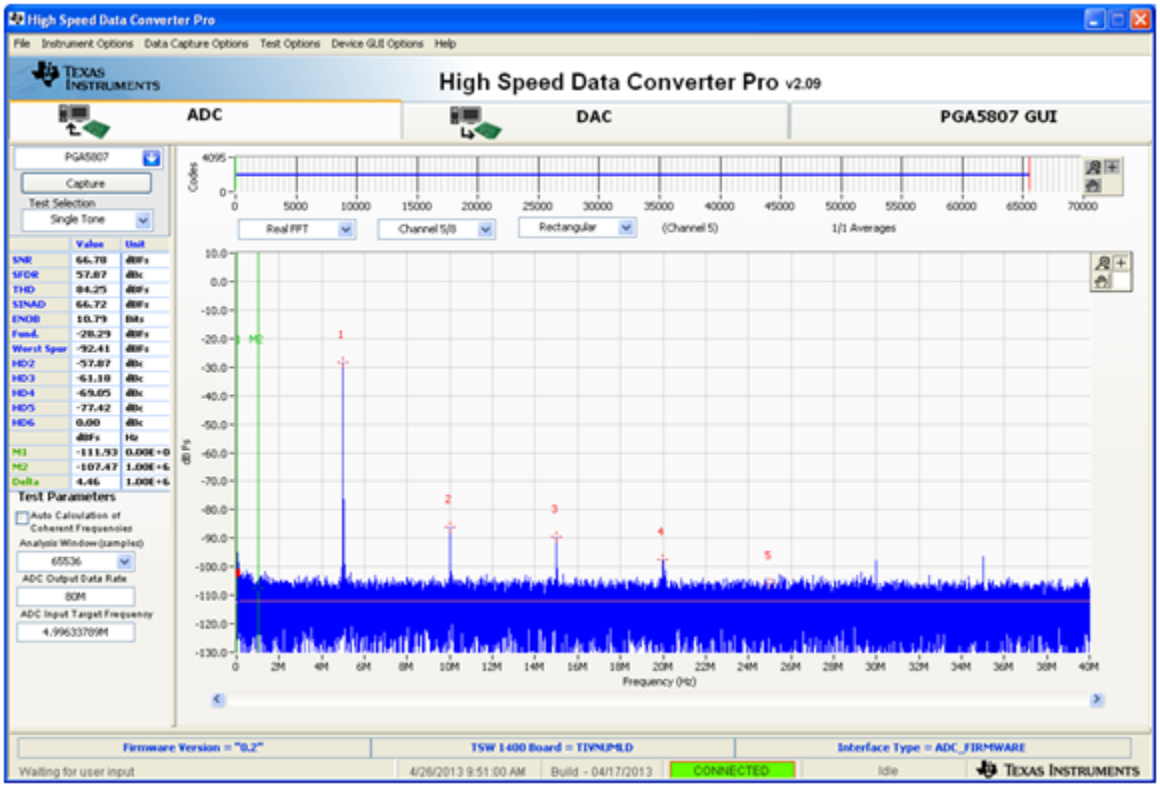


Figure 51. PGA5807+ADS5296 Gain Test Capture 4

10. Finally, in the *PGA5807* tab, reset the device by pressing **RESET (pin 60)** so that this is set to *LOW*. Now click on the **SW_RESET** button within the *SPI CONTROL SECTION*.

5 PGA5807 GUI in Detail

This section is dedicated to explaining the PGA5807 GUI, and all its features, in depth. There is a section dedicated to each tab of the PGA5807 software GUI: *Read Me First*, *PGA5807*, and ADS5296.

After launching *HSDCpro*, the PGA5807 GUI can be invoked in two ways: normal mode or simulation mode. Simulation mode is used in the event that no PGA5807 EVM is available. When this is the case, the message shown in Figure 52 will appear automatically, shortly after choosing the PGA5807 device in *HSDCpro* drop-down menu.

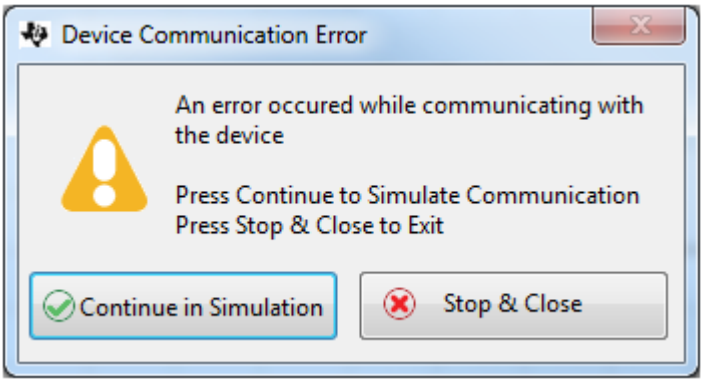


Figure 52. PGA5807 GUI Simulation Mode

The user is given the choice to *Continue in Simulation* or *Stop & Close*. If *Continue in Simulation* is selected the PGA5807 GUI will install and all controls will "appear" to function as normal including the *DIGITAL WAVEFORM GRAPH-WRITE* which shows what is being written to the serial interface. When in *Simulation* mode the checkbox at the top right corner of the GUI will remain checked as shown in Figure 53.

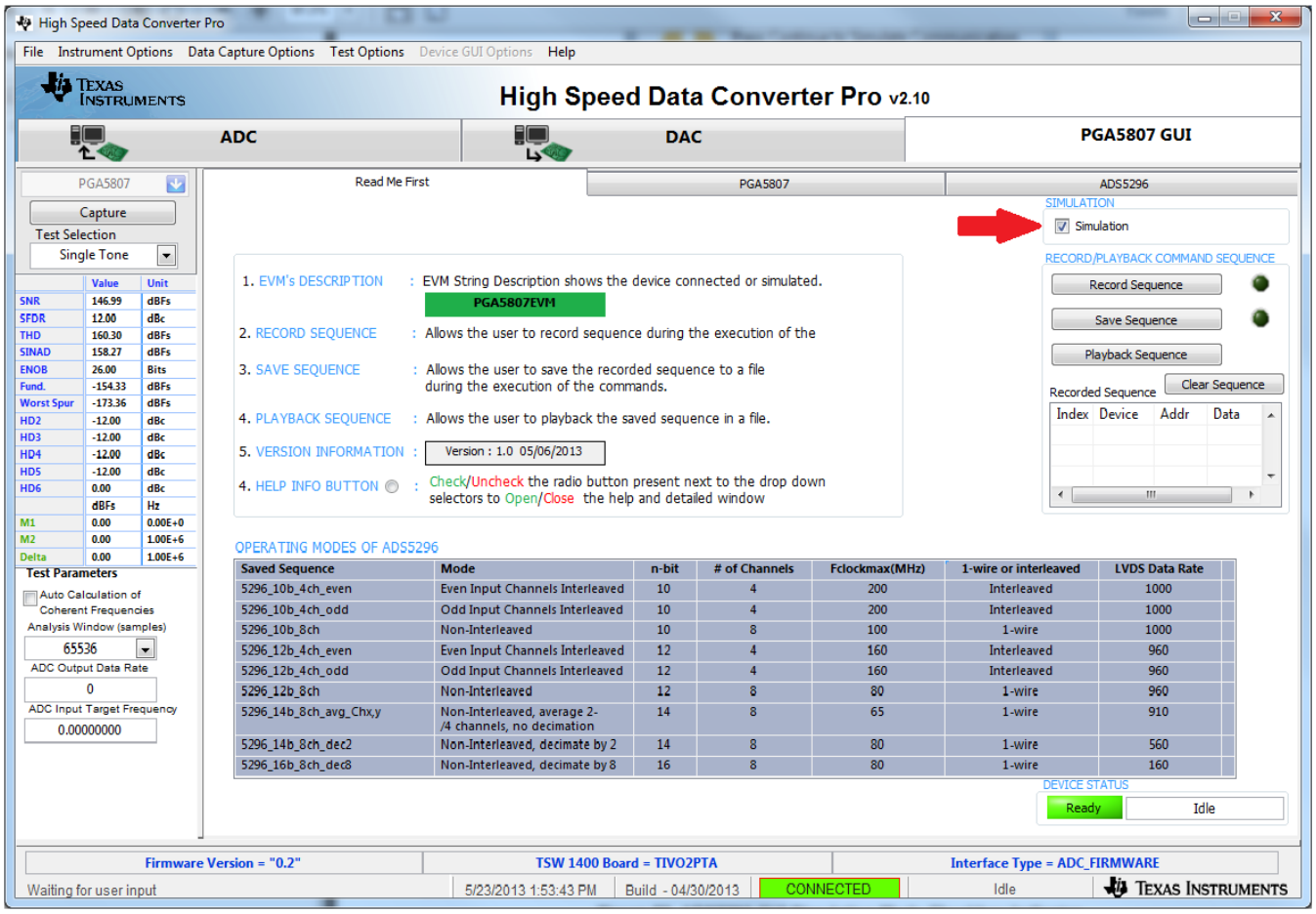


Figure 53. PGA5807 GUI Simulation Mode Checkbox Indicator

5.1 Read Me First tab

The first tab presented when clicking the *PGA5807 GUI* tab is *Read Me First* as shown in Figure 53 (*Simulation* checkbox will be unchecked if EVM is connected).

The two sections in the upper right corner of this tab, *SIMULATION* and *RECORD/PLAYBACK COMMAND SEQUENCE*, are common to all tabs within the PGA5807 GUI. The *RECORD/PLAYBACK COMMAND SEQUENCE* section allows the user to:

- Record a sequence of commands
- Save the sequence that was recorded to a file
- Playback a sequence that was saved from a file

Once the *Record Sequence* button is pressed, the sequence of commands, or SPI writes, will appear chronologically in the *Recorded Sequence* box at the bottom of this section as depicted in Figure 54.

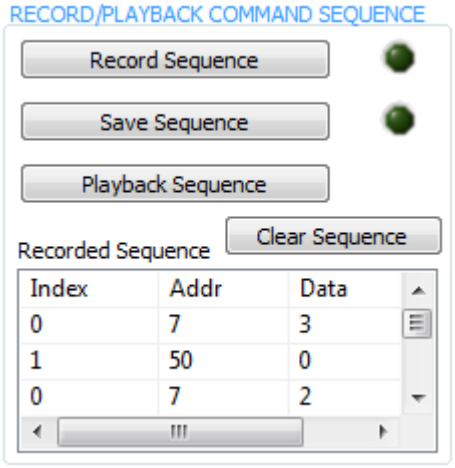


Figure 54. RECORD/PLAYBACK COMMAND SEQUENCE

Hitting the *Save Sequence* button brings up dialog box to save the sequence to the GUI install path:

`C:\Program Files (x86)\Texas Instruments\PGA5807\Recorded Sequences\PGA5807 Recorded Sequences`

To playback a saved sequence, hit the *Playback Sequence* button and choose the sequence to execute. As shown in Figure 55, there are nine sequences pre-defined in this folder corresponding to the nine *OPERATING MODES OF ADS5296* shown in the table at the bottom of the tab. The table includes the maximum sampling clock speed supported for each mode. Ensure that the clock source is within this limit for a particular mode.

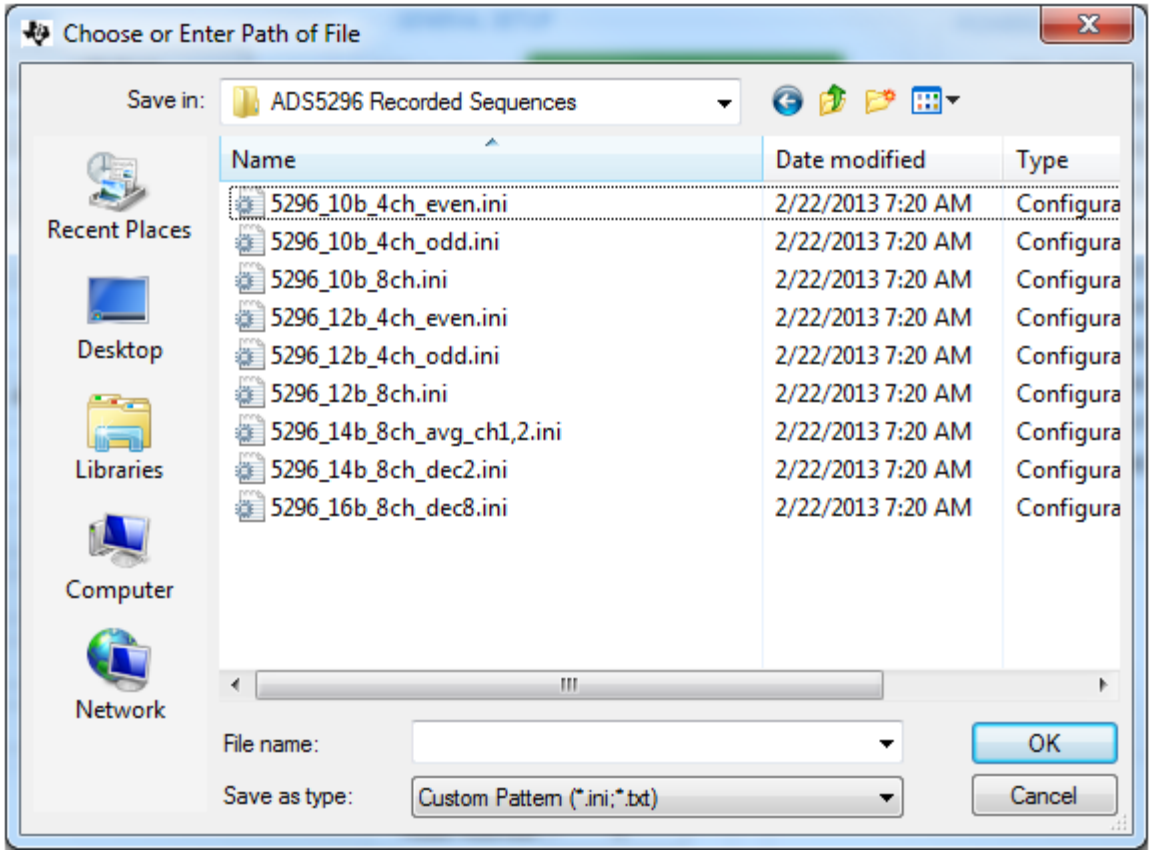


Figure 55. PLAYBACK COMMAND SEQUENCE

5.2 PGA5807 tab

The second tab under the *PGA5807 GUI* tab is *PGA5807*. As shown in Figure 56, this tab contains three sections: *DEVICE PIN CONTROL SECTION*, *SPI CONTROL SECTION*, and *CUSTOM WRITE/READ*. In the right border of this tab is a section called *DIGITAL WAVEFORM GRAPH-WRITE*.

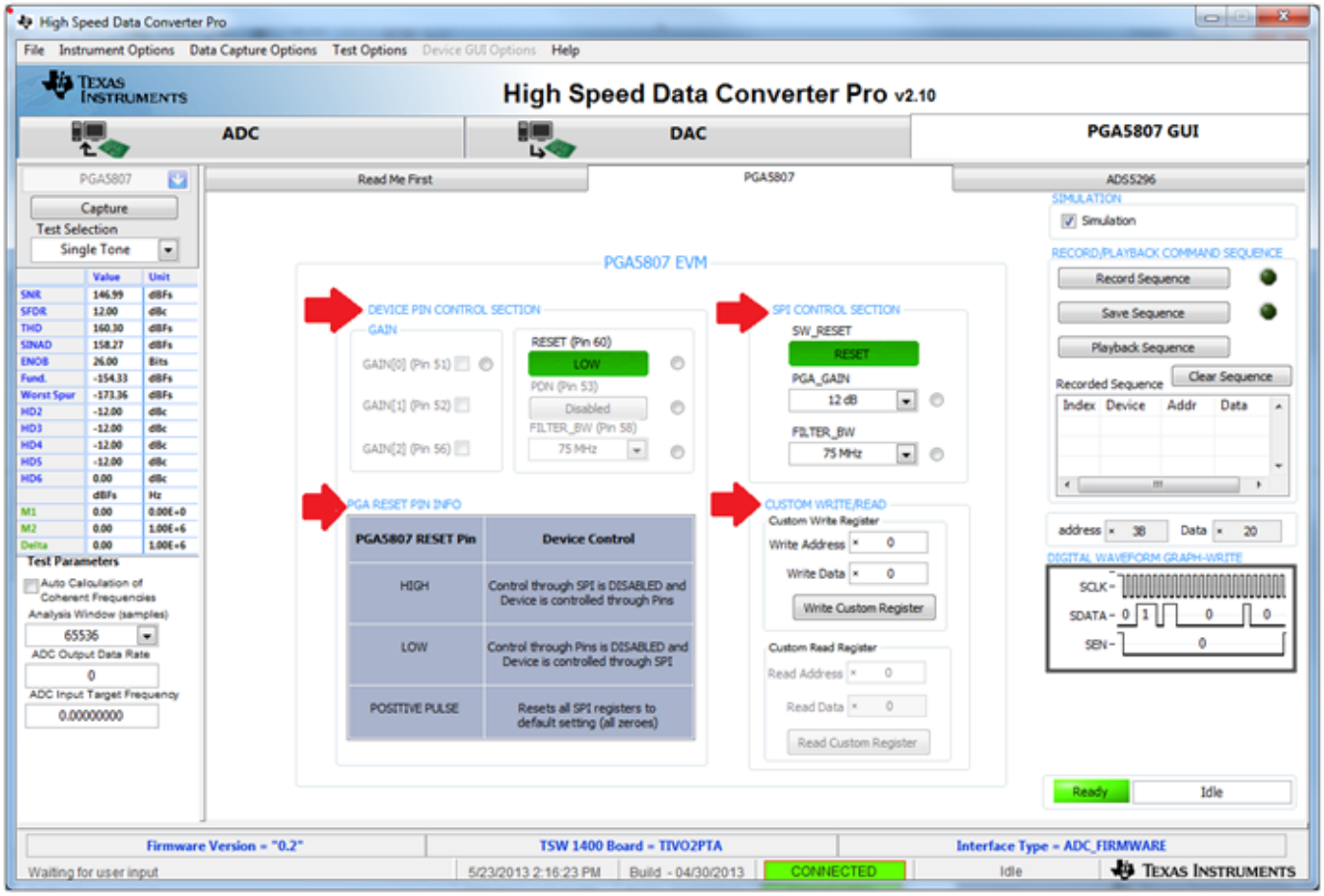


Figure 56. PGA5807 tab

Like sections *Simulation* and *RECORD/PLAYBACK COMMAND SEQUENCE* above it, this section remains fixed in the border when switching among tabs. The *DIGITAL WAVEFORM GRAPH-WRITE* section, shown in Figure 57, tracks all SPI writes from the GUI and displays them here.

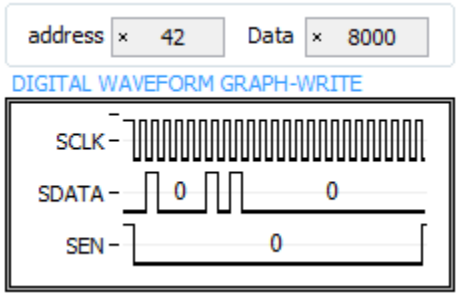


Figure 57. DIGITAL WAVEFORM GRAPH-WRITE Indicator

The *DEVICE PIN CONTROL SECTION* does exactly as the name implies; it provides static logic levels to PGA5807 device pins for programming the reset, PGA gain, power down, and filter bandwidth. As Figure 58 shows, when the **RESET (Pin 60)** is held *High*, all controls in this section are enabled and the SPI interface is disabled causing *SPI CONTROL SECTION* to become greyed and disabled (not shown in Figure 58). The *PGA RESET PIN INFO* is provided as a reminder of the **RESET** pin functionality.

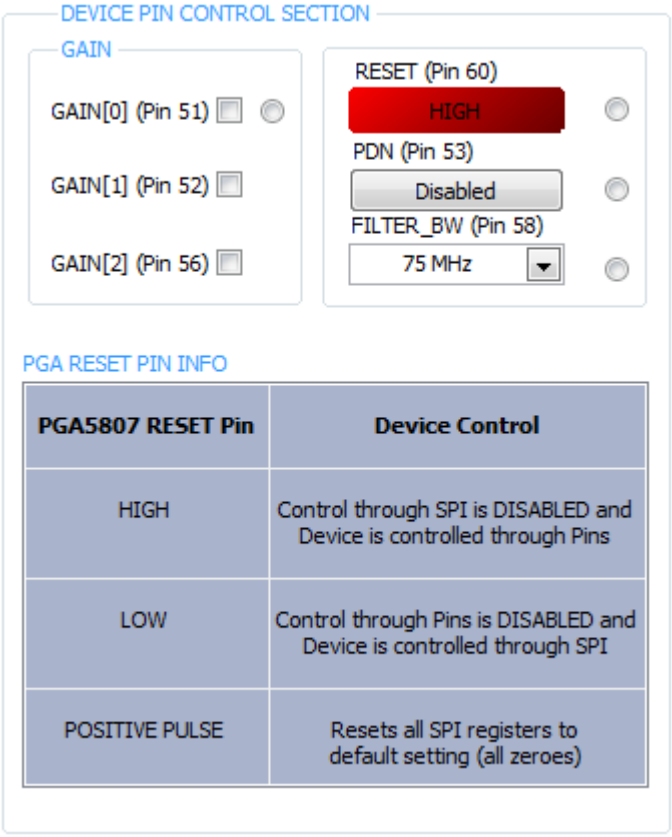


Figure 58. DEVICE PIN CONTROL SECTION

An info button is present to the right of each control, or set of controls. Pressing this button displays relevant information from the datasheet. Figure 59 shows the information presented when the info button in the GAIN section is selected.

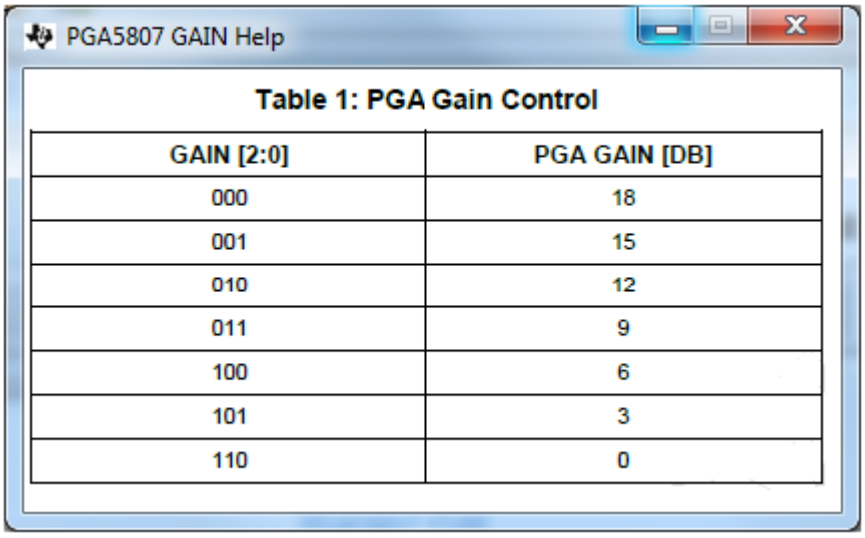


Figure 59. Gain Info Button

The *SPI CONTROL SECTION* writes to the device's SPI interface for programming the software reset, PGA gain, and filter bandwidth. As Figure 60 shows, this section is enabled only when the **RESET (Pin 60)** pin is set *LOW*.

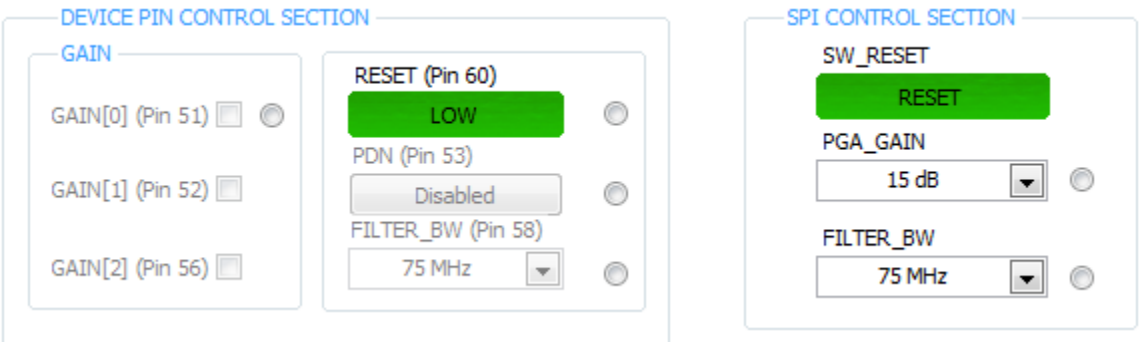


Figure 60. Gain Info Button

The *CUSTOM WRITE/READ* section allows for custom writing to the serial interface of the PGA5807 device as well as reading back register values. When a valid register address and value is provided, the corresponding control will automatically update to reflect the current state of the device. Figure 61 shows that when the value of register 0x3B, containing field **PGA_GAIN**, was written as 0x0 and then as 0x20, the **PGA_GAIN** control updated its value to reflect the present state of the device.

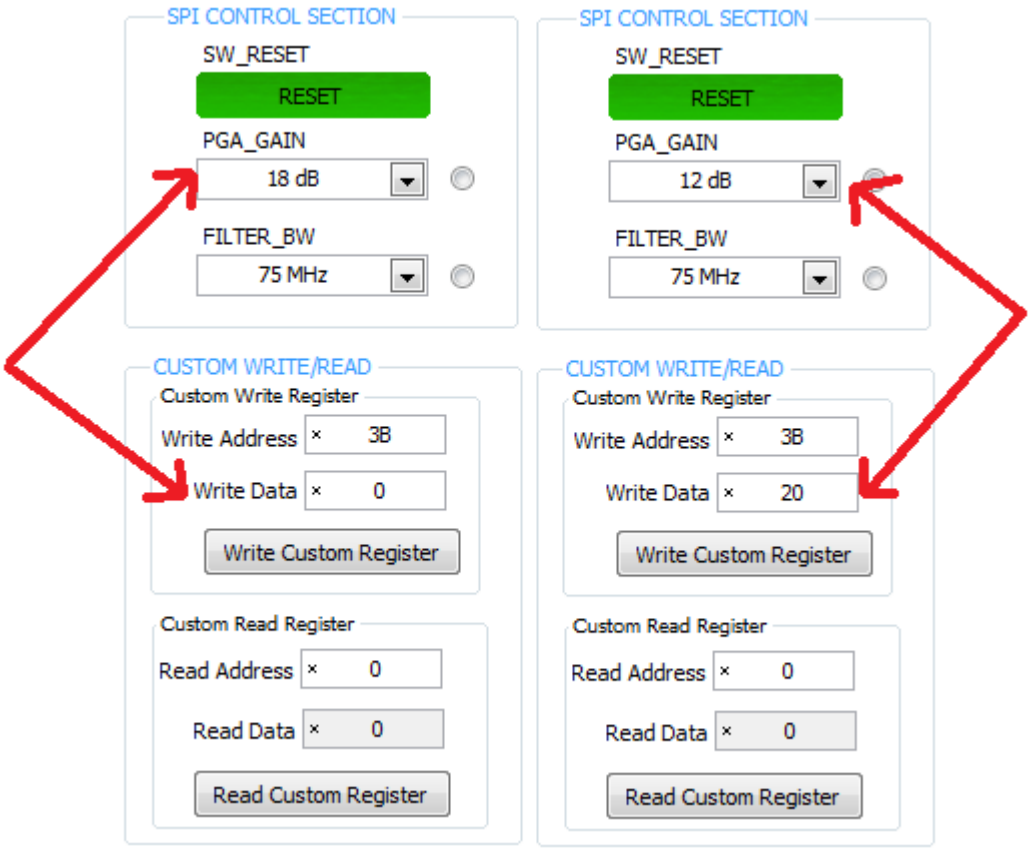


Figure 61. CUSTOM WRITE/READ

5.3 ADS5296 tab

The last tab under the *PGA5807 GUI* tab is *ADS5296*. As shown in Figure 62, this tab contains four sub-tabs *Top Level*, *Test Pattern*, *Digital Signal Processing*, and *Channel Filter*. For an in-depth explanation of the ADS5296 GUI and all its features, please refer to Section 5 of the ADS5296 User's Guide (SLAU491).

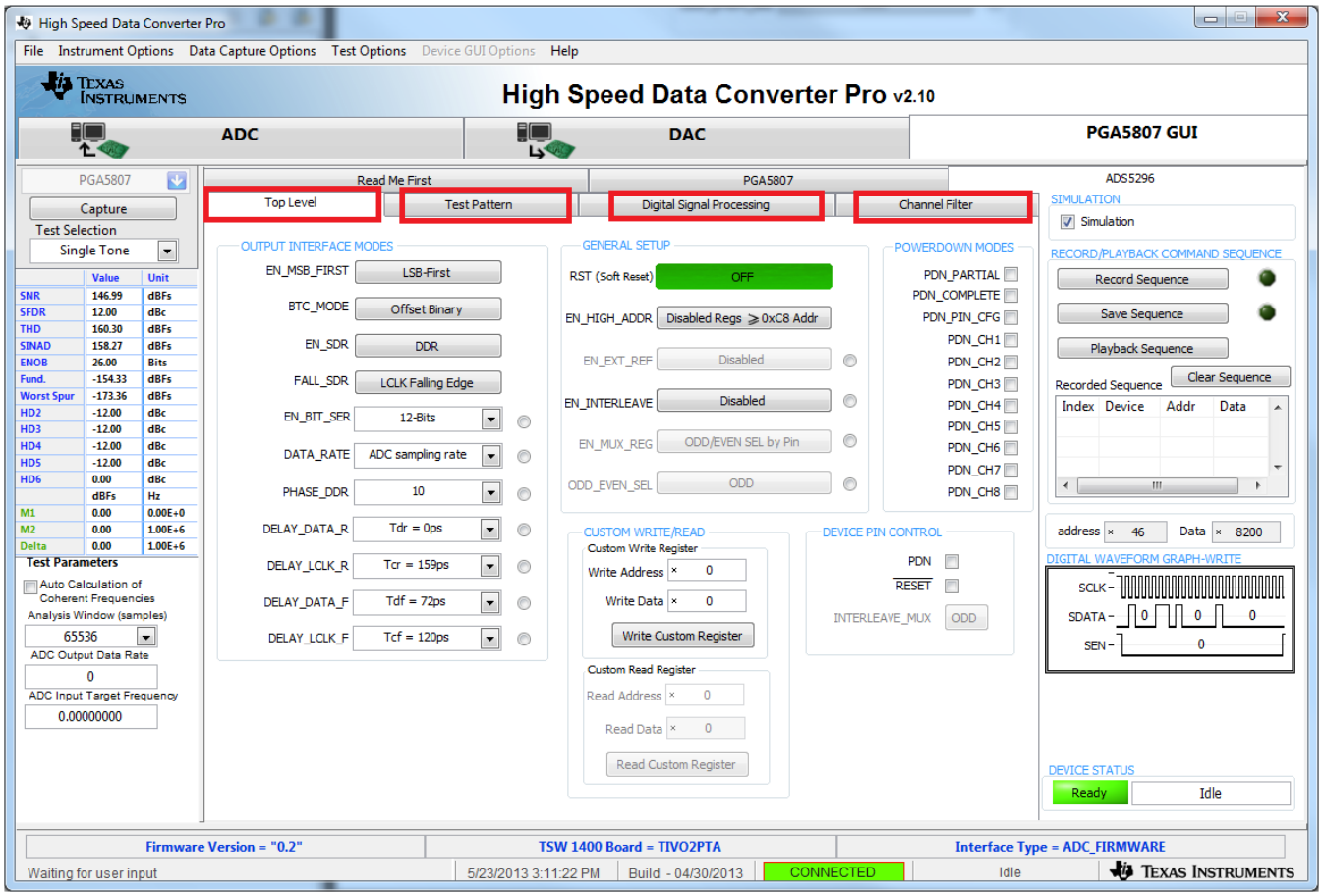


Figure 62. ADS5296 tab

6 PGA5807 EVM Schematics

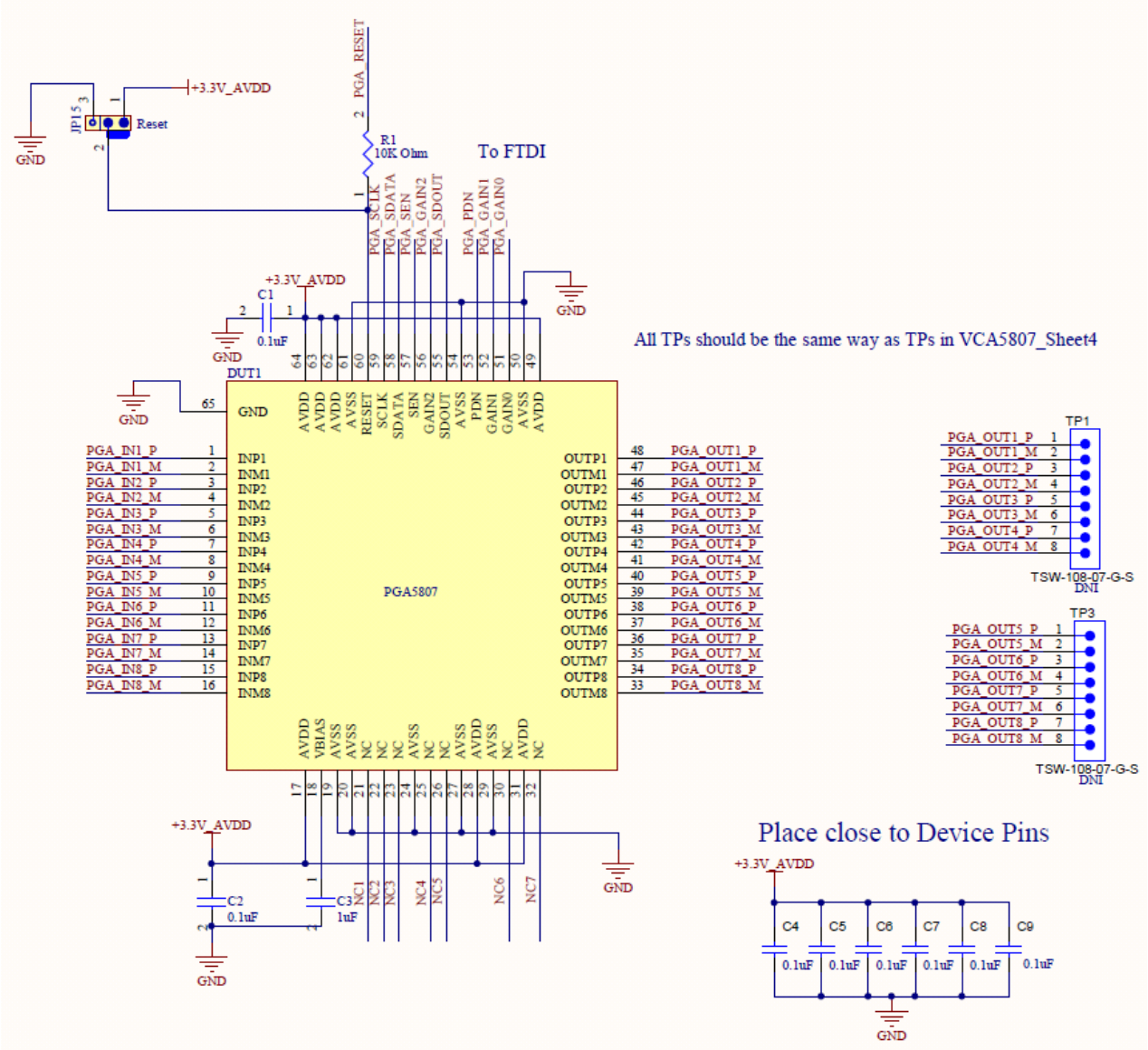


Figure 63. PGA5807 Schematic, (Sh. 1 of 16), PGA5807 Device

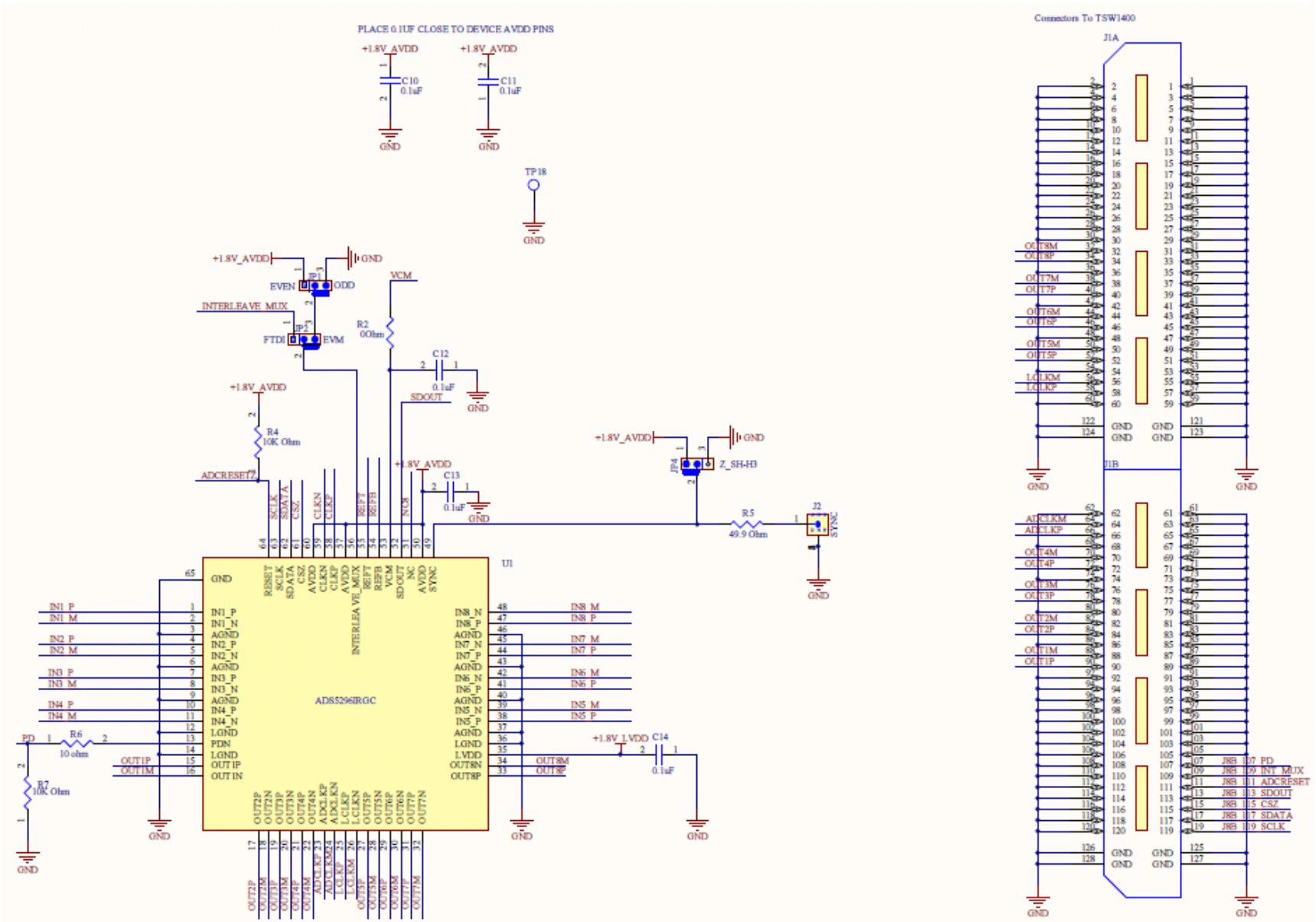
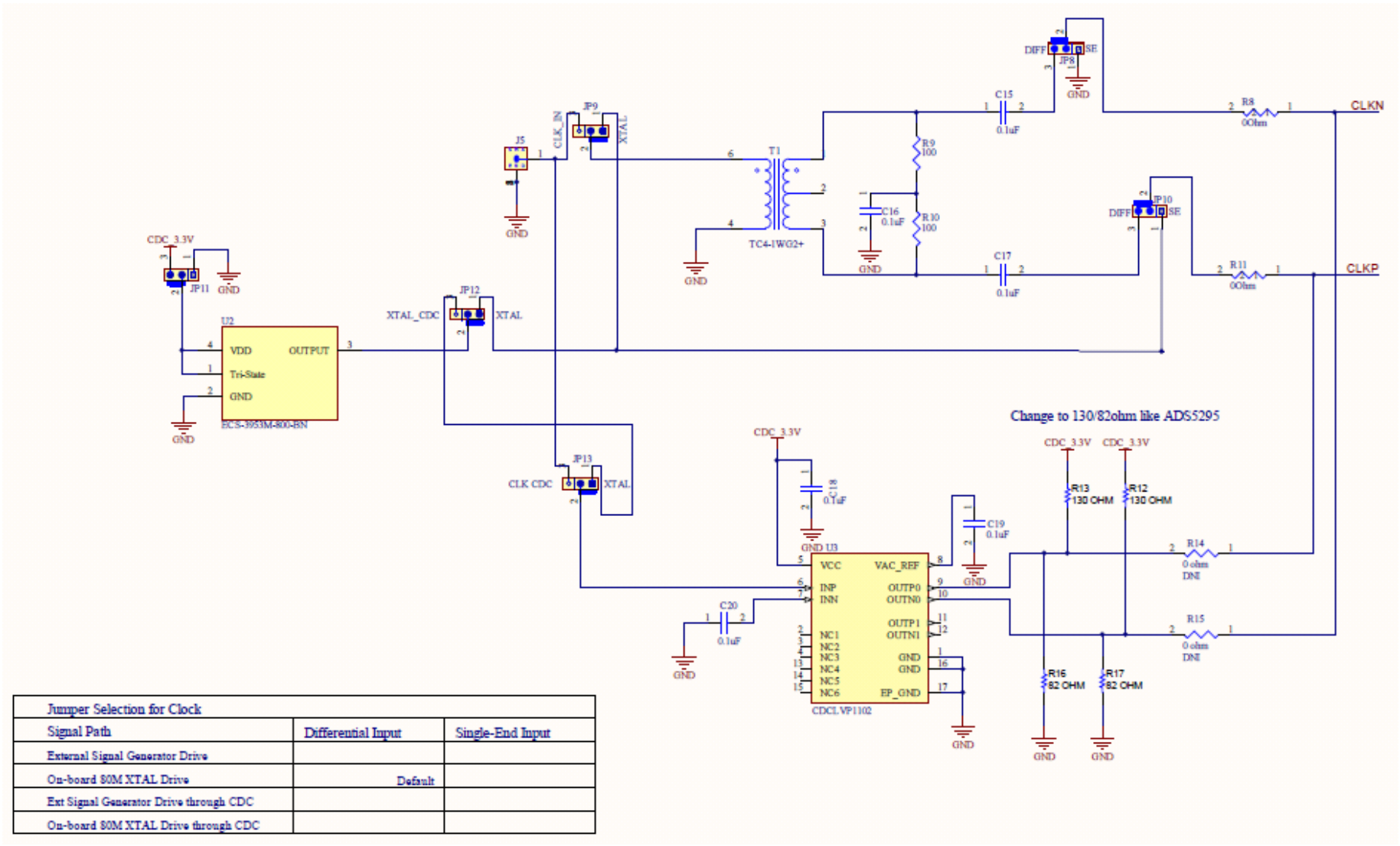


Figure 64. PGA5807 Schematic, (Sh. 2 of 16), ADS5296 Device



Jumper Selection for Clock		
Signal Path	Differential Input	Single-End Input
External Signal Generator Drive		
On-board 80M XTAL Drive	Default	
Ext Signal Generator Drive through CDC		
On-board 80M XTAL Drive through CDC		

Figure 65. PGA5807 Schematic, (Sh. 3 of 16), ADS5296 Sampling Clock

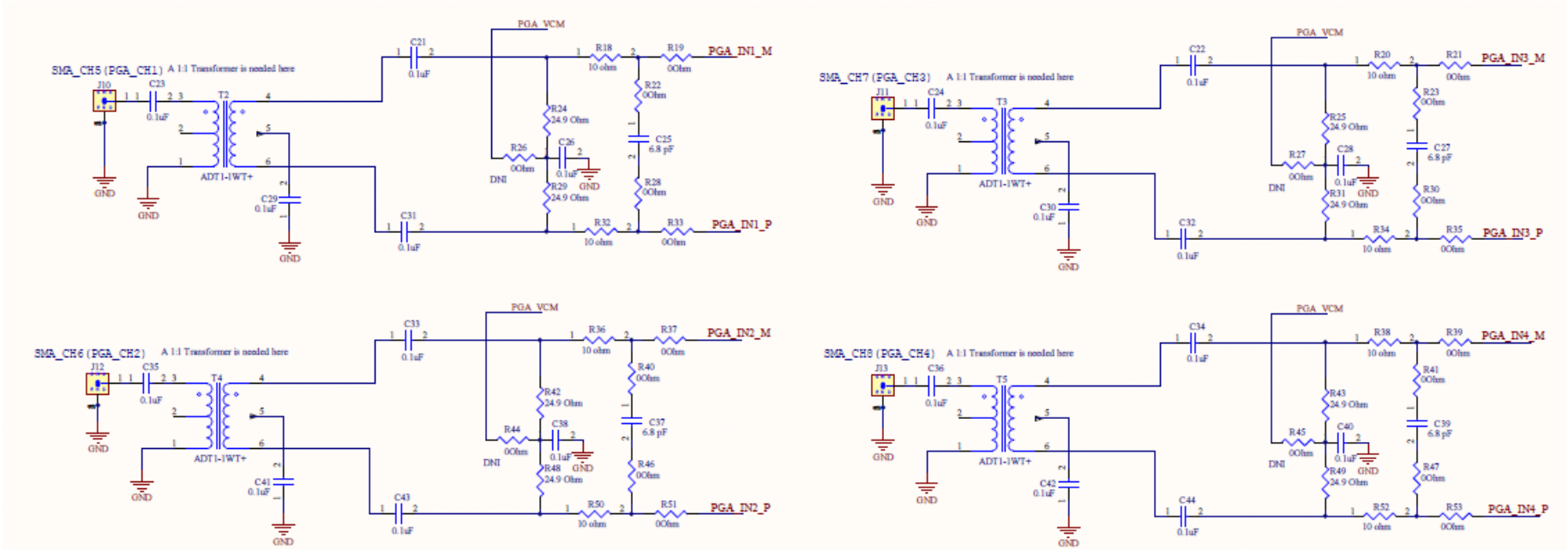


Figure 66. PGA5807 Schematic, (Sh. 4 of 16), PGA5807 Analog Inputs Ch1-4

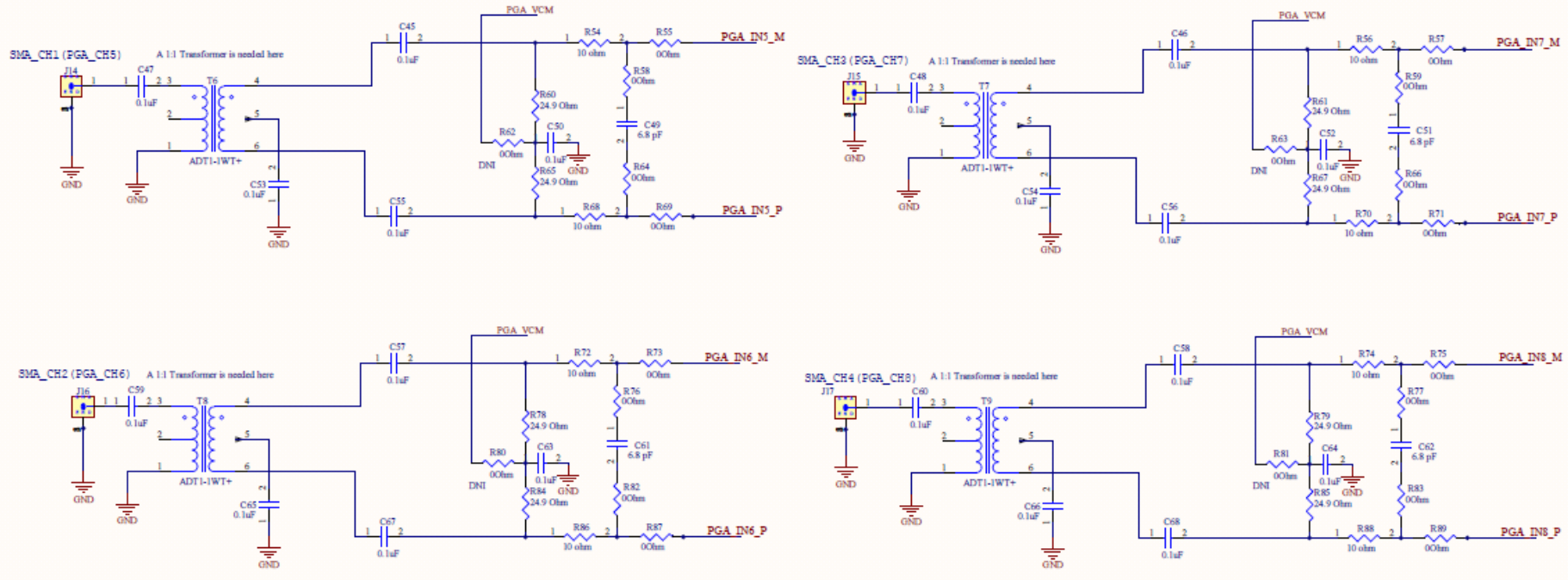


Figure 67. PGA5807 Schematic, (Sh. 5 of 16), PGA5807 Analog Inputs Ch5-8

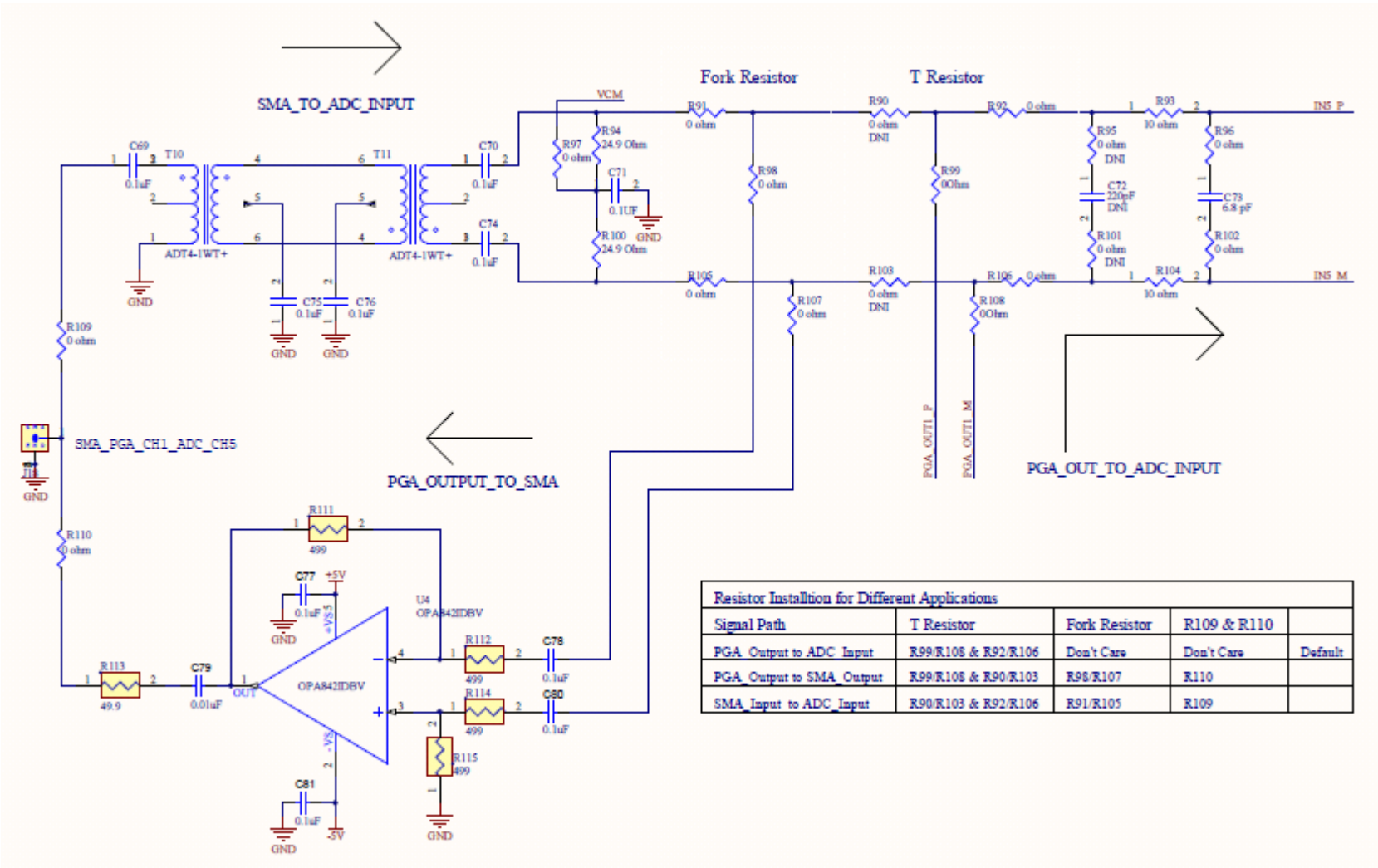


Figure 68. PGA5807 Schematic, (Sh. 6 of 16), PGA_CH1, ADC_CH5

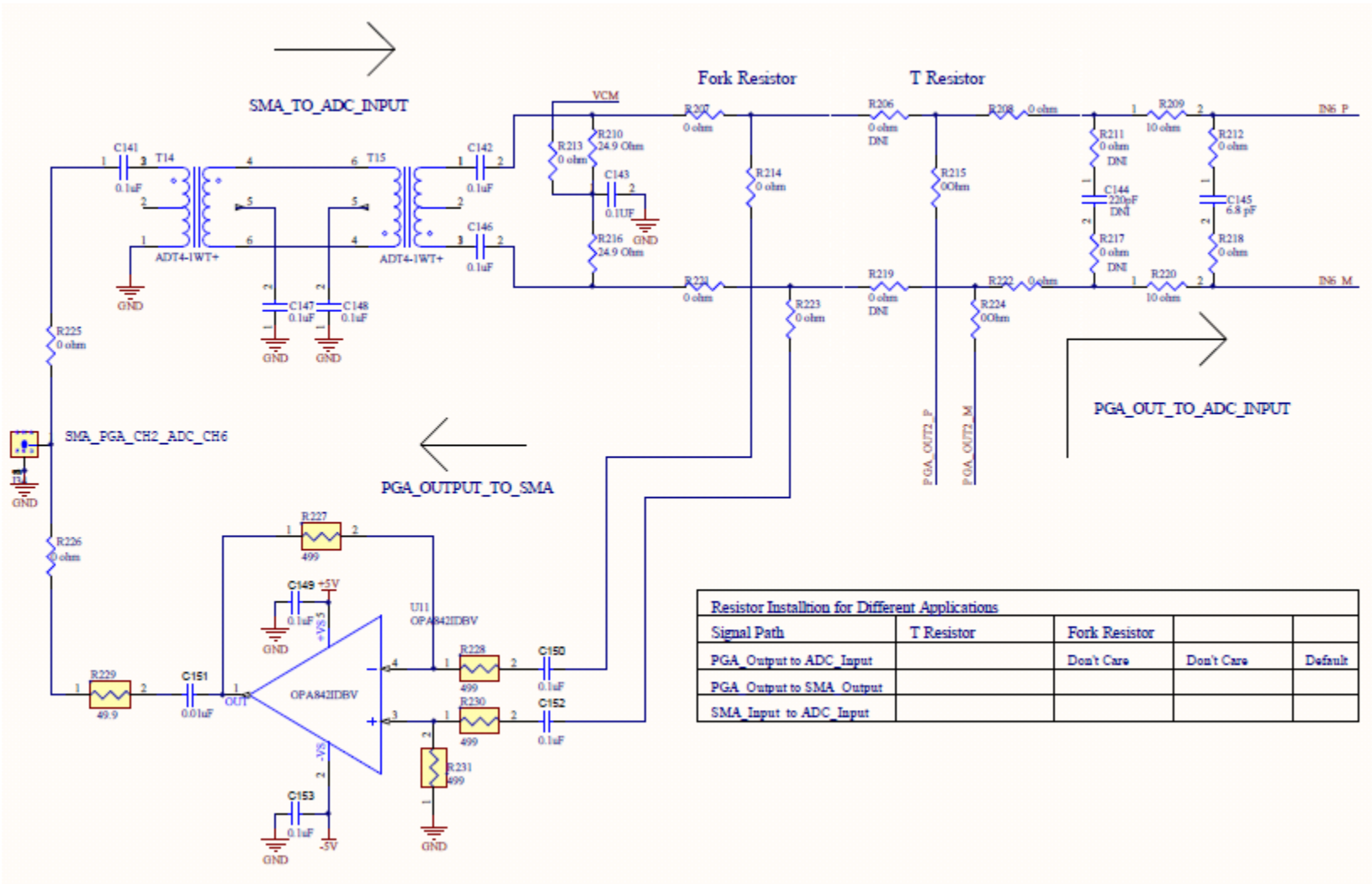


Figure 69. PGA5807 Schematic, (Sh. 7 of 16), PGA_CH2, ADC_CH6

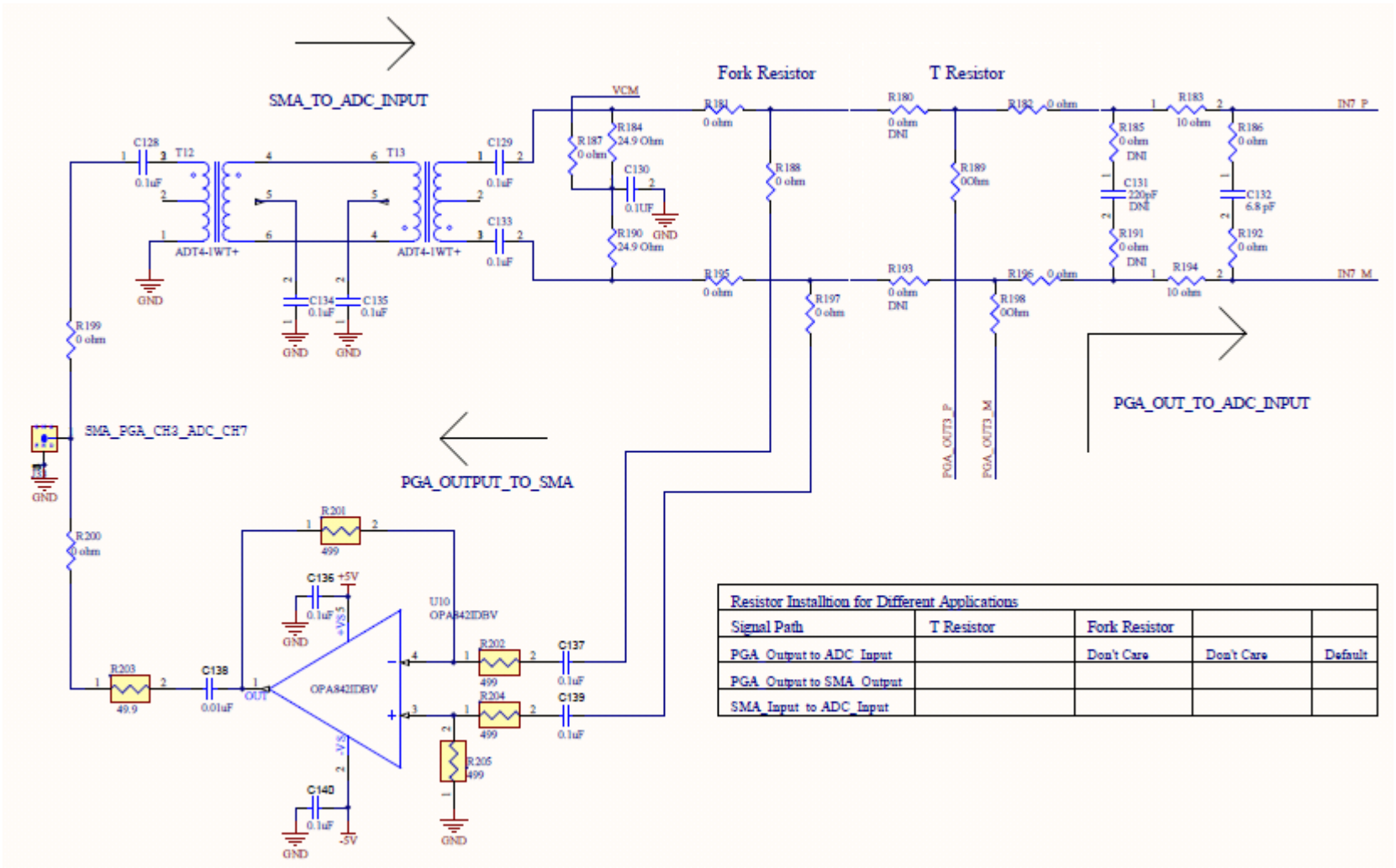


Figure 70. PGA5807 Schematic, (Sh. 8 of 16), PGA_CH3, ADC_CH7

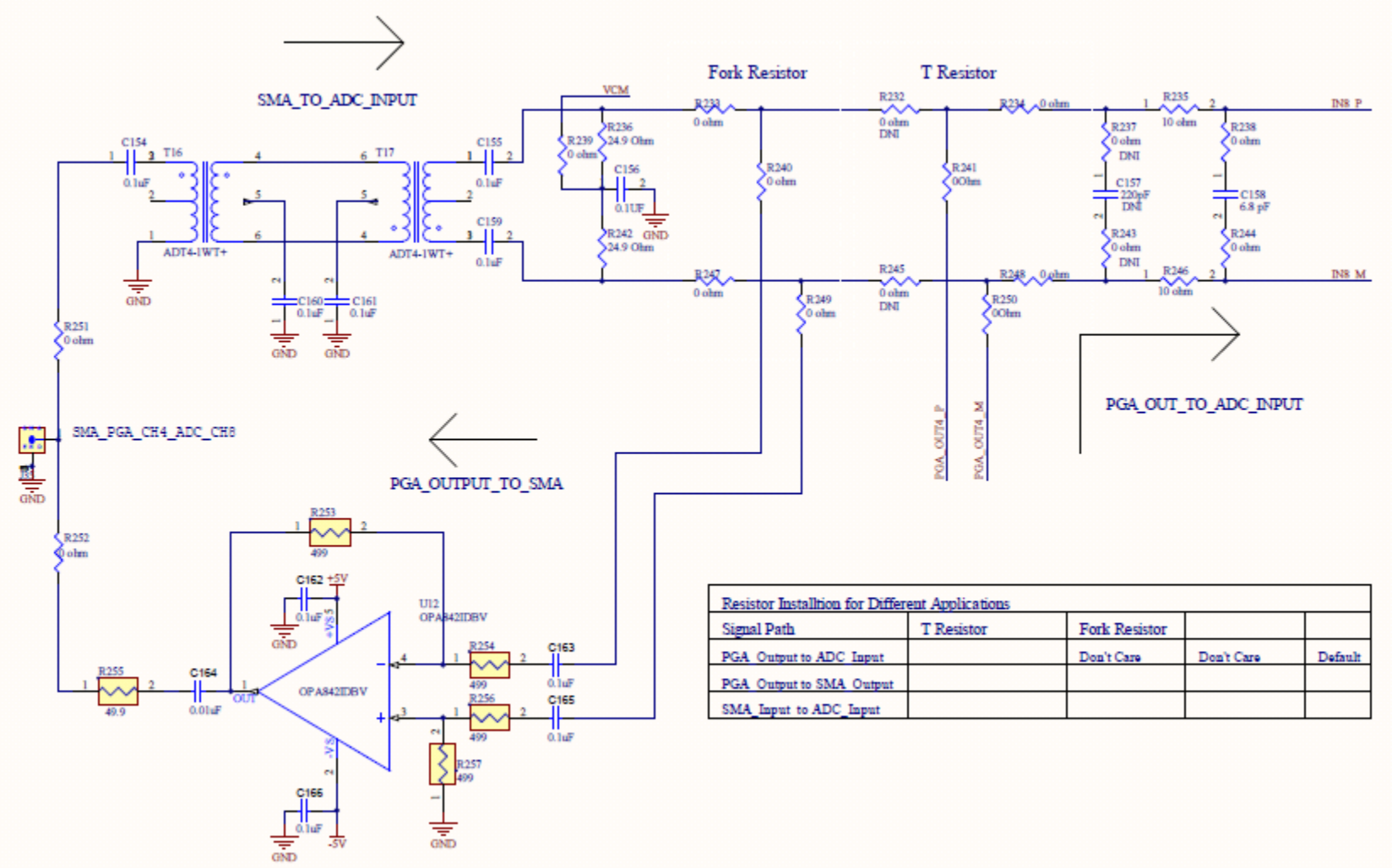


Figure 71. PGA5807 Schematic, (Sh. 9 of 16), PGA_CH4, ADC_CH8

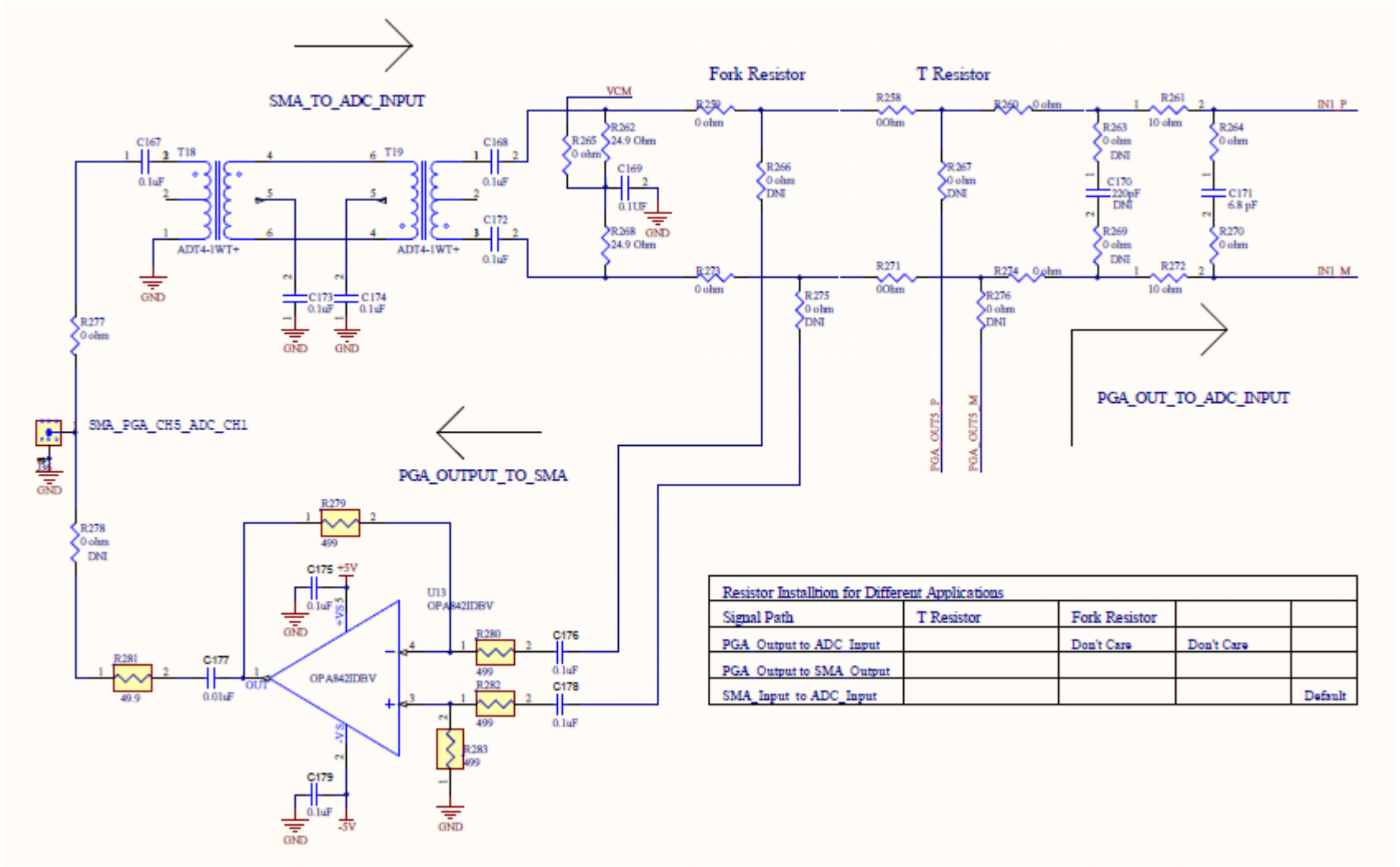


Figure 72. PGA5807 Schematic, (Sh. 10 of 16), PGA_CH5, ADC_CH1

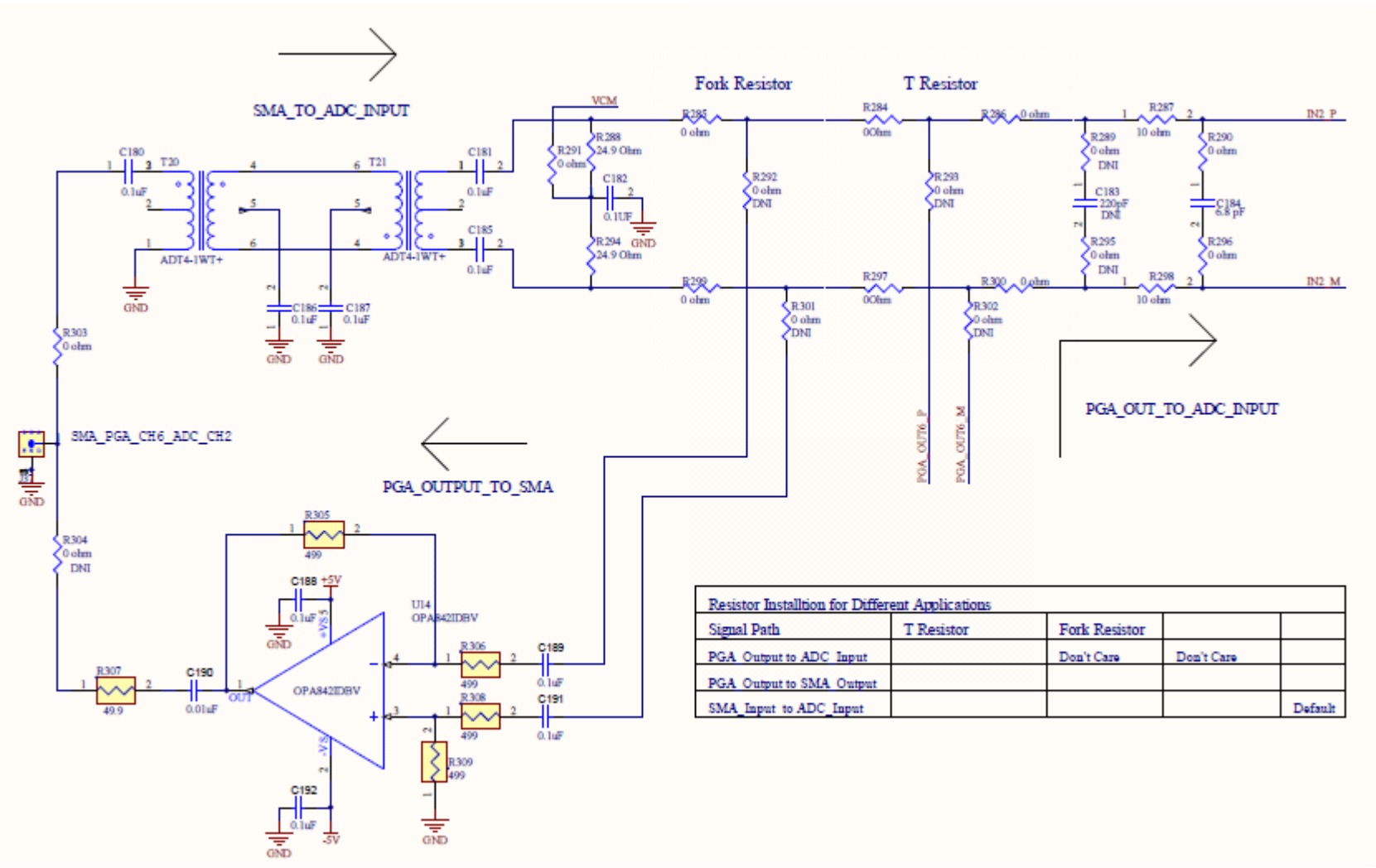


Figure 73. PGA5807 Schematic, (Sh. 11 of 16), PGA_CH6, ADC_CH2

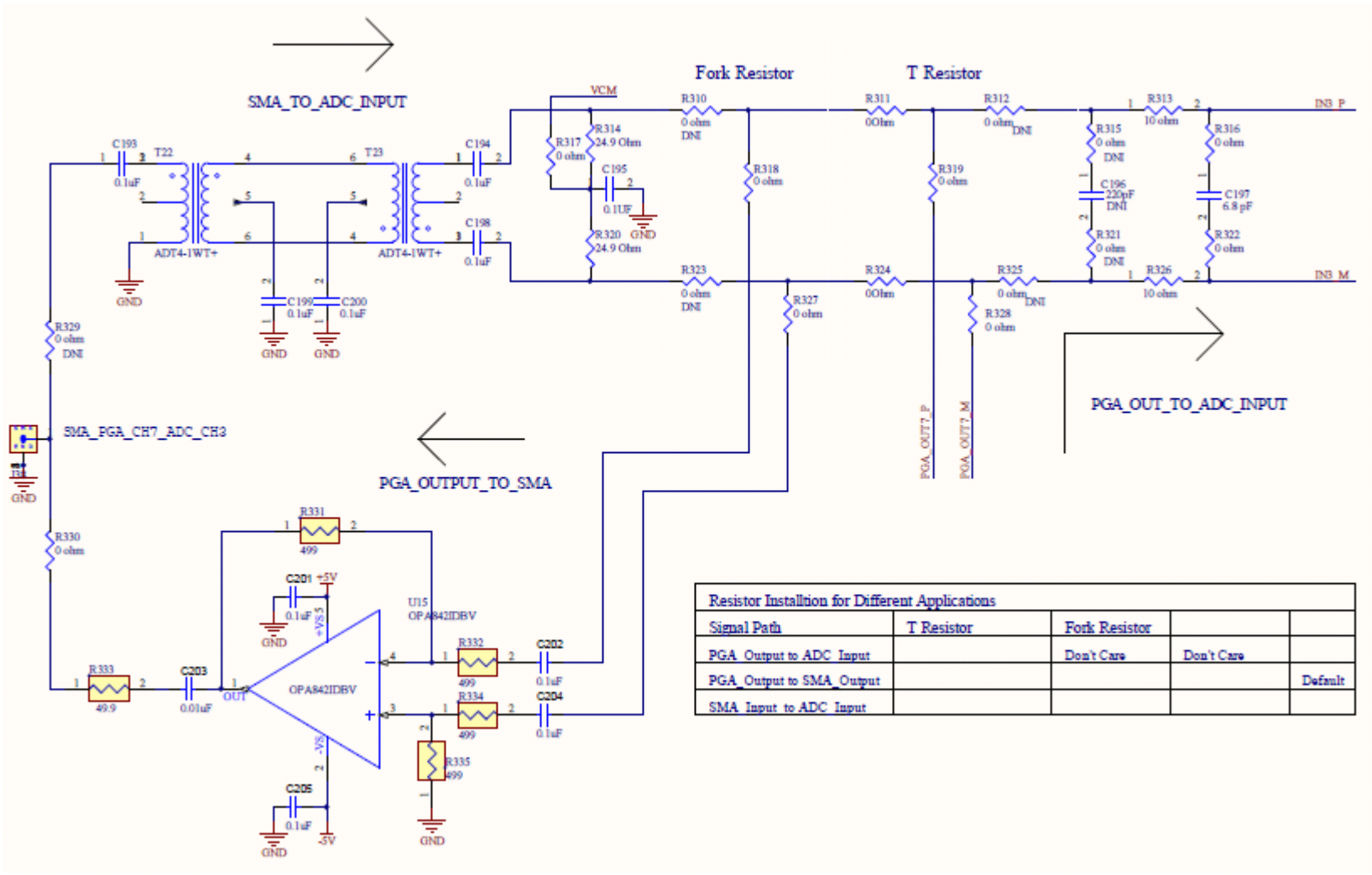
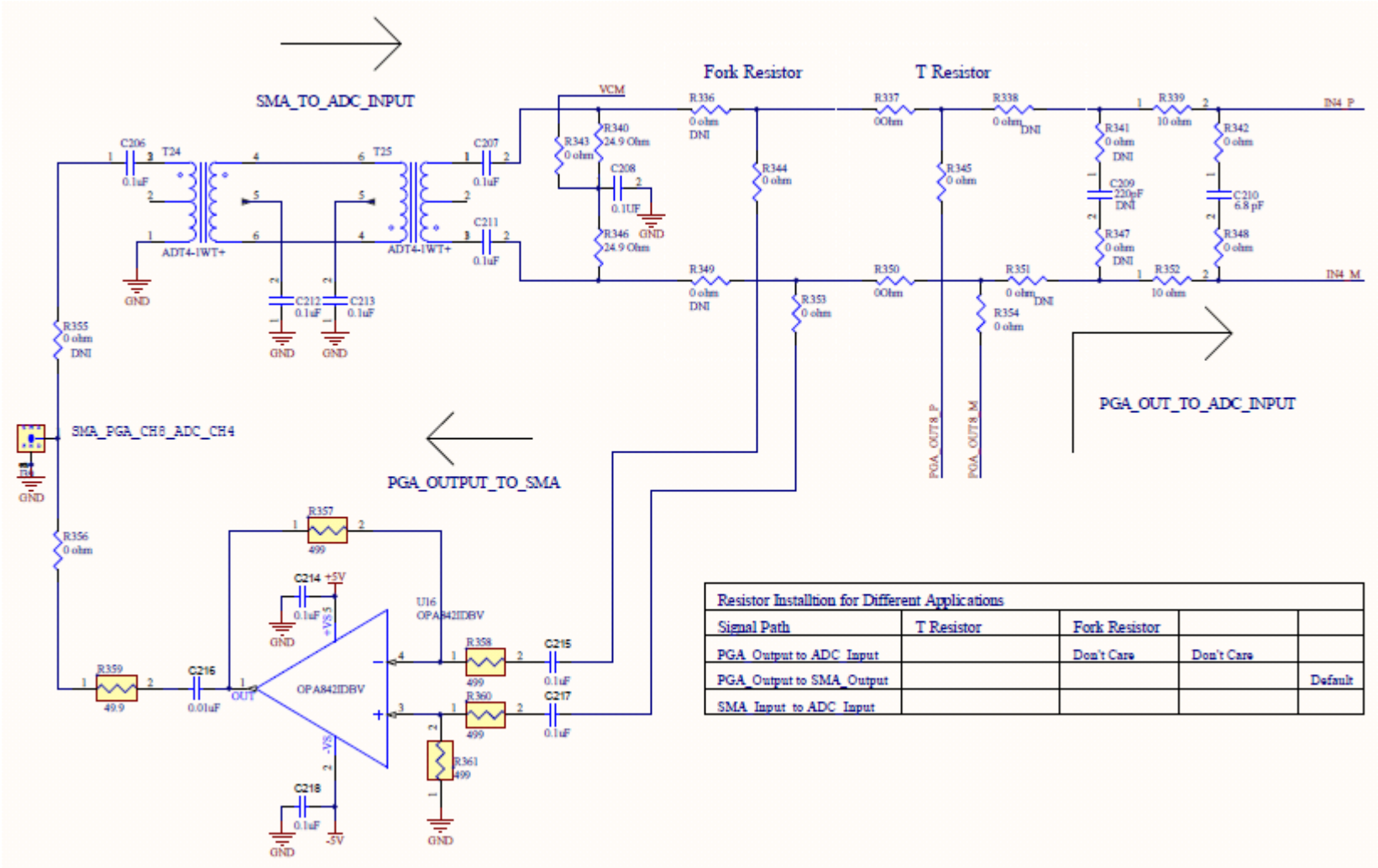


Figure 74. PGA5807 Schematic, (Sh. 12 of 16), PGA_CH7, ADC_CH3



Resistor Installtion for Different Applications				
Signal Path	T Resistor	Fork Resistor		
PGA_Output to ADC_Input		Don't Care	Don't Care	
PGA_Output to SMA_Output				Default
SMA_Input to ADC_Input				

Figure 75. PGA5807 Schematic, (Sh. 13 of 16), PGA_CH8, ADC_CH4

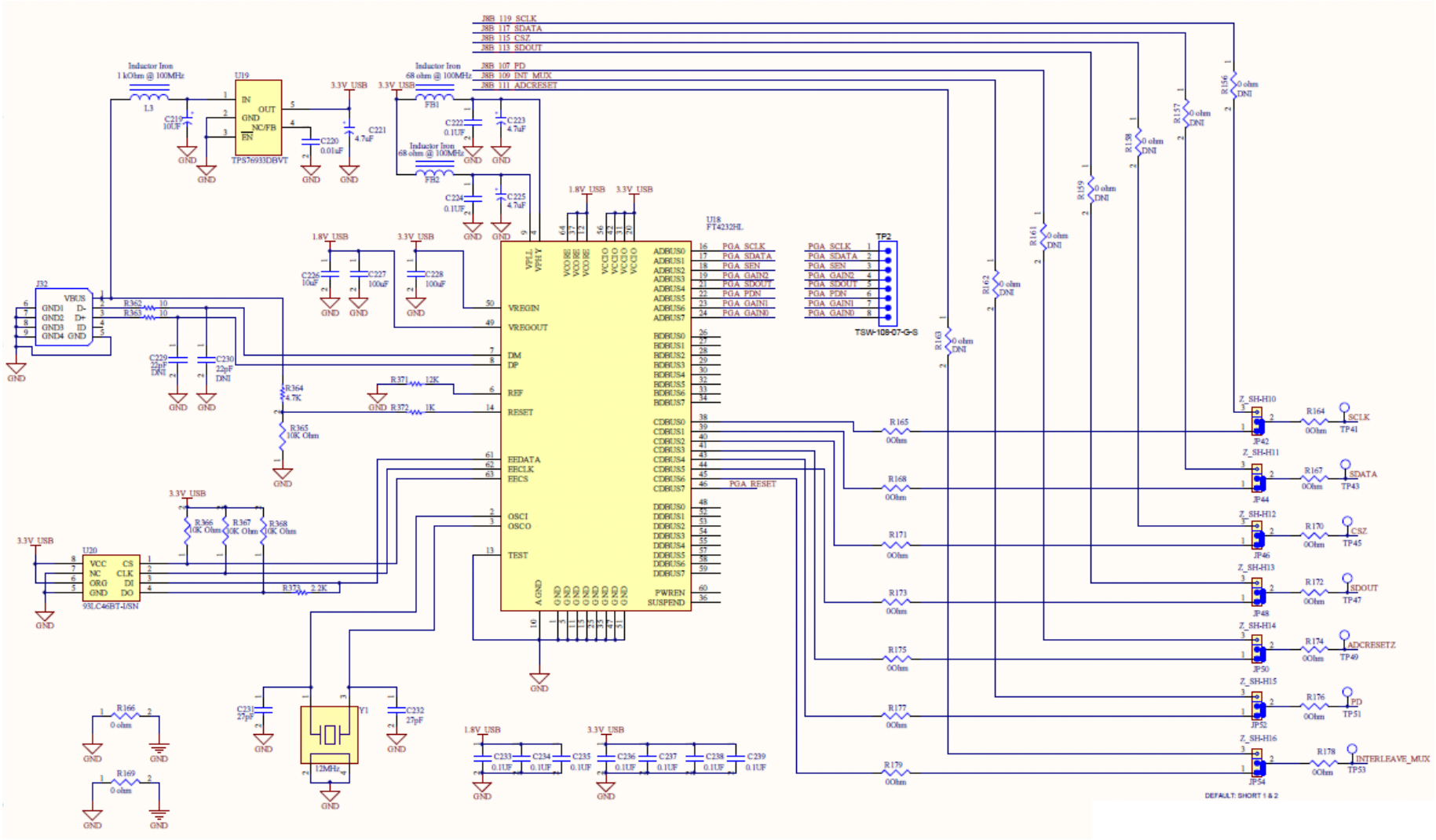


Figure 76. PGA5807 Schematic, (Sh. 14 of 16), FTDI Serial Interface

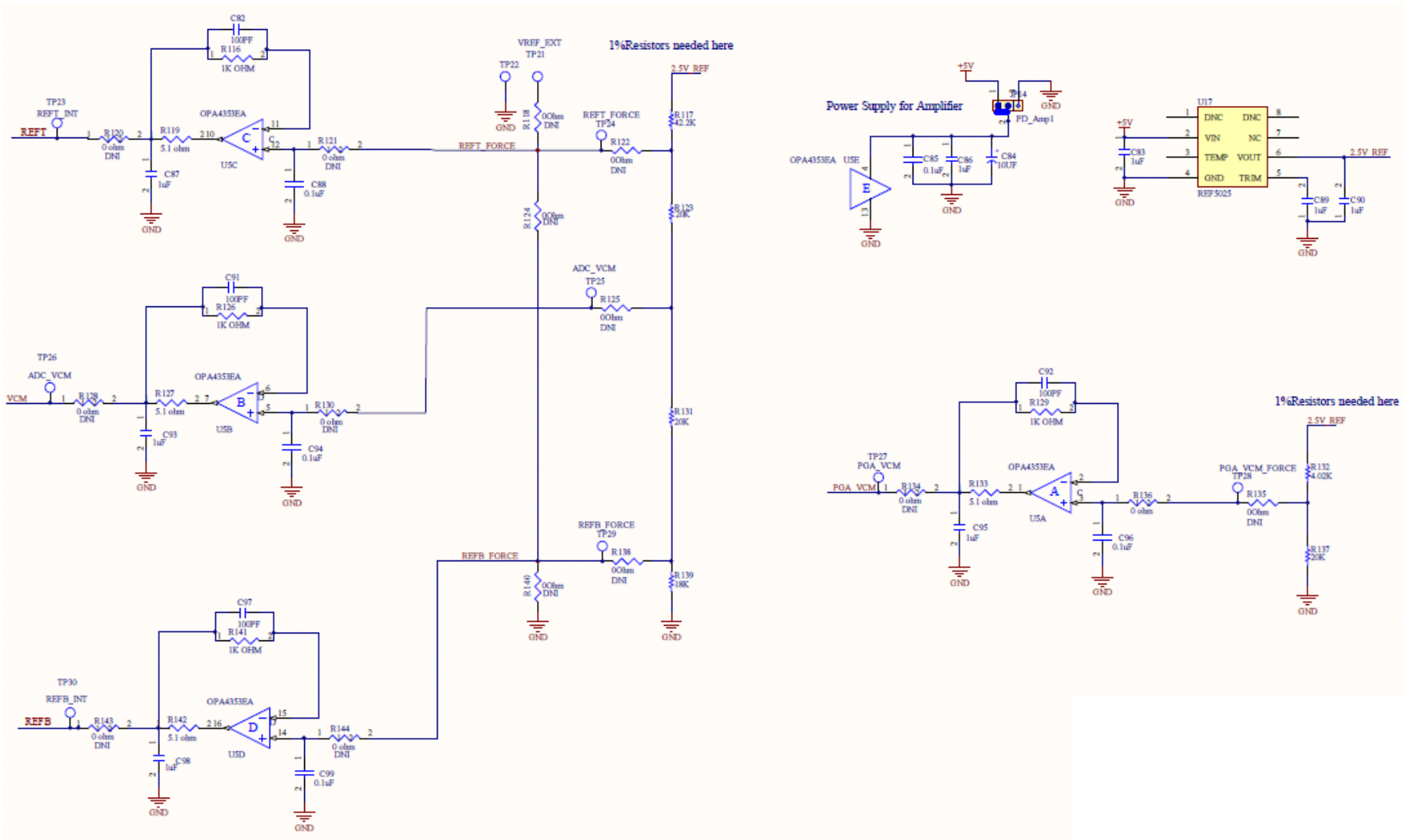


Figure 77. PGA5807 Schematic, (Sh. 15 of 16), ADS5296 External Reference

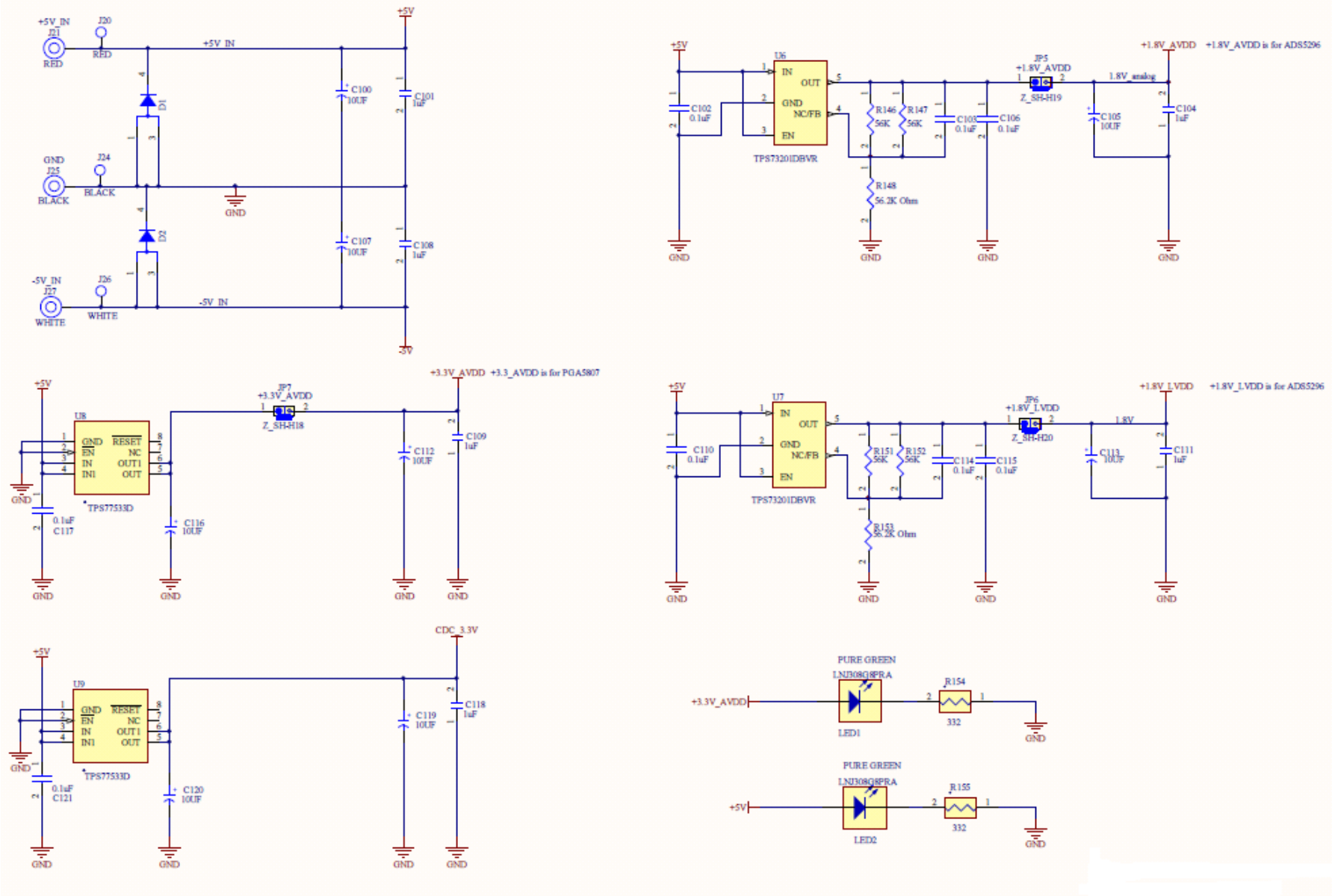


Figure 78. PGA5807 Schematic, (Sh. 16 of 16), Power Supply

7 PGA5807 EVM Bill of Materials

Table 2. PGA5807 EVM Bill of Materials

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
106	C1, C2, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C26, C28, C29, C30, C31, C32, C33, C34, C35, C36, C38, C40, C41, C42, C43, C44, C45, C46, C47, C48, C50, C52, C53, C54, C55, C56, C57, C58, C59, C60, C63, C64, C65, C66, C67, C68, C69, C70, C74, C75, C76, C85, C88, C94, C96, C99, C102, C103, C106, C110, C114, C115, C117, C121, C128, C129, C133, C134, C135, C141, C142, C146, C147, C148, C154, C155, C159, C160, C161, C167, C168, C172, C173, C174, C180, C181, C185, C186, C187, C193, C194, C198, C199, C200, C206, C207, C211, C212, C213	0.1uF	AVX	06035C104JAT2A	CAP CER .10UF 50V X7R 10% 0603
22	C4, C5, C6, C7, C8, C9, C78, C80, C137, C139, C150, C152, C163, C165, C176, C178, C189, C191, C202, C204, C215, C217	0.1uF	AVX	0402YC104KAT2A	CAP, CERAMIC, 0.1UF, 10%, 16V, X7R, SMT0402
16	C25, C27, C37, C39, C49, C51, C61, C62, C73, C132, C145, C158, C171, C184, C197, C210	6.8 pF	MURATA	GRM1885C1H6R8DZ01D	CAP CER 6.8PF 50V NP0 0603
8	C71, C130, C143, C156, C169, C182, C195, C208	0.1UF	TAIYO YUDEN	GMK105BJ104KV-F	0.1uF 35V X5R 0402
8	C72, C131, C144, C157, C170, C183, C196, C209	220pF	AVX	06035A221FAT2A	CAP CERM 220PF 1% 50V NP0 0603
16	C77, C81, C136, C140, C149, C153, C162, C166, C175, C179, C188, C192, C201, C205, C214, C218	0.1uF	KEMET	C0402C104K8PACTU	CAP, CERAMIC, 0.1UF, 10%, 10V, X5R, SMT0402
8	C79, C138, C151, C164, C177, C190, C203, C216	0.01uF	KEMET	C0402C103K3RACTU	CAP, CERAMIC, 0.01UF, 10%, 25V, X7R, SMT0402
4	C82, C91, C92, C97	100PF	Panasonic	ECH-U1C101JX5	CAP FILM 100PF 16VDC 0603
15	C3, C83, C86, C87, C89, C90, C93, C95, C98, C101, C104, C108, C109, C111, C118	1uF	AVX	0603YC105KAT2A	CAP CER 1.0UF 16V X7R 10% 0603
10	C84, C100, C105, C107, C112, C113, C116, C119, C120, C219	10UF	AVX	TAJB106K016RNJ	CAP TANT 10UF 16V 10% 1210
1	C220	0.01uF	MURATA	GRM155R71E103KA01D	CAP CER 0.01UF 25V 10% X7R 0402
3	C221, C223, C225	4.7uF	AVX	TAJA475K016RNJ	CAP TANT 4.7UF 16V 10% 1206
2	C222, C224	0.1UF	TAIYO YUDEN	EMK105BJ104KV-F	CAP CER 0.1UF 16V 10% X5R 0402
1	C226	10uF	MURATA	GRM188R60J106ME47D	CAP CER 10UF 6.3V 20% X5R 0603
2	C227, C228	100uF	KEMET	C1206C107M9PACTU	CAP CER 100UF 6.3V 20% X5R 1206
2	C229, C230	22pF	MURATA	GRM1885C2A220JA01D	CAP CER 22PF 100V 5% NP0 0603
2	C231, C232	27pF	Johanson Technology Inc	251R14S270GV4T	CAP CER 27PF 250V 2% NP0 0603
7	C233, C234, C235, C236, C237, C238, C239	0.1UF	MURATA	GRM188R71C104KA01D	CAP CER 0.1UF 16V 10% X7R 0603
2	D1, D2	MBRB2515L	ON Semiconductor	MBRB2515LT4G	DIODE SCHOTTKY 15V 25A D2PAK
1	DUT1		Texas Instruments	PGA5807	
2	FB1, FB2	68 ohm @ 100MHz	PANASONIC	EXC-ML32A680U	BEAD CORE 68 OHM 3A 1206 SMD
1	J1	QTH-060-02-F-D-A	SAMTEC	QTH-060-02-F-D-A	High speed connector
18	J2, J5, J10, J11, J12, J13, J14, J15, J16, J17, J18, J33, J34, J35, J36, J37, J38, J39	SMA	SAMTEC	SMA-J-P-H-ST-TH1	JACK PANEL MOUNT SMA
1	J21	RED	POMONA	1581-2	BANANA JACK, 15A, TURRET, RED
1	J25	BLACK	POMONA	1581-0	BANANA JACK, 15A, TURRET, BLACK
1	J27	WHITE	POMONA	1581-9	BANANA JACK, 15A, TURRET, WHITE
1	J32	USB_MINI_AB	JAE	DX3R005HN2E700	USB_MINI_AB
18	JP1, JP2, JP4, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP42, JP44, JP46, JP48, JP50, JP52, JP54	HEADER 3POS .1 CTR	Sullins Connector Solutions	PBC03SAAN	JUMPER,3P,.100CC
3	JP5, JP6, JP7	HEADER_1x2_100_430L	SAMTEC	HMTSW-102-07-G-S-240	CONN HEADER 2POS .100" T/H GOLD

Table 2. PGA5807 EVM Bill of Materials (continued)

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
1	L3	1 kOhm @ 100MHz	MURATA	BLM21AG102SN1D	FERRITE CHIP 1000 OHM 0805
2	LED1, LED2		PANASONIC	LNJ308G8PRA	LED, GREEN, SMT-0603
3	R1, R4, R7	10K Ohm	PANASONIC	ERJ-3EKF1002V	RES 10.0K OHM 1/10W 1% 0603 SMD
142	R2, R8, R11, R19, R21, R22, R23, R28, R30, R33, R35, R37, R39, R40, R41, R46, R47, R51, R53, R55, R57, R58, R59, R64, R66, R69, R71, R73, R75, R76, R77, R82, R83, R87, R89, R91, R92, R96, R97, R98, R99, R102, R105, R106, R107, R108, R109, R110, R136, R164, R165, R167, R168, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R181, R182, R186, R187, R188, R189, R192, R195, R196, R197, R198, R199, R200, R207, R208, R212, R213, R214, R215, R218, R221, R222, R223, R224, R225, R226, R233, R234, R238, R239, R240, R241, R244, R247, R248, R249, R250, R251, R252, R258, R259, R260, R264, R265, R270, R271, R273, R274, R277, R284, R285, R286, R290, R291, R296, R297, R299, R300, R303, R311, R316, R317, R318, R319, R322, R324, R327, R328, R330, R337, R342, R343, R344, R345, R348, R350, R353, R354, R356	0Ohm	PANASONIC	ERJ-3GEY0R00V	RESISTOR,SMT,0603,0 OHM,5%,ZERO OHM JUMPER
1	R5	49.9 Ohm	PANASONIC	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
33	R6, R18, R20, R32, R34, R36, R38, R50, R52, R54, R56, R68, R70, R72, R74, R86, R88, R93, R104, R183, R194, R209, R220, R235, R246, R261, R272, R287, R298, R313, R326, R339, R352	10 ohm	PANASONIC	ERJ-3GEYJ100V	RES 10.0 OHM 0603 SMD
2	R9, R10	100	Panasonic	ERJ-3GEYJ101V	RES 100 OHM 1/10W 5% 0603 SMD
2	R12, R13	130 OHM	VISHAY	CRCW0603130RFKEA	RESISTOR, THICK FILM, 130 OHM, 1%, 0.10W, SMT0603
75	R14, R15, R26, R27, R44, R45, R62, R63, R80, R81, R90, R95, R101, R103, R118, R120, R121, R122, R124, R125, R128, R130, R134, R135, R138, R140, R143, R144, R156, R157, R158, R159, R161, R162, R163, R180, R185, R191, R193, R206, R211, R217, R219, R232, R237, R243, R245, R263, R266, R267, R269, R275, R276, R278, R289, R292, R293, R295, R301, R302, R304, R310, R312, R315, R321, R323, R325, R329, R336, R338, R341, R347, R349, R351, R355	0 ohm	PANASONIC	ERJ-3GEY0R00V	RES 0.0 OHM 1/10W 0603 SMD
2	R16, R17	82 OHM	VISHAY	CRCW060382R0FKEA	RESISTOR, THICK FILM, 82 OHM, 1%, 0.10W, SMT0603
32	R24, R25, R29, R31, R42, R43, R48, R49, R60, R61, R65, R67, R78, R79, R84, R85, R94, R100, R184, R190, R210, R216, R236, R242, R262, R268, R288, R294, R314, R320, R340, R346	24.9 Ohm	PANASONIC	ERJ-3EKF24R9V	RES 24.9 OHM 1/10W 1% 0603 SMD
32	R111, R112, R114, R115, R201, R202, R204, R205, R227, R228, R230, R231, R253, R254, R256, R257, R279, R280, R282, R283, R305, R306, R308, R309, R331, R332, R334, R335, R357, R358, R360, R361	499	VISHAY DALE	CRCW0402499RFKED	RESISTOR, THICK FILM, 499 OHM, 1%, 0.063W, 100 PPM/K, SMT0402
8	R113, R203, R229, R255, R281, R307, R333, R359	49.9	VISHAY DALE	CRCW040249R9FKED	RESISTOR, THICK FILM, 49.9 OHM, 1%, 0.063W, 100 PPM/K, SMT0402
4	R116, R126, R129, R141	1K OHM	TYCO ELECTRONICS	CRG0603F1K0	RES 1.00K OHM 1/10W 1% 0603
1	R117	42.2K	VISHAY	CRCW060342K2FKEA	RESISTOR, THICK FILM, 42.2K OHM, 1%, 0.10W, SMT0603
4	R119, R127, R133, R142	5.1 ohm	VISHAY	CRCW06035R10FKEA	RES 5.10 OHM 1/10W 1% 0603 SMD
3	R123, R131, R137	20K	VISHAY	CRCW060320K0FKEA	RESISTOR, THICK FILM, 20K OHM, 1%, 0.10W, SMT0603
1	R132	4.02K	VISHAY	CRCW06034K02FKEA	RESISTOR, THICK FILM, 4.02K OHM, 1%, 0.10W, SMT0603
1	R139	18K	VISHAY	CRCW060318K0FKEA	RESISTOR, THICK FILM, 18K OHM, 1%, 0.10W, SMT0603
4	R146, R147, R151, R152	56K	PANASONIC	ERJ-3EKF5602V	RES 56.0K OHM 1/10W 1% 0603 SMD
2	R148, R153	56.2K Ohm	PANASONIC	ERJ-3EKF5622V	RES 56.2K OHM 1/10W 1% 0603 SMD
2	R154,R155	332	PANASONIC	ERJ-2RKF3320X	RESISTOR, THICK FILM, 332 OHM, 1%, 0.1W, SMT0402

Table 2. PGA5807 EVM Bill of Materials (continued)

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
2	R166, R169	0 ohm	PANASONIC	ERJ-2GE0R00X	RES 0 OHM 1/16W 1% 0402 SMD
2	R362, R363	10	YAGEO	RC0603FR-0710RL	RES 10.0 OHM 1/10W 1% 0603 SMD
1	R364	4.7K	PANASONIC	ERJ-2RKF4701X	RES 4.70K OHM 1/10W 1% 0402 SMD
4	R365, R366, R367, R368	10K Ohm	PANASONIC	ERJ-2RKF1002X	RES 10.0K OHM 1/10W 1% 0402 SMD
1	R371	12K	PANASONIC	ERJ-3EKF1202V	RES 12.0K OHM 1/10W 1% 0603 SMD
1	R372	1K OHM	PANASONIC	ERJ-3EKF1001V	RES 1.00K OHM 1/10W 1% 0603 SMD
1	R373	2.2K	PANASONIC	ERJ-2RKF2201X	RES 2.20K OHM 1/10W 1% 0402 SMD
1	T1	TC4-1WG2+	Mini-Circuits	TC4-1WG2+	
7	T2, T3, T4, T5, T6, T7, T8, T9,	ADT1-1WT+	Mini-Circuits	ADT1-1WT+	TRANSFORMER, RF, 50 OHM, 2 MHZ TO 755 MHZ, 6-PIN, ROHS
17	T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, T24, T25	ADT4-1WT	Mini-Circuits	ADT4-1WT+	TRANSFORMER, RF, 50 OHM, 2 MHZ TO 755 MHZ, 6-PIN, ROHS
2	TP1, TP3		Samtec, Inc.	TSW-108-07-G-S	Header, TH, 100mil, 8x1, Gold plated, 230 mil above insulator
1	TP2		Samtec, Inc.	TSW-108-07-G-S	Header, TH, 100mil, 8x1, Gold plated, 230 mil above insulator
19	TP18, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP41, TP43, TP45, TP47, TP49, TP51, TP53, J24		Keystone	5001	Tespoints, Black
1	J20		Keystone	5000	Tespoints, Red
1	J26		Keystone	5002	Tespoints, White
1	U1	ADS5296	Texas Instruments	ADS5296IRGC	TI Supplied Device
1	U2	80 MHZ	ECS INC	ECS-3953M-800-BN	OSCILLATOR, 80 MHZ, 4-PIN
1	U3	CDCLVP1102	Texas Instruments	CDCLVP1102RGTT	IC CLK BUFF 1:2 LVPECL SGL 16QFN
8	U4, U10, U11, U12, U13, U14, U15, U16		TEXAS INSTRUMENTS	OPA842IDBVT	IC, WIDEBAND, LOW DISTORTION, UNITY-GAIN STABLE, VOLTAGE-FEEDBACK OPAMP, SOT23-5, DBV
1	U5	2.7 V TO 5.5 V	TEXAS INSTRUMENTS	OPA4353EA/250	IC OPAMP GP R-R 44MHZ 16QSOP
2	U6, U7	TPS73201-SOT23	Texas Instruments	TPS73201DBVR	IC LDO REG 250MA ADJ-V SOT23-5
2	U8, U9	TPS77533D	Texas Instruments	TPS77533D	IC 3.3V 500MA LDO REG 8-SOIC
1	U17		Texas Instruments	REF5025AID	IC,SMT,SOIC-8
1	U18		FTDI	FT4232HL-REEL	IC USB HS QUAD UART/SYNC 64-LQFP
1	U19		Texas Instruments	TPS76933DBVT	IC REG LDO 3.3V .1A SOT-23-5
1	U20		Microchip Technology	93LC46BT-I/SN	IC EEPROM 1KBIT 2MHZ 8SOIC
1	Y1	12 MHz		ABM8G-12.000MHZ-B4Y-T	CRYSTAL 12.000MHZ 10PF SMD
21	PD_Amp1, Z_SH-H1, Z_SH-H2, Z_SH-H3, Z_SH-H4, Z_SH-H5, Z_SH-H6, Z_SH-H7, Z_SH-H8, Z_SH-H9, Z_SH-H10, Z_SH-H11, Z_SH-H12, Z_SH-H13, Z_SH-H14, Z_SH-H15, Z_SH-H16, Z_SH-H17, Z_SH-H18, Z_SH-H19, Z_SH-H20	SHUNT-HEADER	Keltron	MJ-5.97-G-F1 or equivalent	SHUNT FOR HEADER
8		SCREW STEEL M3 THR 6MM	Digi-Key	29311	SCREW STEEL M3 THR 6MM
8		STANDOFF HEX M3 THR ALUM 18MM	Digi-Key	24436	STANDOFF HEX M3 THR ALUM 18MM

8 PGA5807 EVM Layout

Figure 79 through Figure 86 illustrate the PCB layouts for the EVM.

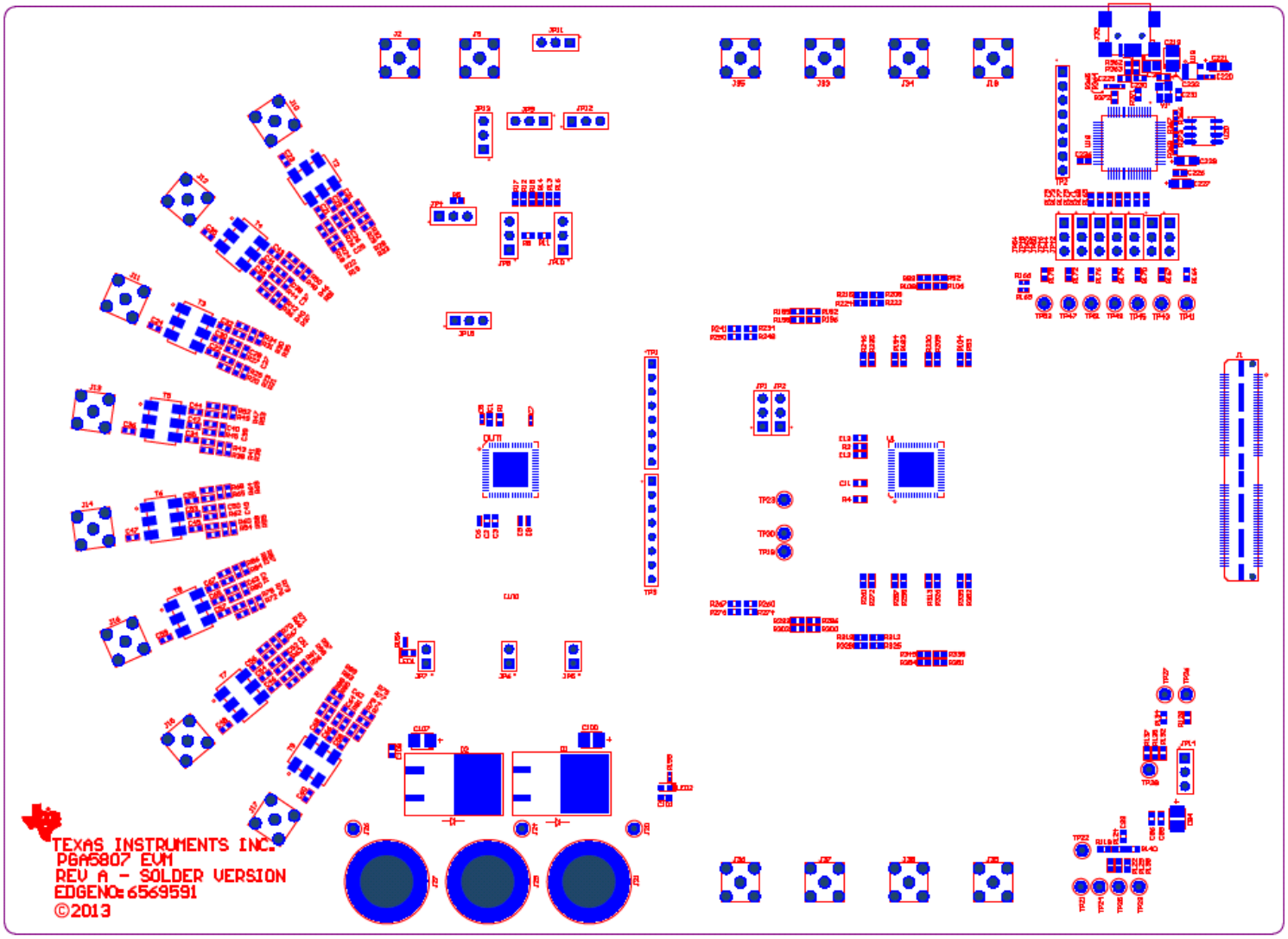


Figure 79. PGA5807 EVM Top Layer Assembly Drawing – Top View

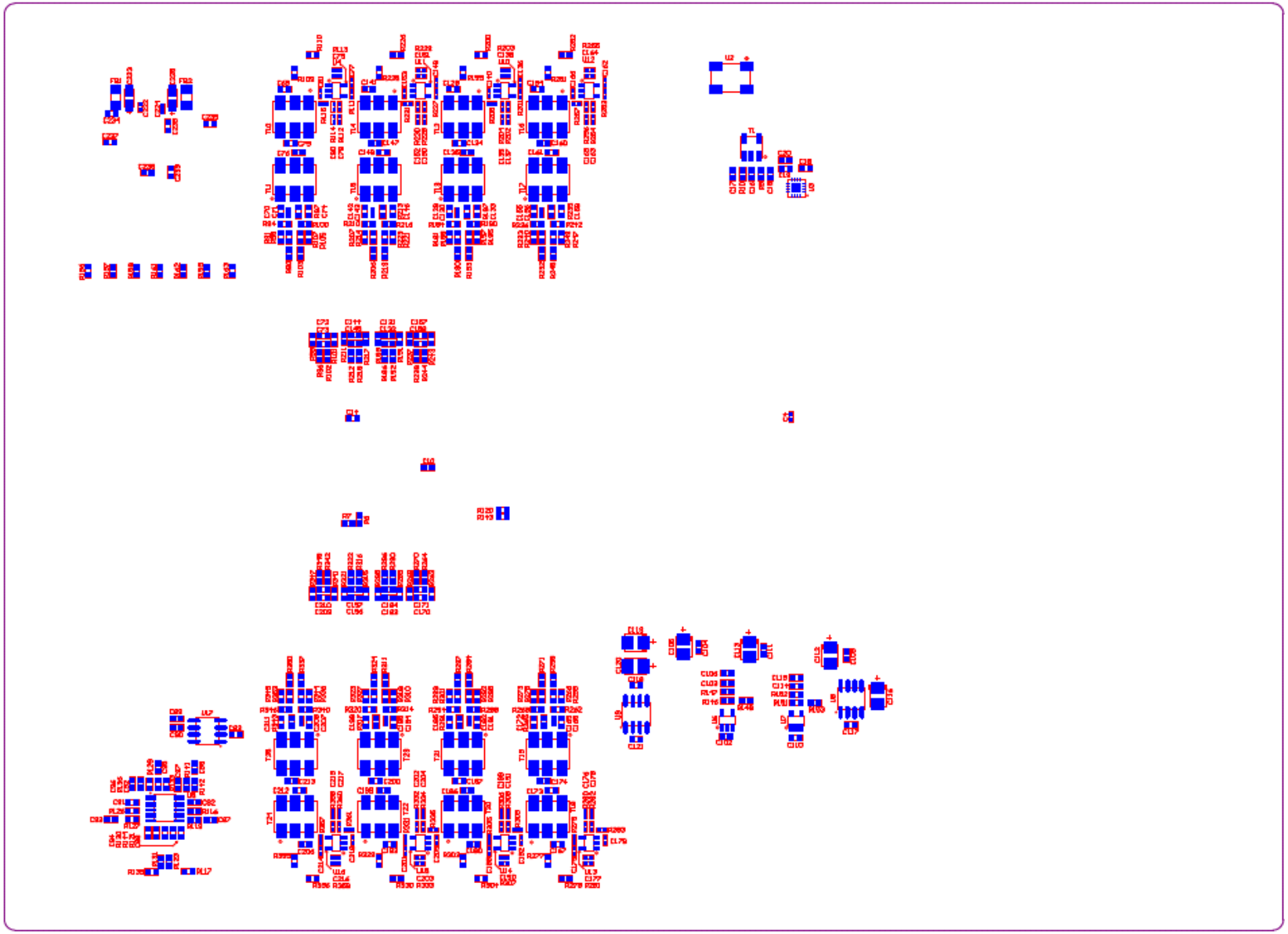


Figure 80. PGA5807 EVM Bottom Layer Assembly Drawing – Bottom View

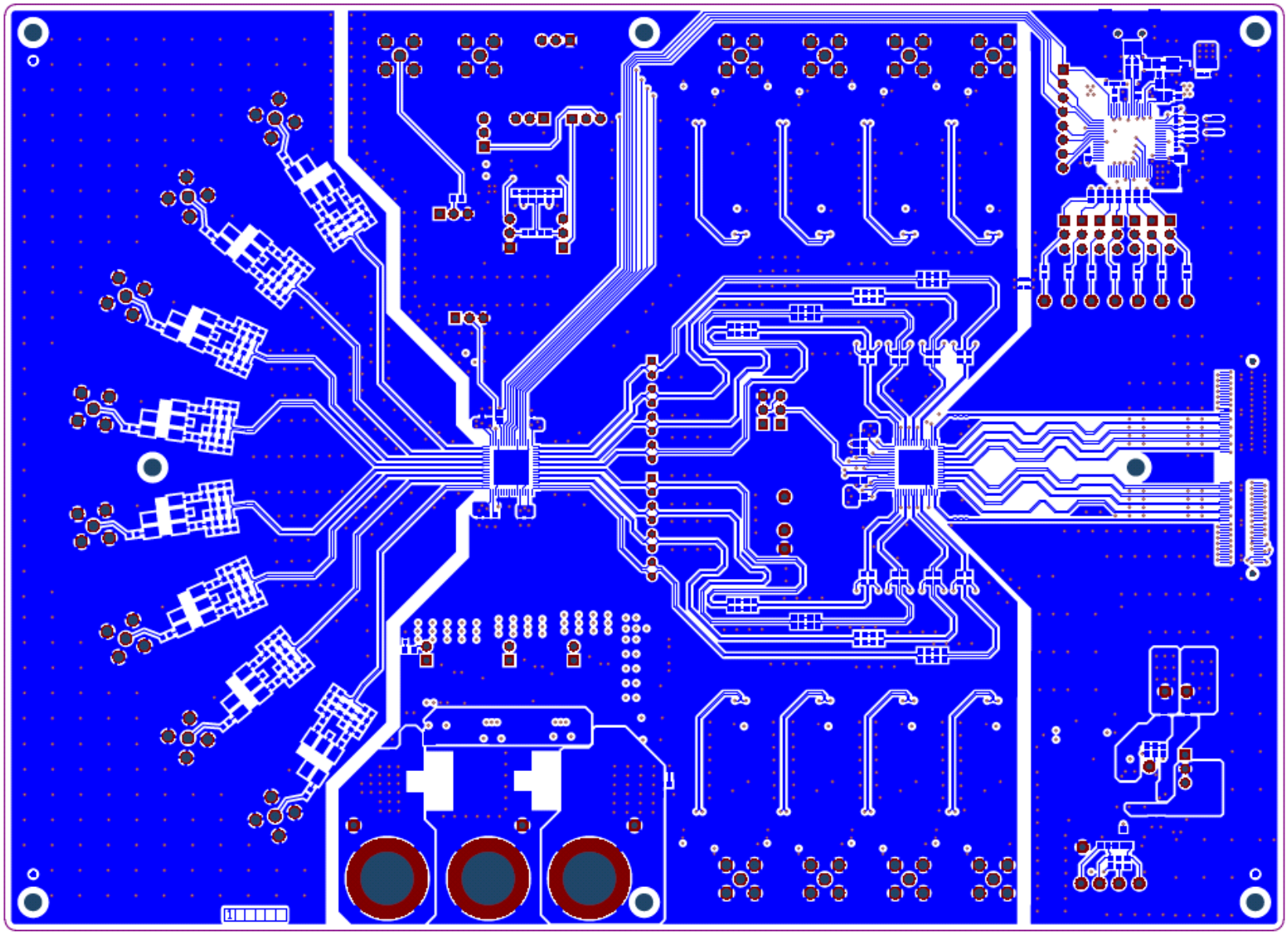


Figure 81. PGA5807 EVM Top Side

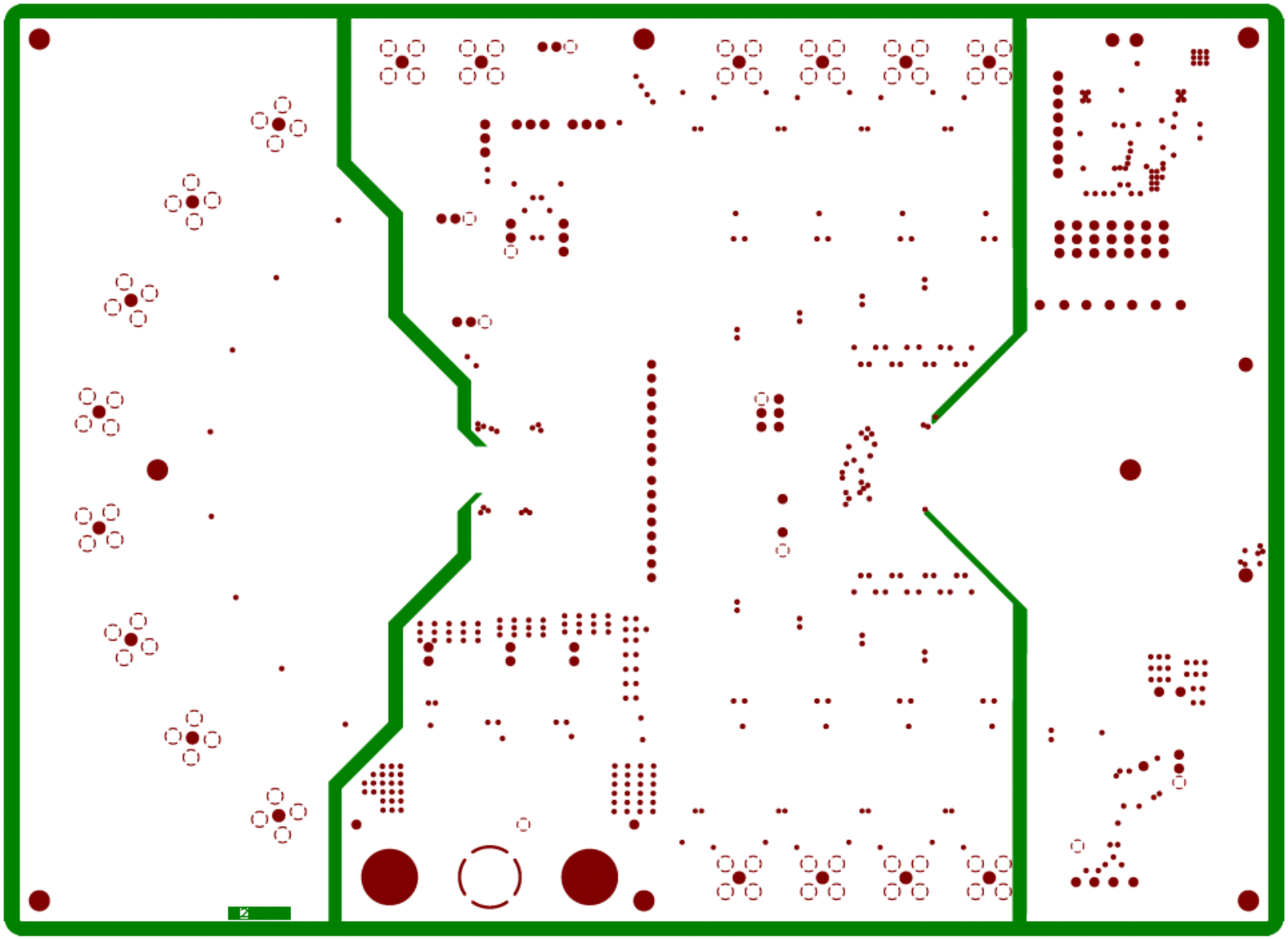


Figure 82. PGA5807 EVM Ground Plane 1

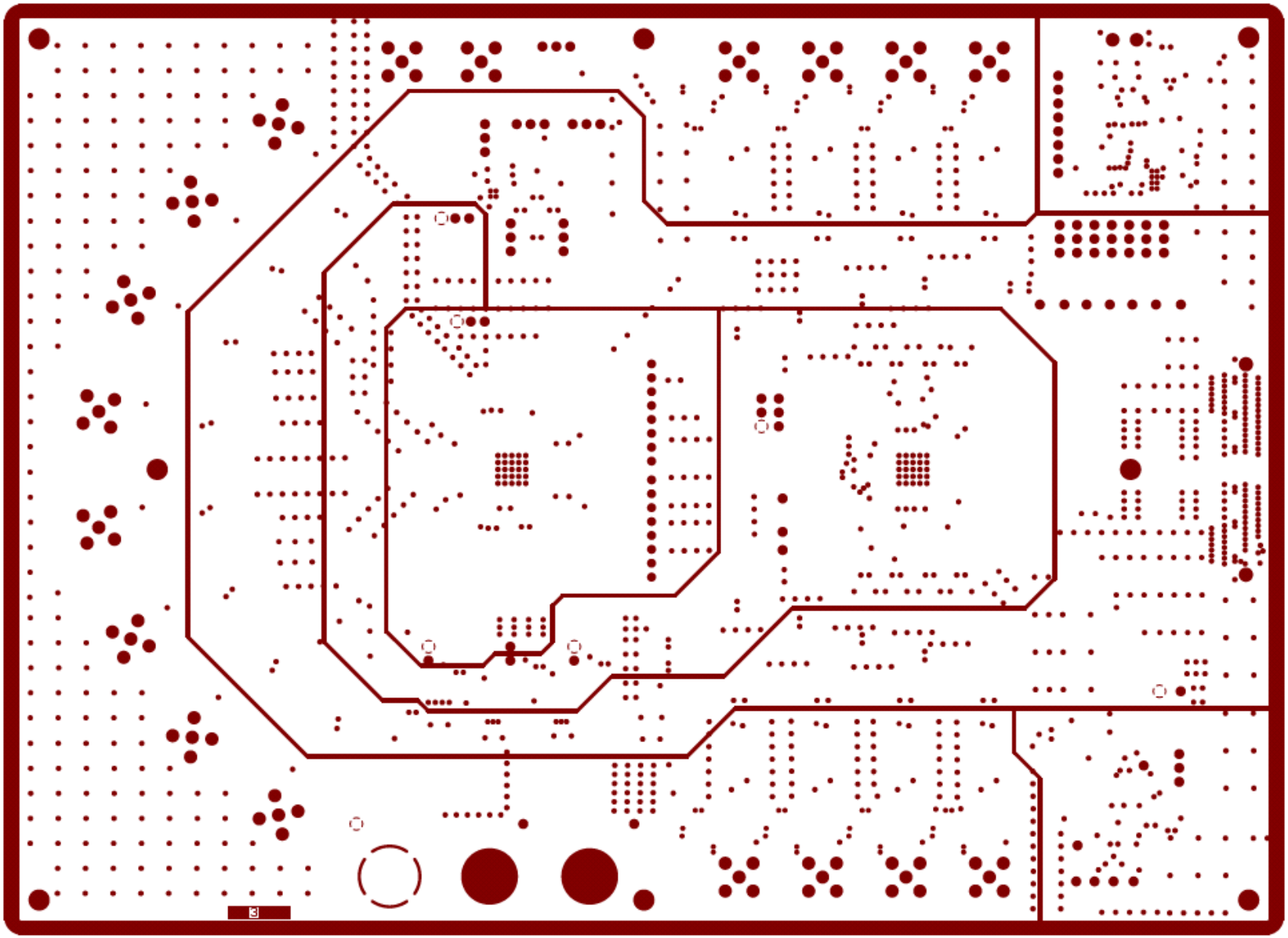


Figure 83. PGA5807 EVM Power Split Plane 1

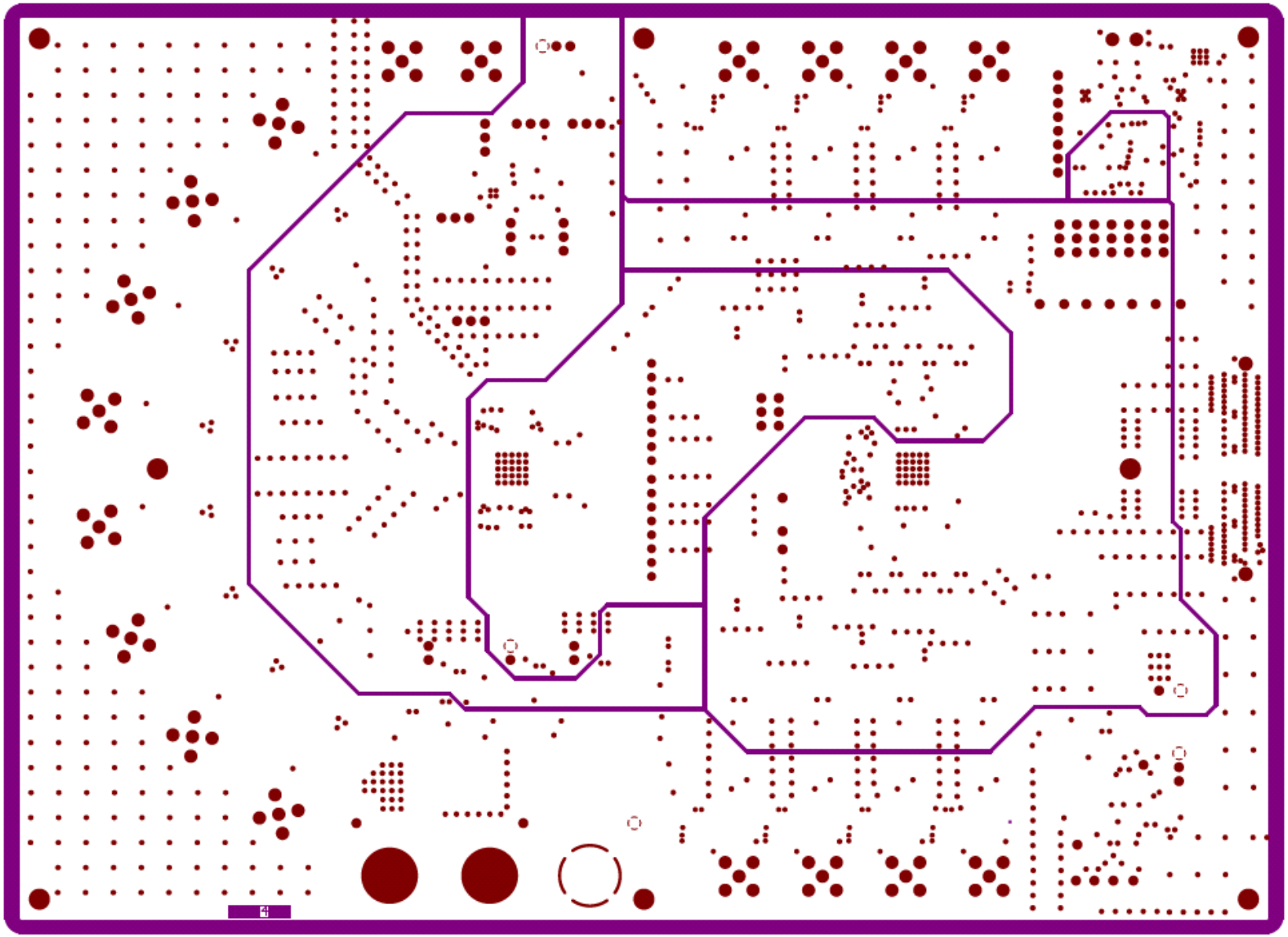


Figure 84. PGA5807 EVM Power Split Plane 2

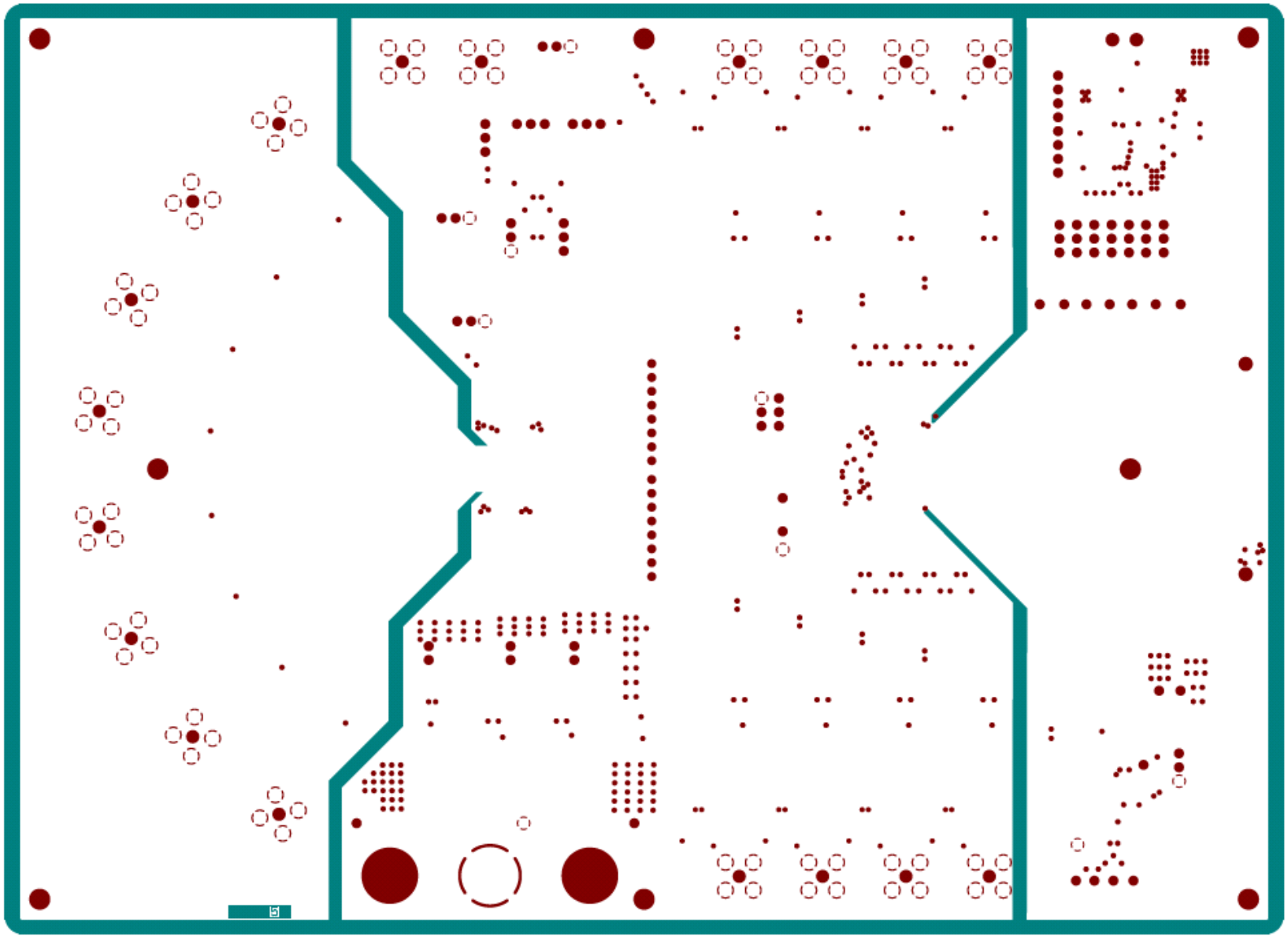


Figure 85. PGA5807 EVM GND Split Plane 2

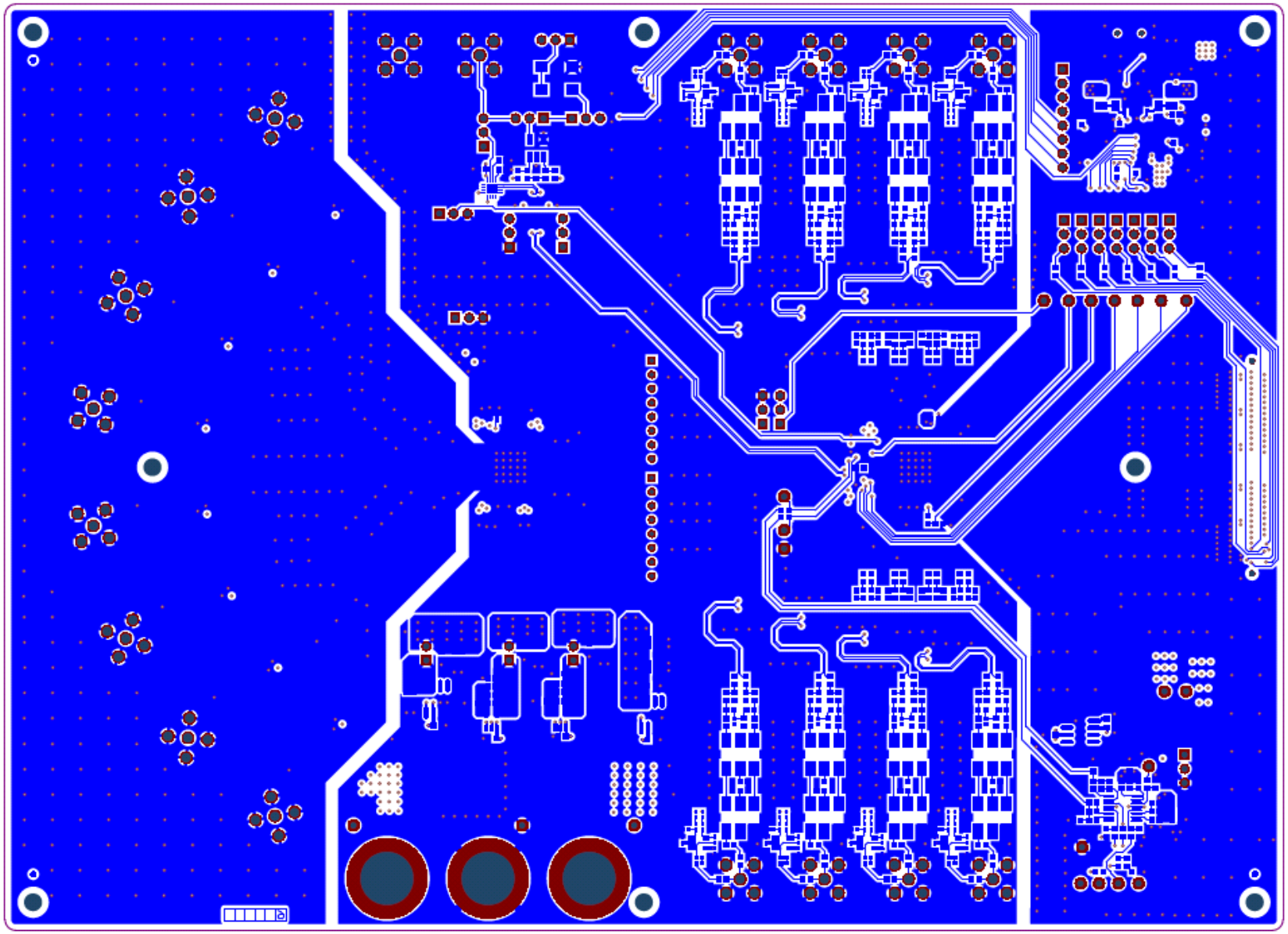


Figure 86. PGA5807 EVM Bottom Side

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Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
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http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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