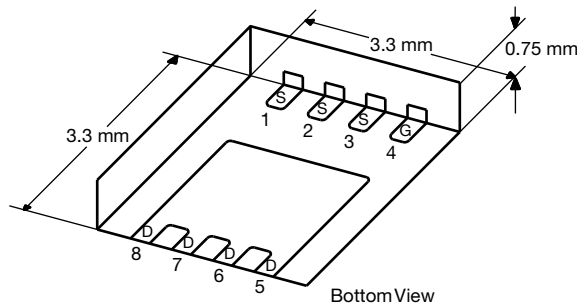


P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 20	0.0045 at V _{GS} = - 4.5 V	- 50 ^e	93 nC
	0.0063 at V _{GS} = - 2.5 V	- 50 ^e	
	0.0115 at V _{GS} = - 1.8 V	- 50 ^e	

PowerPAK 1212-8S



Ordering Information:
SiSS23DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

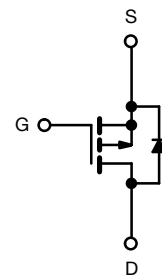
- TrenchFET[®] Power MOSFET
- Low Thermal Resistance PowerPAK[®] Package with Small Size and Low 0.75 mm Profile
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Smart Phones, Tablet PCs, Mobile Computing
 - Battery Switch
 - Load Switch
 - Power Management
 - Battery Management



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	- 20	V
Gate-Source Voltage		V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	- 50 ^e	A
	T _C = 70 °C		- 50 ^e	
	T _A = 25 °C		- 27 ^{a, b}	
	T _A = 70 °C		- 21 ^{a, b}	
Pulsed Drain Current (t = 100 μs)		I _{DM}	- 200	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	- 47.5	
	T _A = 25 °C		- 4 ^{a, b}	
Avalanche Current	L = 0.1 mH	I _{AS}	- 23	
Single-Pulse Avalanche Energy		E _{AS}	26	mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	57	W
	T _C = 70 °C		36	
	T _A = 25 °C		4.8 ^{a, b}	
	T _A = 70 °C		3 ^{a, b}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}			260	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Package limited.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	21	26	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.7	2.2	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 63 °C/W.

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = -250$ μ A	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250$ μ A		-12		mV/ °C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ μ A	-0.4		-0.9	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20$ V, $V_{GS} = 0$ V			-1	μ A
		$V_{DS} = -20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -4.5$ V	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -20$ A		0.0035	0.0045	Ω
		$V_{GS} = -2.5$ V, $I_D = -10$ A		0.0051	0.0063	
		$V_{GS} = -1.8$ V, $I_D = -10$ A		0.0081	0.0115	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10$ V, $I_D = -20$ A		44		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -15$ V, $V_{GS} = 0$ V, $f = 1$ MHz		8840		pF
Output Capacitance	C_{oss}			835		
Reverse Transfer Capacitance	C_{rss}			900		
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -20$ A		195	300	nC
				93	140	
Gate-Source Charge	Q_{gs}	$V_{DS} = -15$ V, $V_{GS} = -4.5$ V, $I_D = -20$ A		12		nC
Gate-Drain Charge	Q_{gd}			21		
Gate Resistance	R_g		$f = 1$ MHz	0.5	2.6	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 1$ Ω $I_D \cong -10$ A, $V_{GEN} = -4.5$ V, $R_g = 1$ Ω		45	90	ns
Rise Time	t_r			50	100	
Turn-Off Delay Time	$t_{d(off)}$			140	280	
Fall Time	t_f			50	100	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 1$ Ω $I_D \cong -10$ A, $V_{GEN} = -10$ V, $R_g = 1$ Ω		15	30	ns
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(off)}$			150	300	
Fall Time	t_f			40	80	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C			-50 ^c	A
Pulse Diode Forward Current ^d	I_{SM}				-200	
Body Diode Voltage	V_{SD}	$I_F = -10$ A		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -10$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			15	30	nC
Reverse Recovery Fall Time	t_a			16		ns
Reverse Recovery Rise Time	t_b			14		

Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

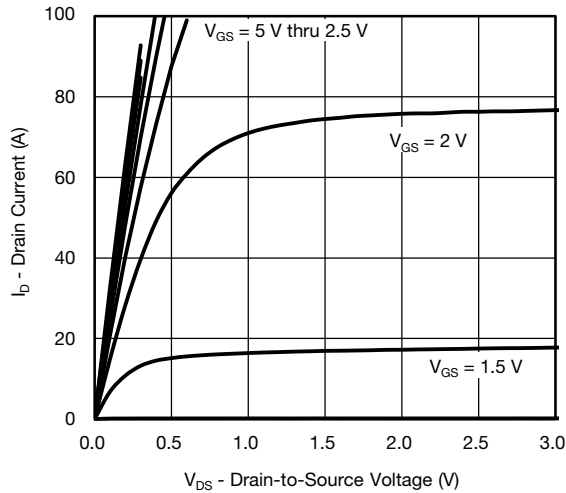
b. Guaranteed by design, not subject to production testing.

c. Package limited.

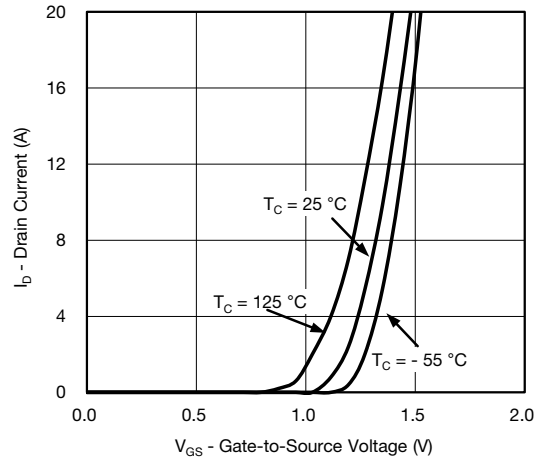
d. $t = 100$ μ s.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

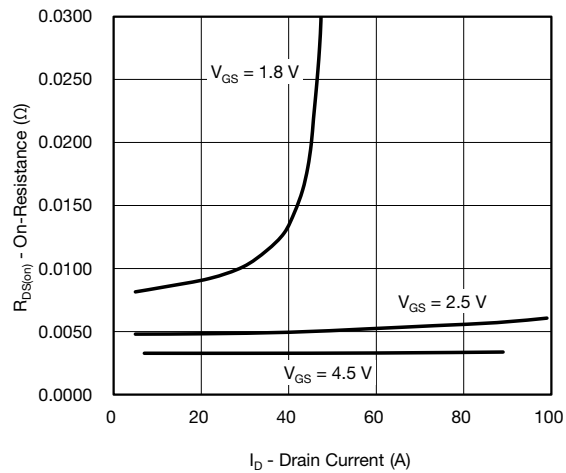
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



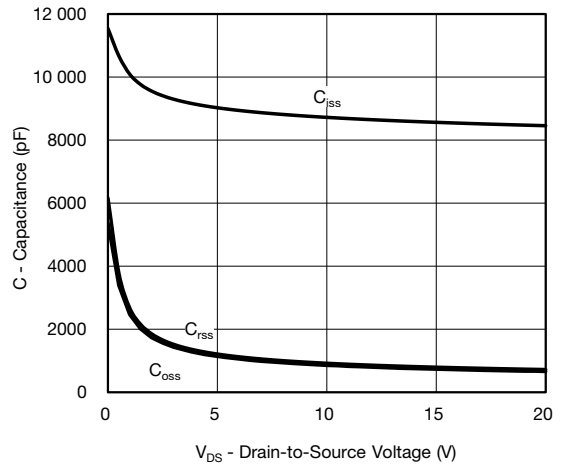
Output Characteristics



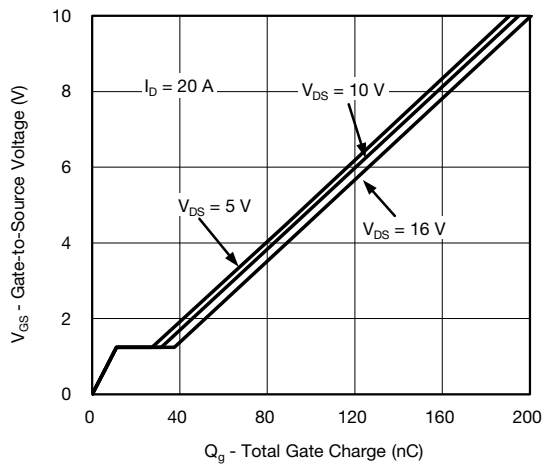
Transfer Characteristics



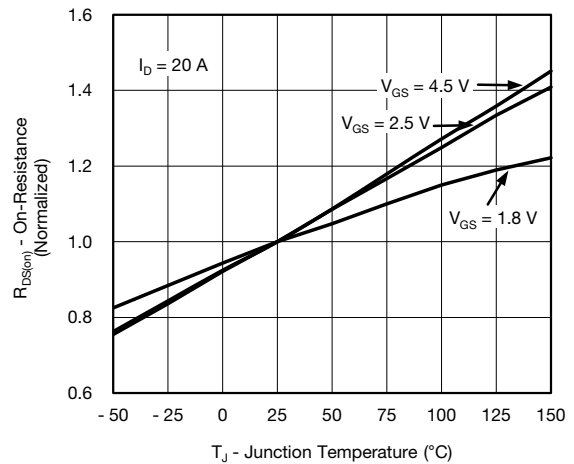
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

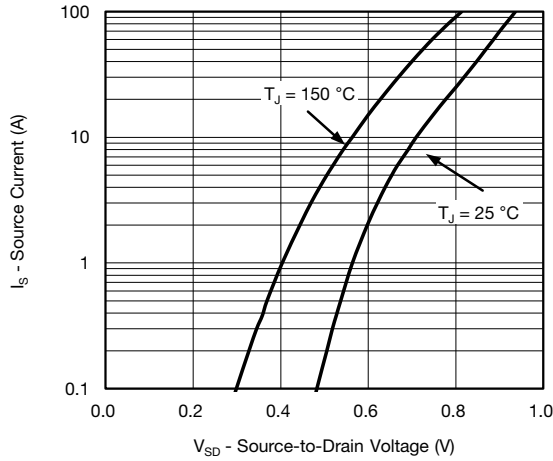


Gate Charge

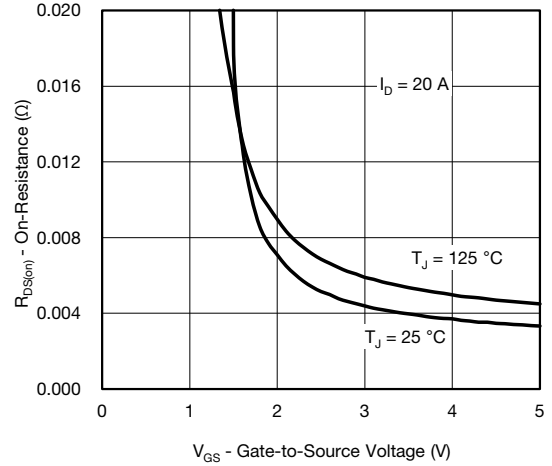


On-Resistance vs. Junction Temperature

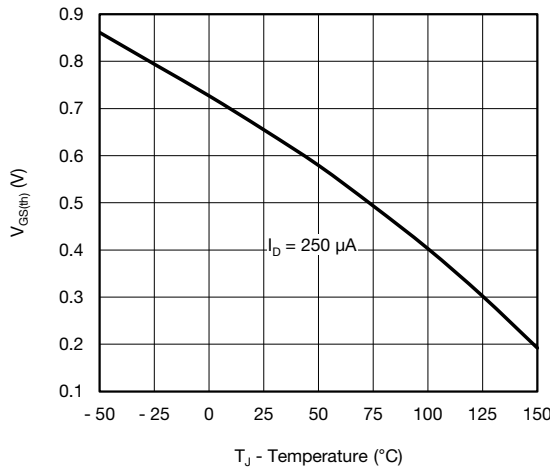
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



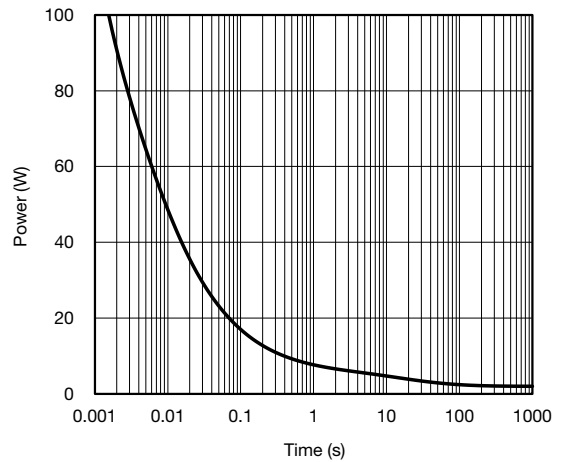
Source-Drain Diode Forward Voltage



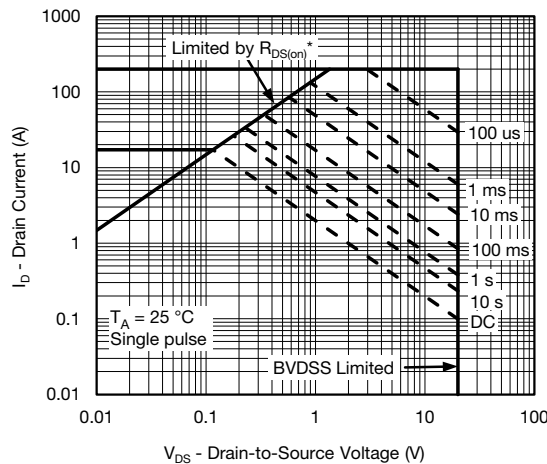
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

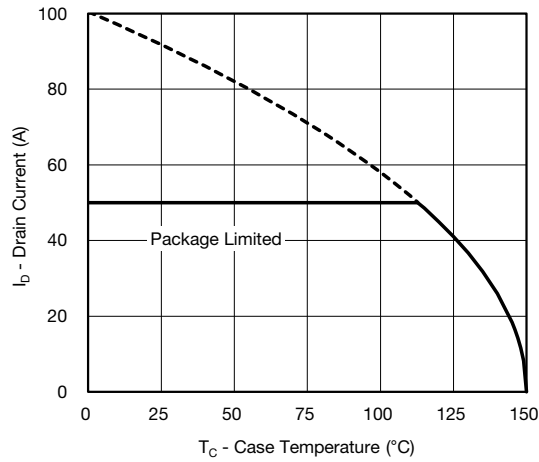


Single Pulse Power, Junction-to-Ambient

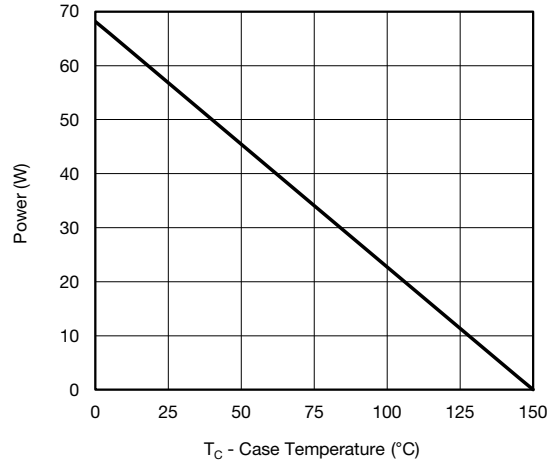


Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

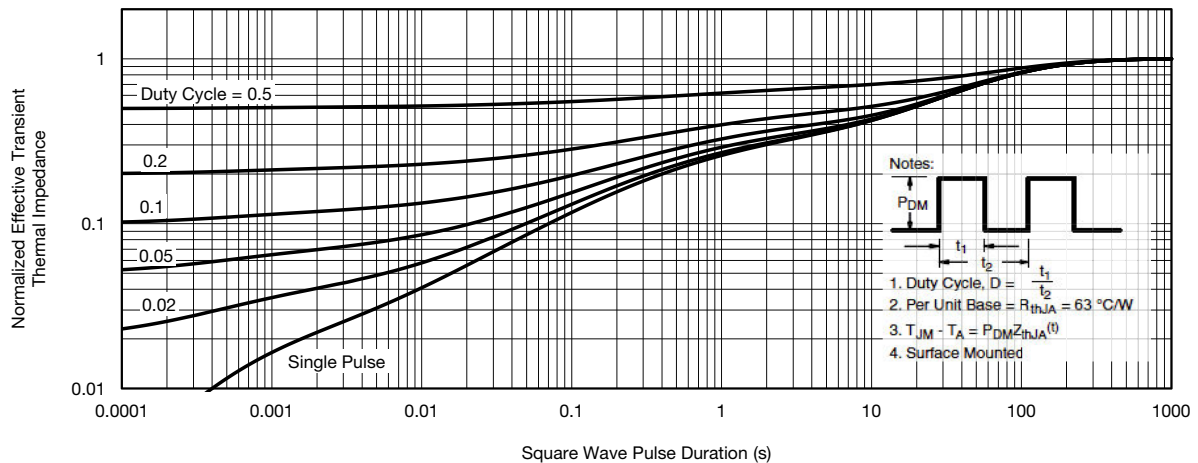


Current Derating*



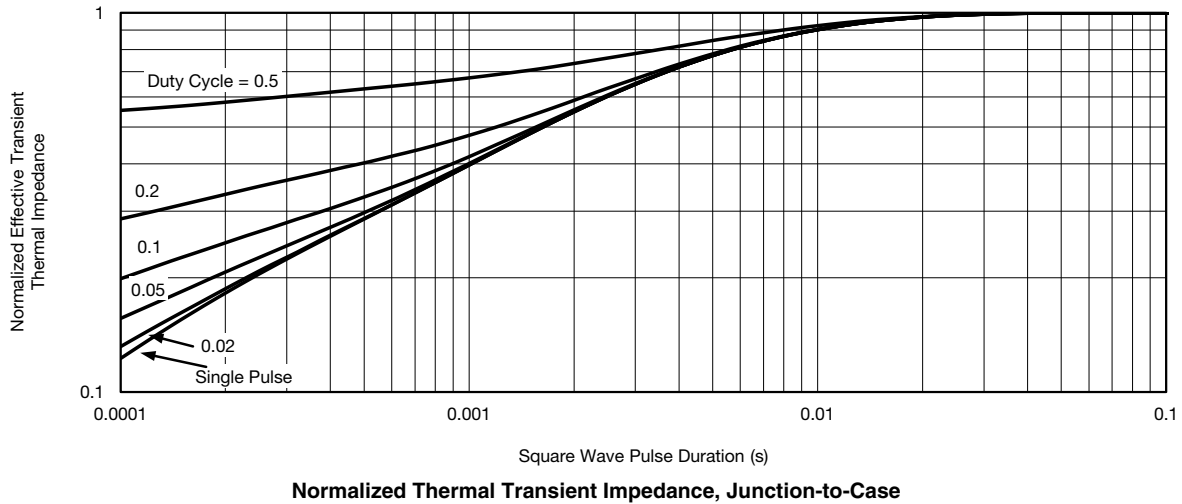
Power, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62852.

Case Outline for PowerPAK® 1212-8S


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: C20-0862-Rev. B, 20-Jul-2020
DWG: 6008

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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