

N-Channel 60 V (D-S) MOSFET



FEATURES

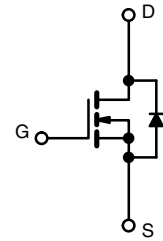
- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS} - Q_g$ figure-of-merit (FOM)
- Tuned for the lowest $R_{DS} - Q_{oss}$ FOM
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Solar micro inverter
- Motor drive switch
- Battery and load switch
- Industrial



N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00175
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.00240
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 6$ V	0.00340
Q_g typ. (nC)	42.5
I_D (A)	165
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR626ADP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	300	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	5.6 ^{b, c}
Single pulse avalanche current	I_{AS}	50	mJ
Single pulse avalanche energy	E_{AS}	125	
Maximum power dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s



THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^a	t ≤ 10 s	R _{thJA}	15	20	°C/W	
Maximum junction-to-case (drain)	Steady state	R _{thJC}	0.9	1.2		

Notes

a. Surface mounted on 1" x 1" FR4 board

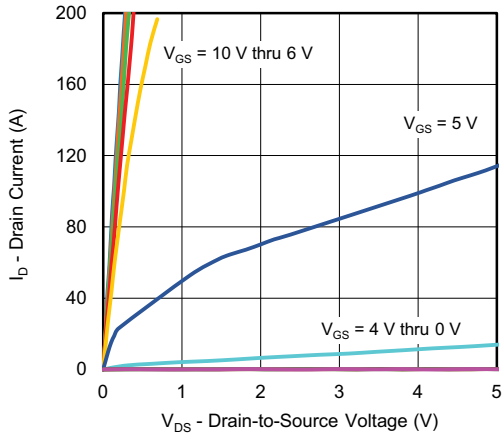
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 1 mA	-	32	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-7.8	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	3.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	40	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00145	0.00175	Ω
		V _{GS} = 7.5 V, I _D = 20 A	-	0.00190	0.00240	
		V _{GS} = 6 V, I _D = 20 A	-	0.00260	0.00340	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A	-	84	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	-	3770	-	pF
Output capacitance	C _{oss}		-	1370	-	
Reverse transfer capacitance	C _{rss}		-	40	-	
Total gate charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 20 A	-	55	83	nC
Gate-source charge	Q _{gs}	V _{DS} = 30 V, V _{GS} = 7.5 V, I _D = 20 A	-	42.5	64	
Gate-drain charge	Q _{gd}		-	16.7	-	
Output charge	Q _{oss}		-	9.2	-	
Gate resistance	R _g		V _{DS} = 30 V, V _{GS} = 0 V f = 1 MHz	0.3	0.9	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, R _L = 1.5 Ω, I _D ≅ 20 A, V _{GEN} = 10 V, R _g = 1 Ω	-	16	32	ns
Rise time	t _r		-	10	20	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, R _L = 1.5 Ω, I _D ≅ 20 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	20	40	
Rise time	t _r		-	20	40	
Turn-off delay time	t _{d(off)}		-	27	54	
Fall time	t _f		-	12	24	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	100	A
Pulse diode forward current	I _{SM}		-	-	300	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.7	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C	-	52	104	ns
Body diode reverse recovery charge	Q _{rr}		-	50	100	nC
Reverse recovery fall time	t _a		-	25	-	ns
Reverse recovery rise time	t _b		-	27	-	

Notes

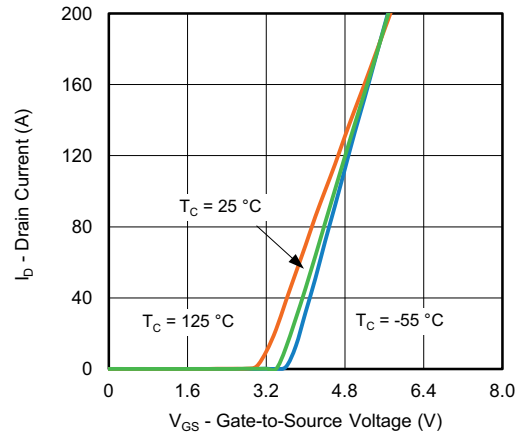
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

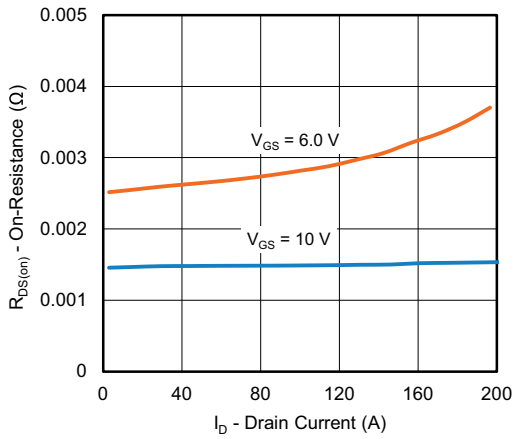
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



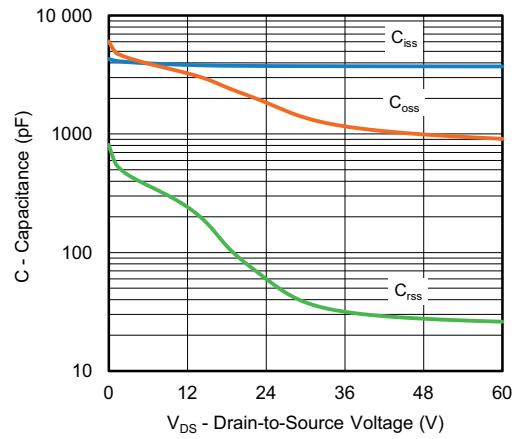
Output Characteristics



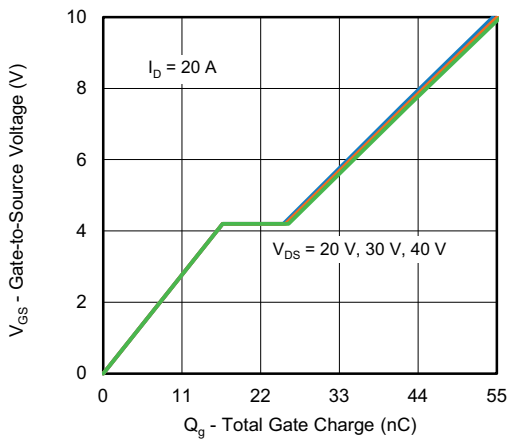
Transfer Characteristics



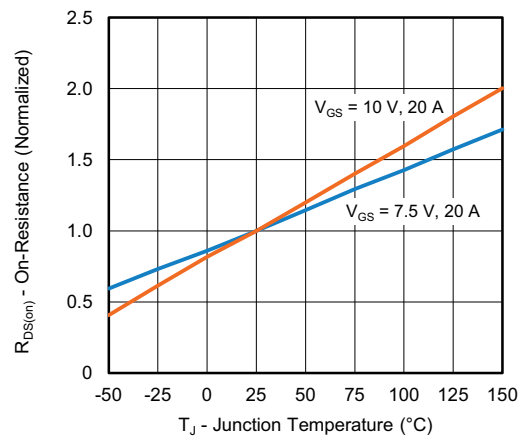
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



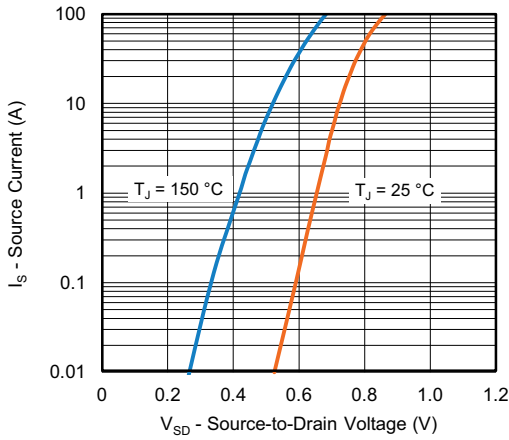
Gate Charge



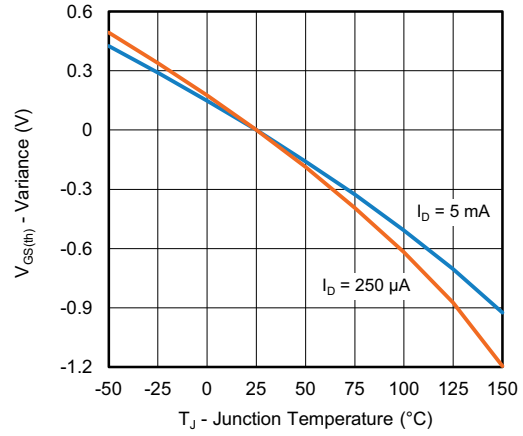
On-Resistance vs. Junction Temperature



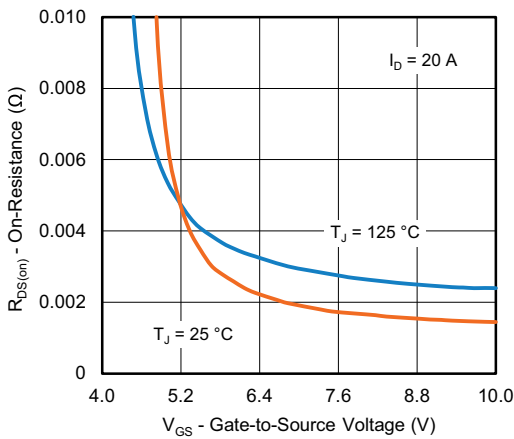
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



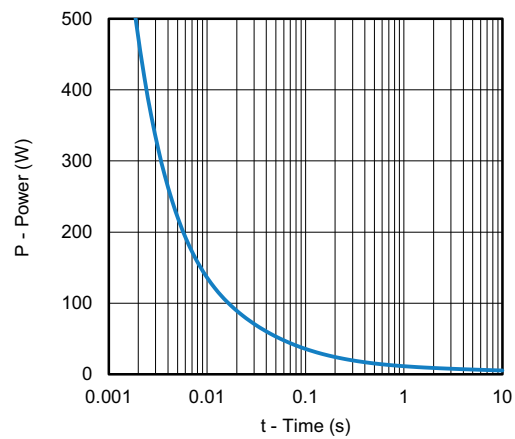
Source-Drain Diode Forward Voltage



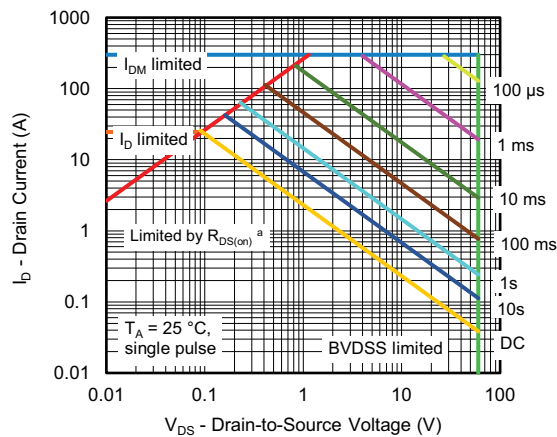
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



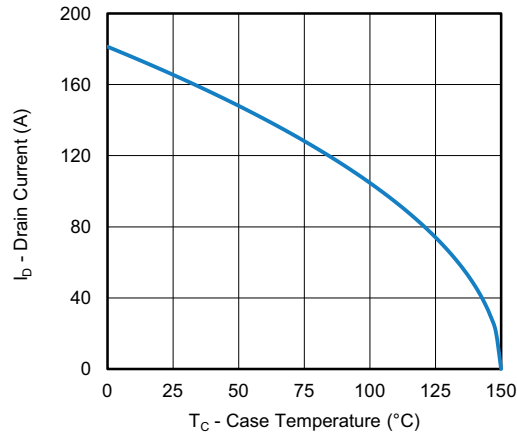
Safe Operating Area, Junction-to-Ambient

Note

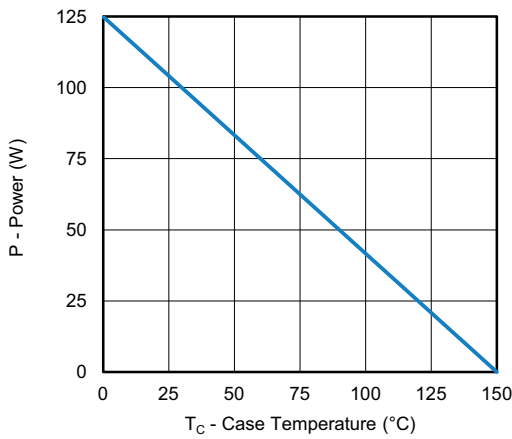
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



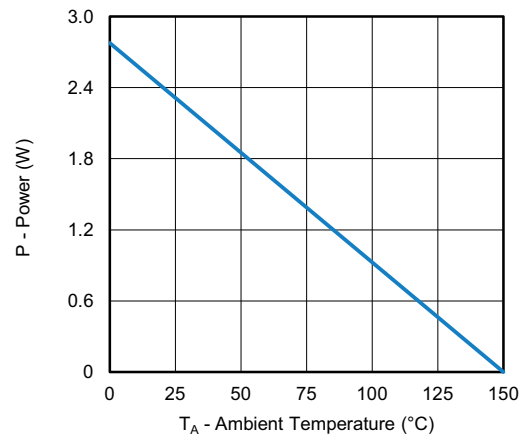
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



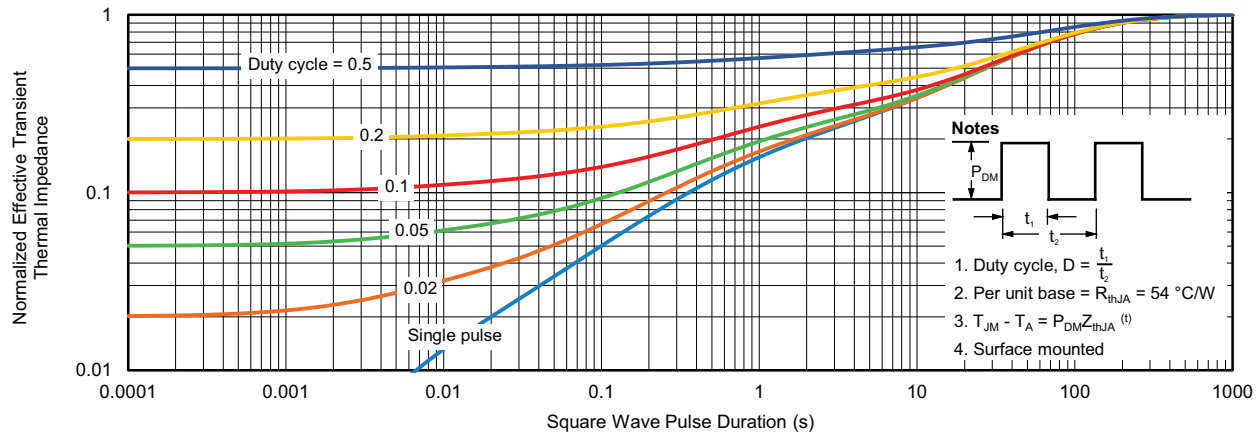
Power, Junction-to-Ambient

Note

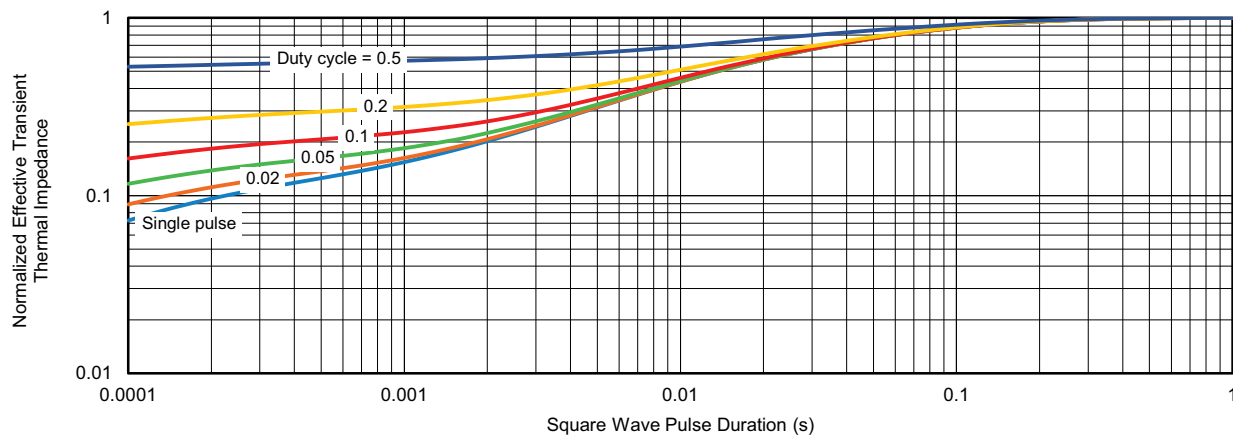
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150 \text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK[®] SO-8, (Single/Dual)



- Notes**
1. Inch will govern.
 2. Dimensions exclusive of mold gate burrs.
 3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S17-0173-Rev. L, 13-Feb-17
DWG: 5881

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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