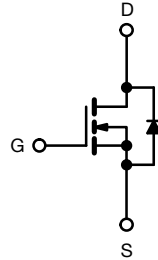
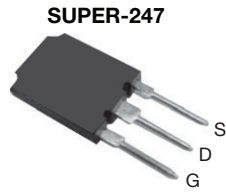


E Series Power MOSFET



N-Channel MOSFET


RoHS
COMPLIANT

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ (Ω) typ. at 25 °C	$V_{GS} = 10$ V	0.025
Q_g (nC) max.	591	
Q_{gs} (nC)	84	
Q_{gd} (nC)	160	
Configuration	Single	

ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free	SiHS90N65E-GE3


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	87	A
		$T_C = 100$ °C	55	
Pulsed drain current ^a	I_{DM}	323		
Linear derating factor		5	W/°C	
Single pulse avalanche energy ^b	E_{AS}	1930	mJ	
Maximum power dissipation	P_D	625	W	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Drain-source voltage slope	dV/dt	$T_J = 125$ °C	41	V/ns
Reverse diode dV/dt ^d		4.1		
Soldering recommendations (peak temperature) ^c	for 10 s	300	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 11.7$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.2	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		650	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.83	-	V/°C
Gate threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	± 1	μA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	25	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 45\text{ A}$	-	0.025	0.029	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 30\text{ V}, I_D = 45\text{ A}$		-	32	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 300\text{ kHz}$		-	11 826	-	pF
Output capacitance	C_{oss}			-	528	-	
Reverse transfer capacitance	C_{rss}			-	9	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 520\text{ V}$		-	384	-	pF
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	1502	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 45\text{ A}, V_{DS} = 520\text{ V}$	-	394	591	nC
Gate-source charge	Q_{gs}			-	84	-	
Gate-drain charge	Q_{gd}			-	160	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 45\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	85	128	ns
Rise time	t_r			-	152	228	
Turn-off delay time	$t_{d(off)}$			-	323	485	
Fall time	t_f			-	267	401	
Gate input resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$		0.6	1.2	2.4	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	87	A
Pulsed diode forward current	I_{SM}			-	-	323	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 45\text{ A}, V_{GS} = 0\text{ V}$		-	0.9	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 45\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	971	1942	ns
Reverse recovery charge	Q_{rr}			-	26	52	μC
Reverse recovery current	I_{RRM}			-	42	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

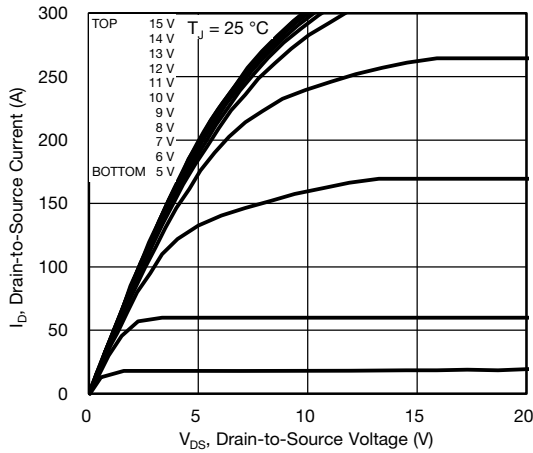


Fig. 1 - Typical Output Characteristics

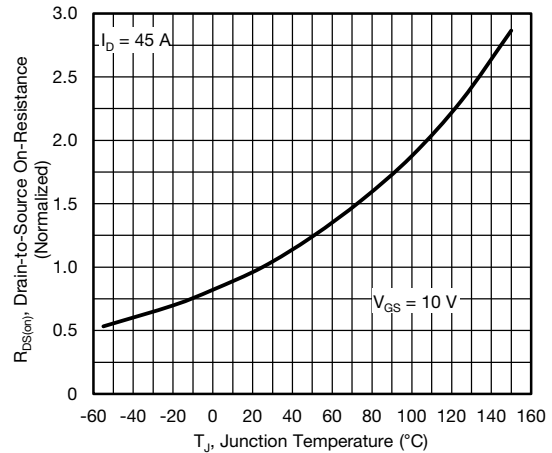


Fig. 4 - Normalized On-Resistance vs. Temperature

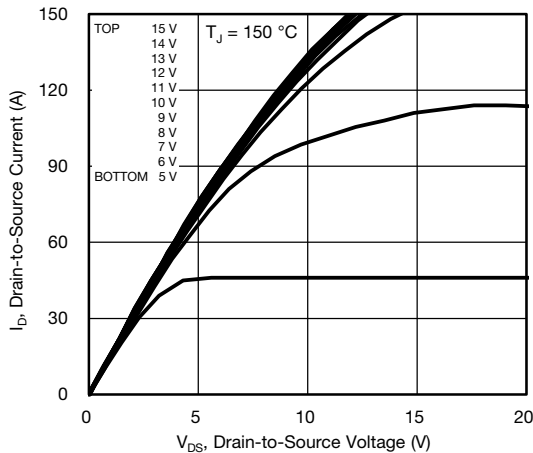


Fig. 2 - Typical Output Characteristics

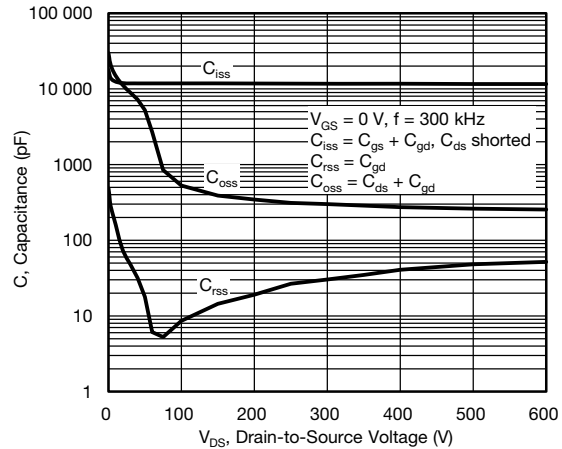


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

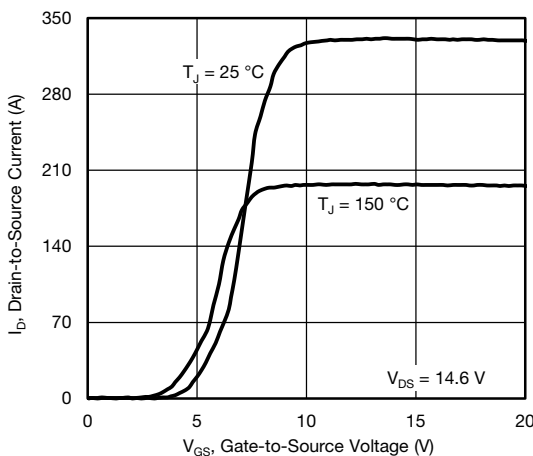


Fig. 3 - Typical Transfer Characteristics

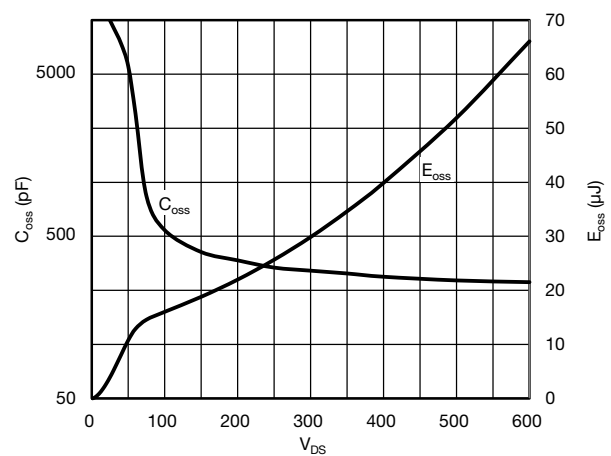


Fig. 6 - Coss and Eoss vs. Vds

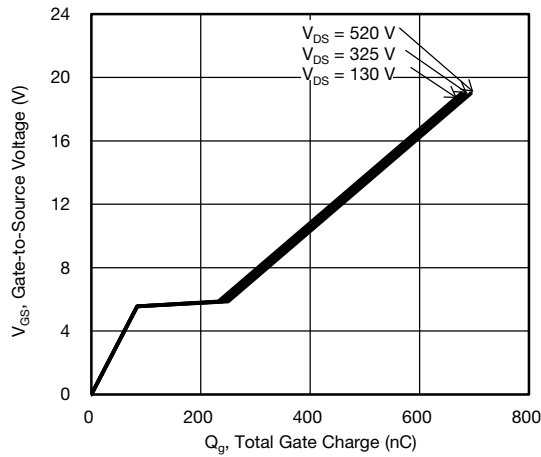


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

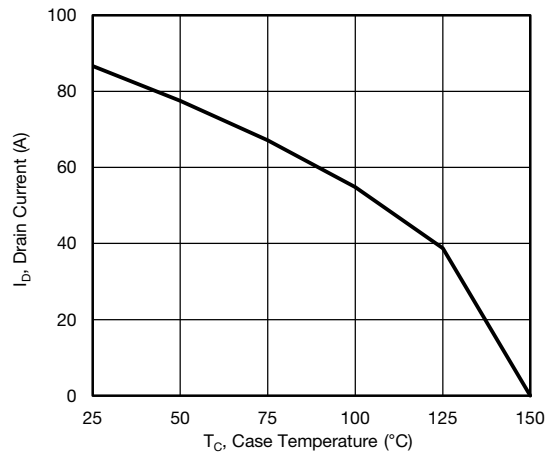


Fig. 10 - Maximum Drain Current vs. Case Temperature

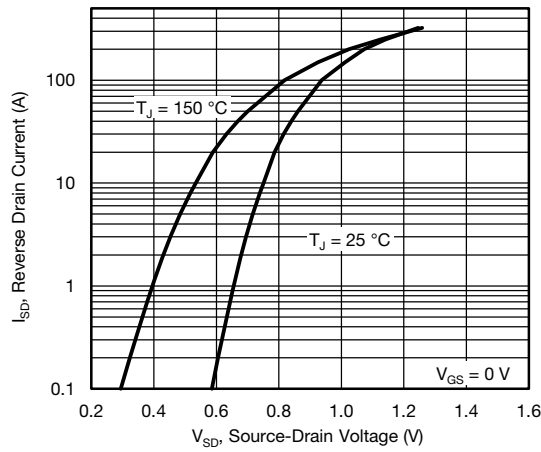


Fig. 8 - Typical Source-Drain Diode Forward Voltage

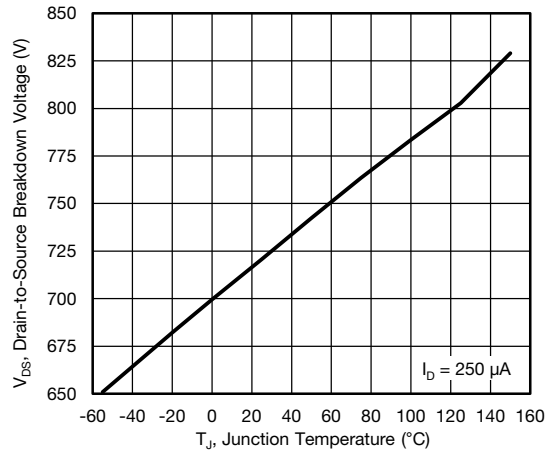


Fig. 11 - Temperature vs. Drain-to-Source Voltage

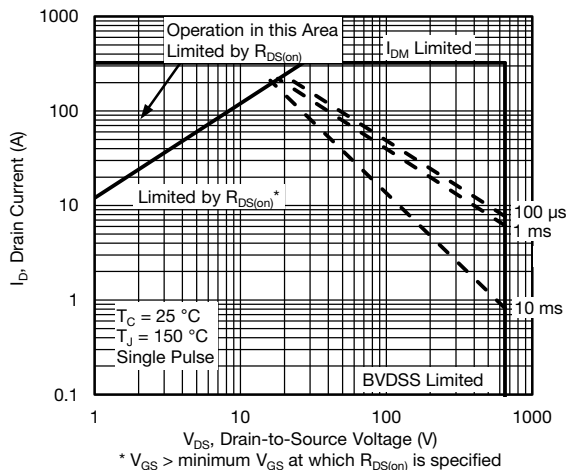


Fig. 9 - Maximum Safe Operating Area

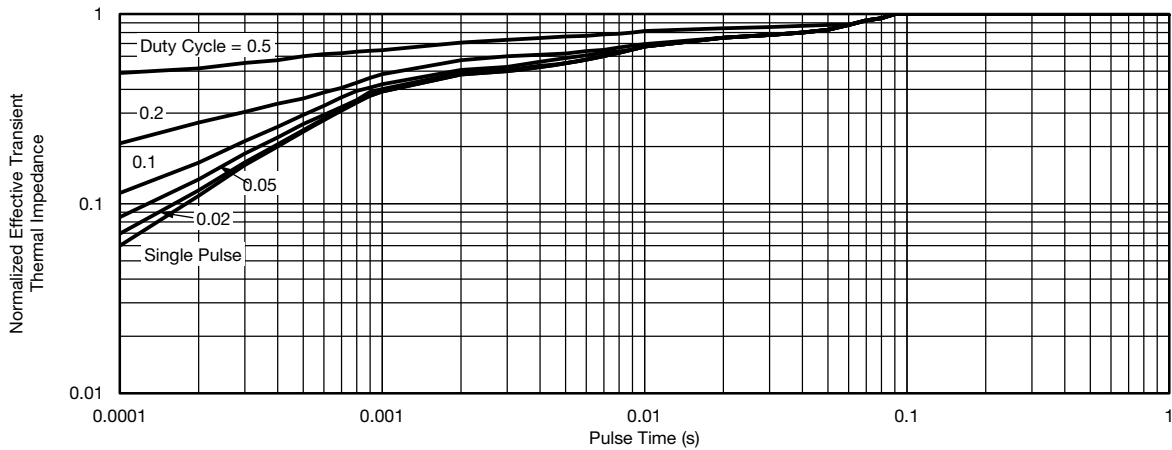


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

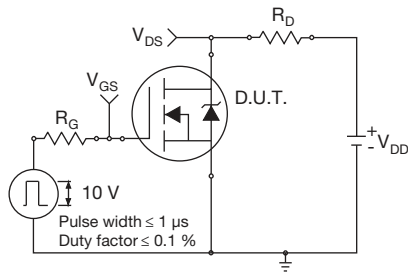


Fig. 13 - Switching Time Test Circuit

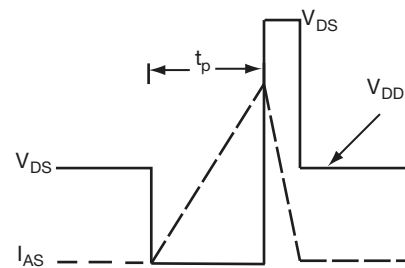


Fig. 16 - Unclamped Inductive Waveforms

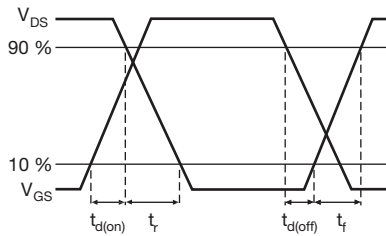


Fig. 14 - Switching Time Waveforms

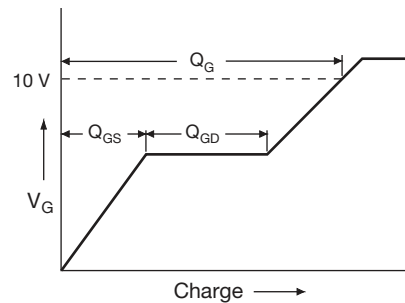


Fig. 17 - Basic Gate Charge Waveform

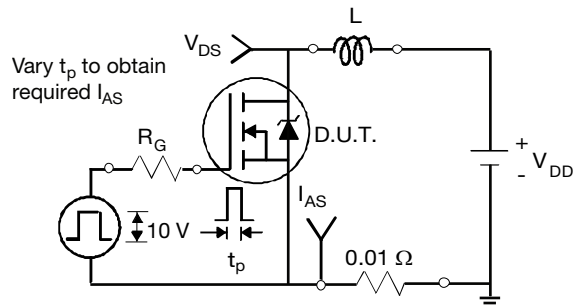


Fig. 15 - Unclamped Inductive Test Circuit

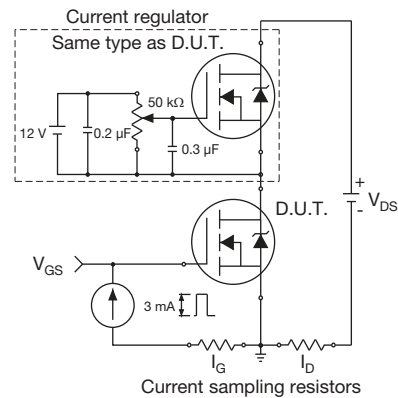
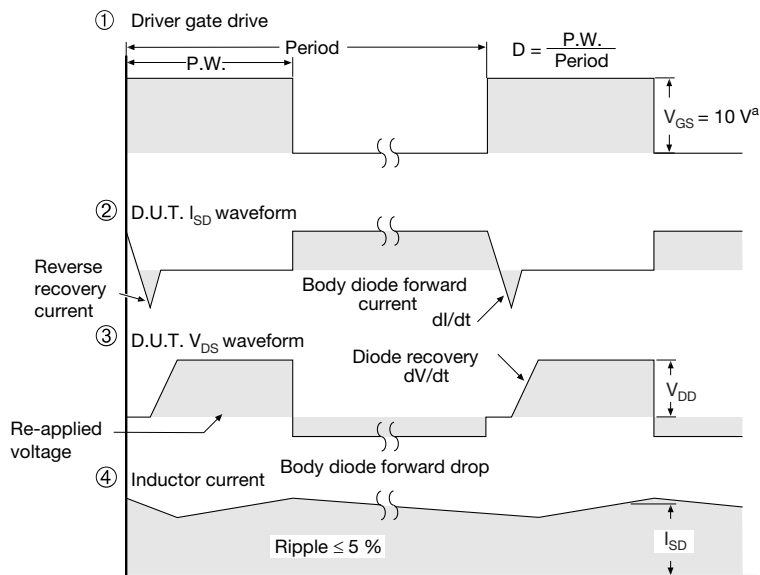
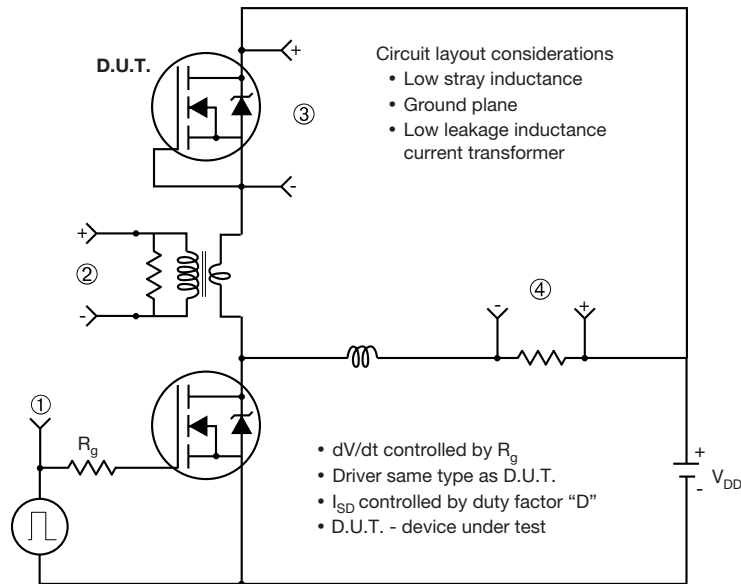


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

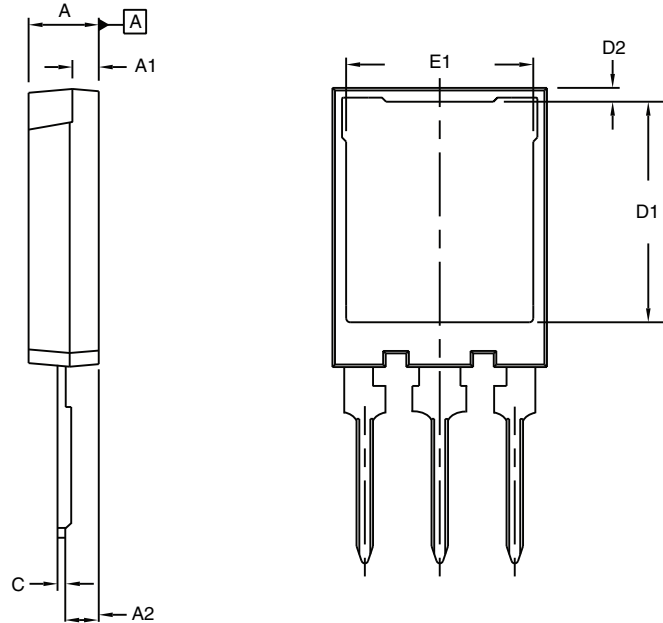
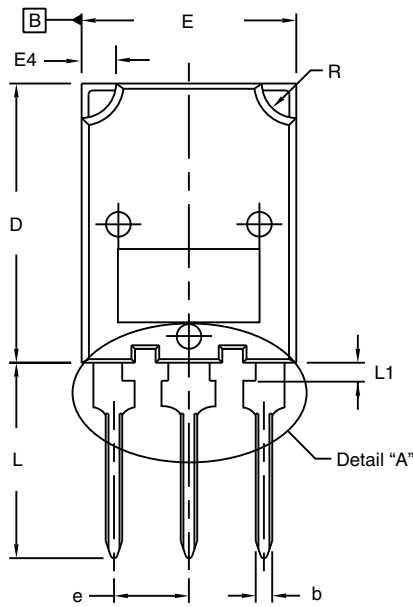
Fig. 19 - For N-Channel

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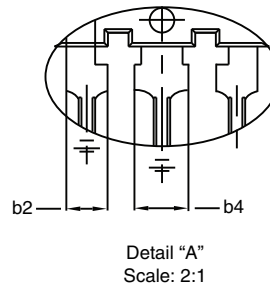
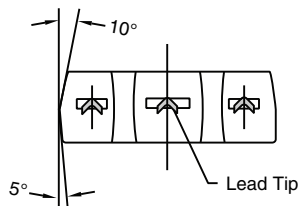


TO-274AA (High Voltage)

VERSION 1: FACILITY CODE = Y



⊕ 0.10 (0.25) ⊖ B A ⊕



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c ⁽¹⁾	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

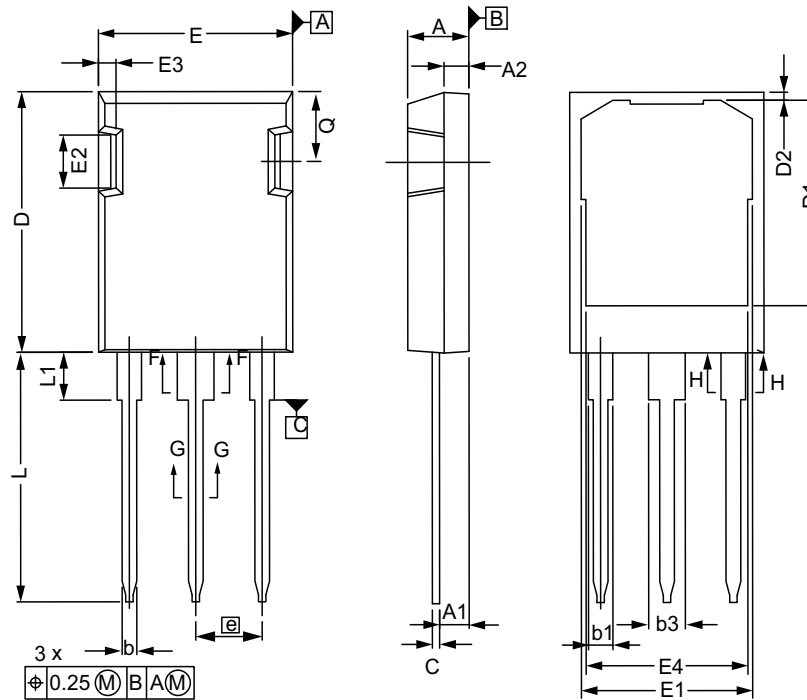
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

Notes

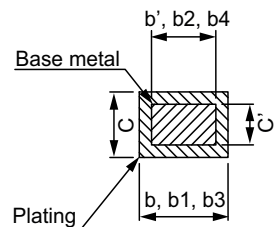
- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
- (1) Dimension measured at tip of lead



VERSION 2: FACILITY CODE = N



3 x $\phi 0.25$ (M) B A (M)



SECTION "F-F", "G-G" AND "H-H"
SCALE: NONE

MILLIMETERS		
DIM.	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	1.91	2.41
b2	1.91	2.16
b3	2.87	3.38
b4	2.87	3.13
c'	0.55	0.65
c	0.55	0.68
D	20.80	21.10

MILLIMETERS		
DIM.	MIN.	MAX.
D1	16.25	17.65
D2	0.50	0.80
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	5.44 BSC	
N	3	
L	19.81	20.32
L1	3.70	4.00
Q	5.49	6.00

ECN: E20-0538-Rev. C, 19-Oct-2020
DWG: 5975

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut



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