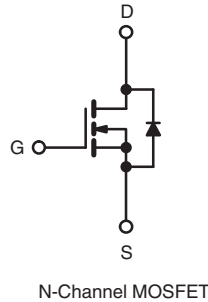
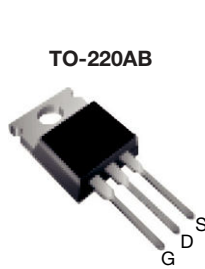


## D Series Power MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

PRODUCT SUMMARY		
$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.340
$Q_g$ (Max.) (nC)	90	
$Q_{gs}$ (nC)	14	
$Q_{gd}$ (nC)	22	
Configuration	Single	



### FEATURES

- Optimal Design
  - Low Area Specific On-Resistance
  - Low Input Capacitance ( $C_{iss}$ )
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-of-Merit (FOM):  $R_{on} \times Q_g$
  - Fast Switching
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### APPLICATIONS

- Consumer Electronics
  - Displays (LCD or Plasma TV)
- Lighting
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
  - Battery Chargers
- SMPS

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	SiHP17N60D-E3
Lead (Pb)-free and Halogen-free	SiHP17N60D-GE3


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		600	V
Gate-Source Voltage	$V_{GS}$		$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	17	A
		$T_C = 100$ °C	10.7	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		48	
Linear Derating Factor			2.22	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		165.6	mJ
Maximum Power Dissipation	$P_D$		277.8	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	°C
Drain-Source Voltage Slope	$T_J = 125$ °C		24	V/ns
Reverse Diode $dV/dt^d$			0.2	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s		300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 2.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 12$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ , starting  $T_J = 25$  °C.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.45	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.7	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	-	5	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	-	0.275	0.340	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 8\text{ A}$	-	6.2	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$	-	1780	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$		-	140	-	
Reverse Transfer Capacitance	$C_{rss}$		-	15	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}, V_{DS} = 480\text{ V}$	-	45	90	nC
Gate-Source Charge	$Q_{gs}$		-	14	-	
Gate-Drain Charge	$Q_{gd}$		-	22	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 8\text{ A}$ $R_g = 9.1\text{ }\Omega, V_{GS} = 10\text{ V}$	-	22	45	ns
Rise Time	$t_r$		-	56	85	
Turn-Off Delay Time	$t_{d(off)}$		-	37	75	
Fall Time	$t_f$		-	30	60	
Internal Gate Resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$	-	1.6	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	17	A
Pulsed Diode Forward Current	$I_{SM}$		-	-	48	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 8\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S,$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}$	-	633	950	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	7	15	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$		-	21	42	A

**Note**

a. Repetitive rating; pulse width limited by maximum junction temperature.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

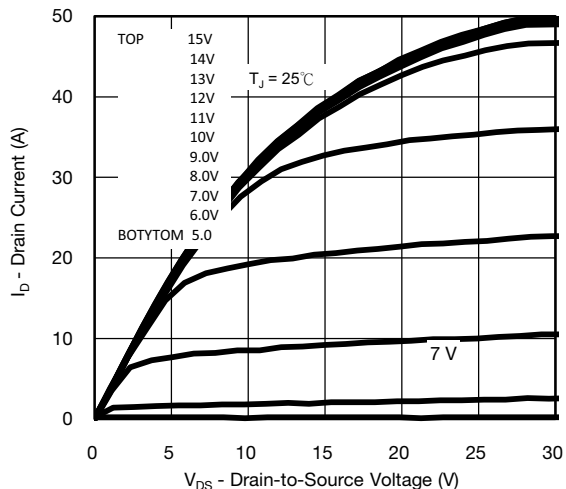


Fig. 1 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

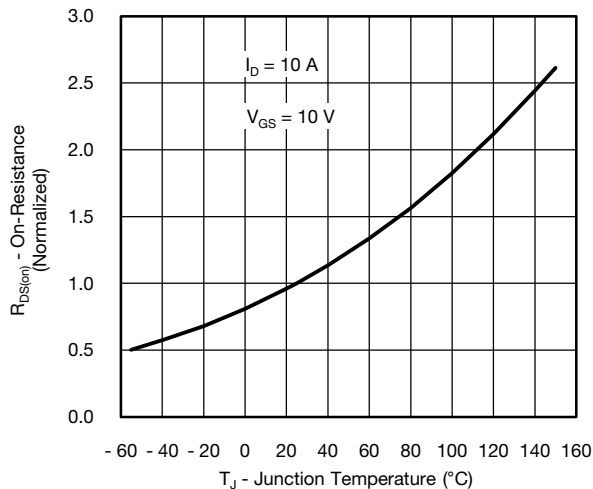


Fig. 4 - Normalized On-Resistance vs. Temperature

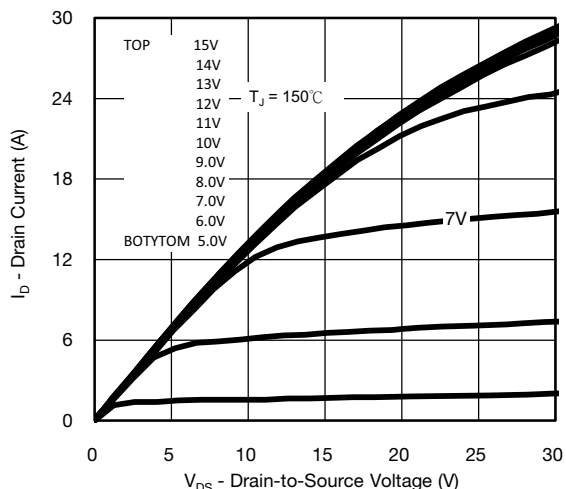


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

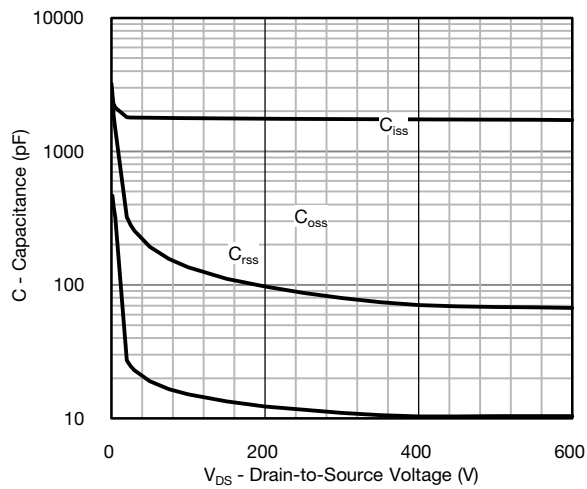


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

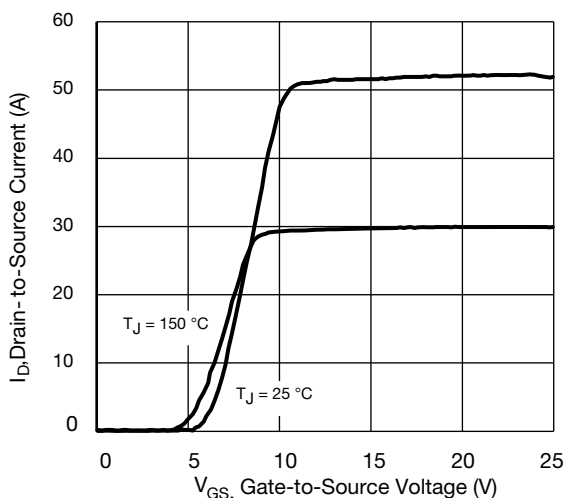


Fig. 3 - Typical Transfer Characteristics

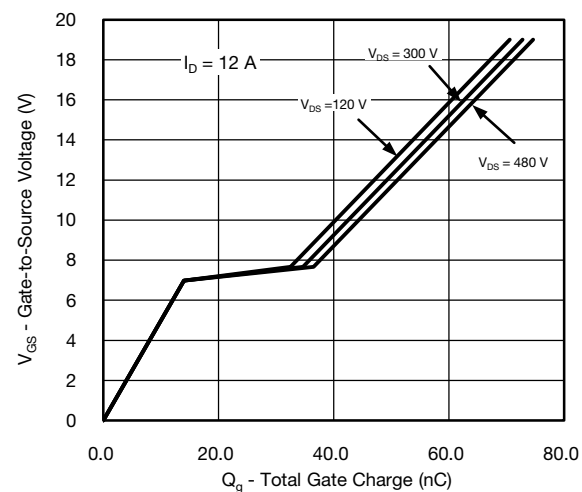


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

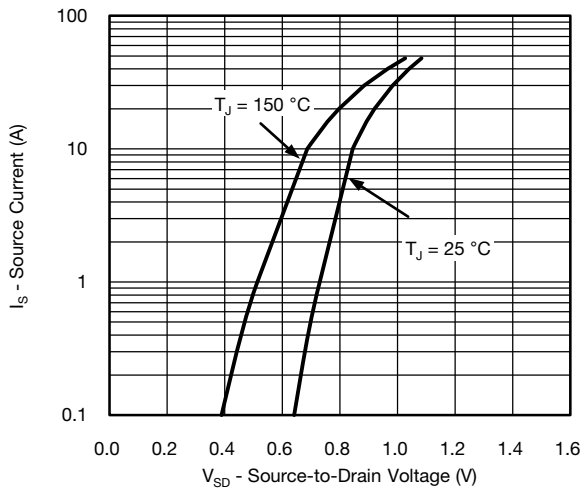


Fig. 7 - Typical Source-Drain Diode Forward Voltage

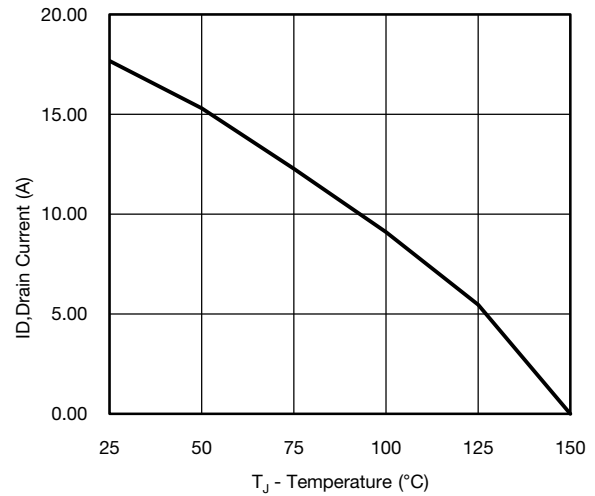


Fig. 9 - Maximum Drain Current vs. Case Temperature

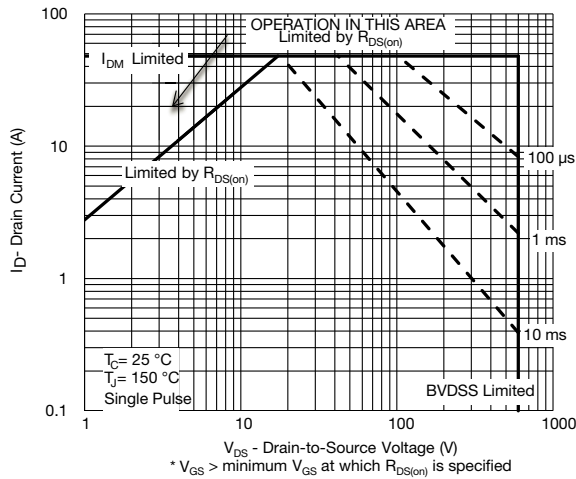


Fig. 8 - Maximum Safe Operating Area

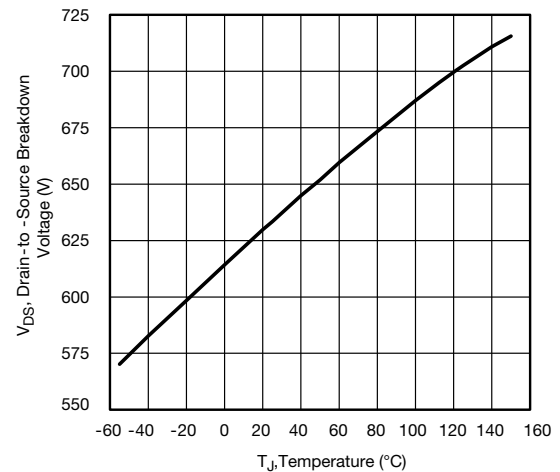


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

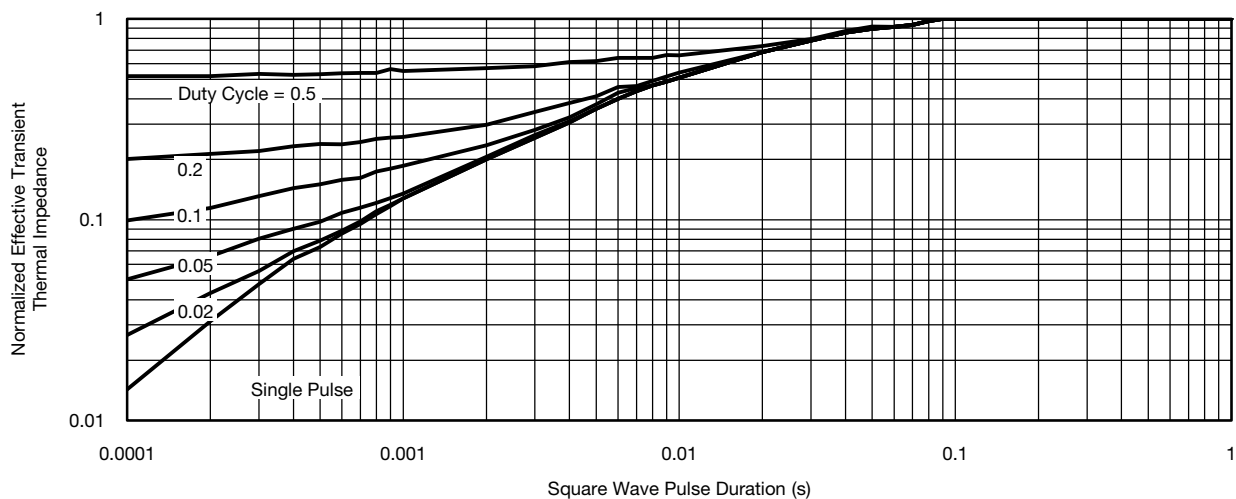
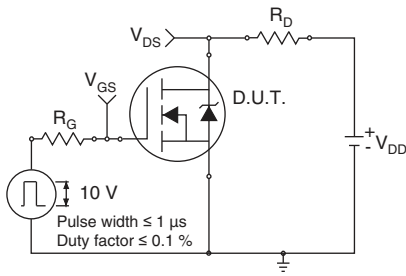
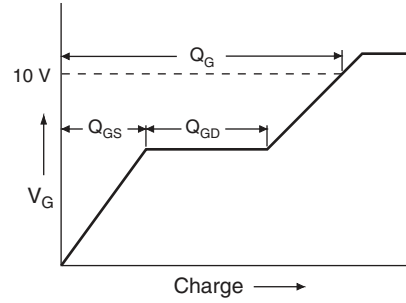


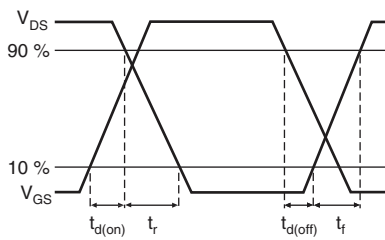
Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



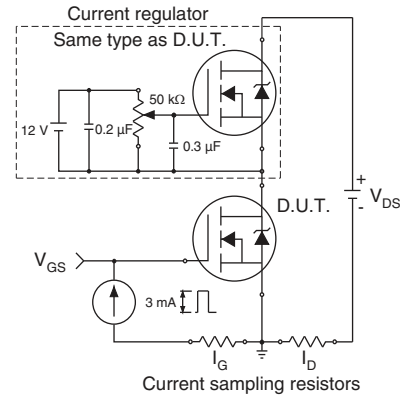
**Fig. 12 - Switching Time Test Circuit**



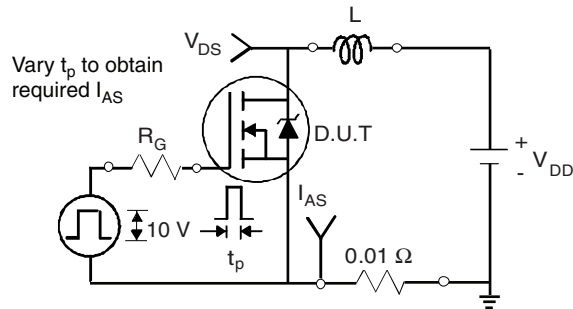
**Fig. 16 - Basic Gate Charge Waveform**



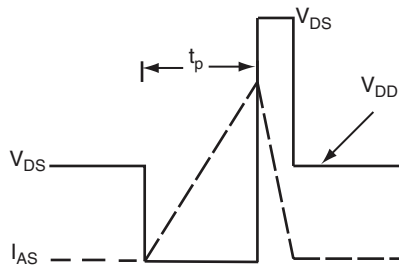
**Fig. 13 - Switching Time Waveforms**



**Fig. 17 - Gate Charge Test Circuit**

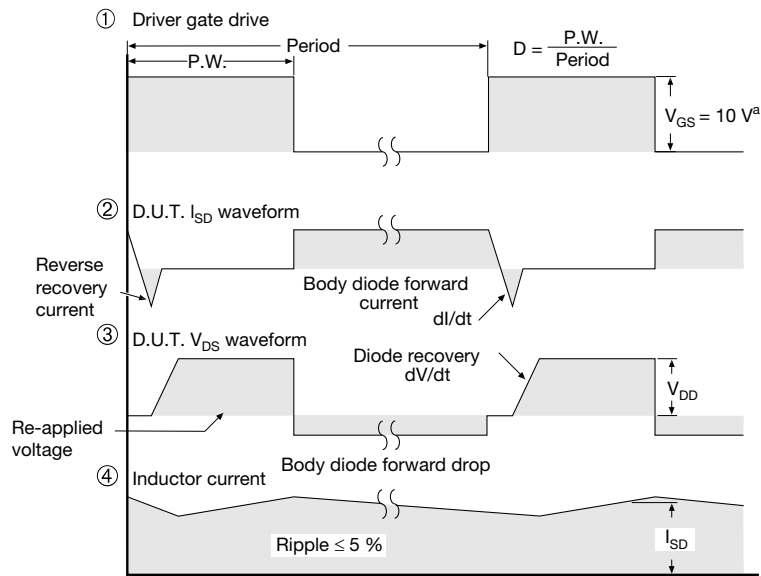
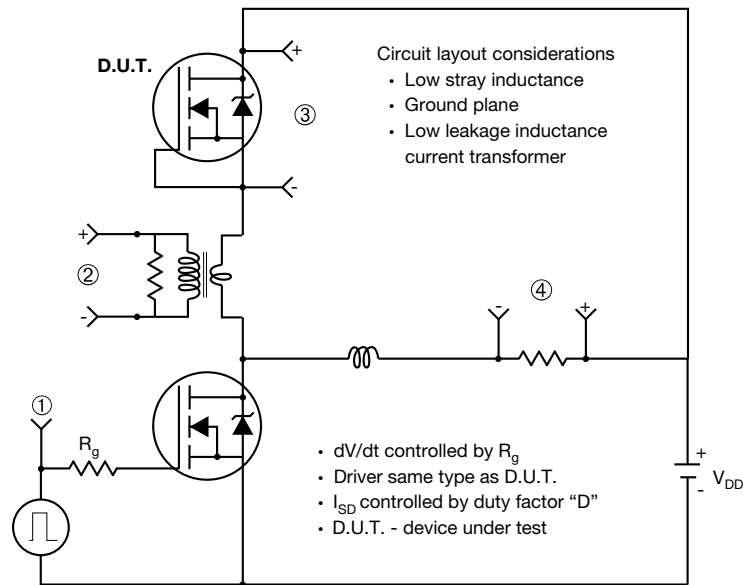


**Fig. 14 - Unclamped Inductive Test Circuit**



**Fig. 15 - Unclamped Inductive Waveforms**

### Peak Diode Recovery dV/dt Test Circuit



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 18 - For N-Channel**

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### TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021  
DWG: 6031

**Note**

- $M^*$  = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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