

E Series Power MOSFET



RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	700
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V 0.090
Q_g max. (nC)	173
Q_{gs} (nC)	29
Q_{gd} (nC)	49
Configuration	Single

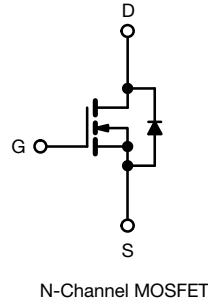
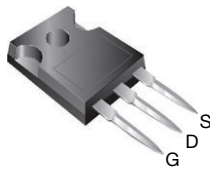
FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

TO-247AC



ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free and Halogen-free	SiHG33N65E-GE3


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	I_D	$T_C = 25$ °C	32.4
			$T_C = 100$ °C	21
Pulsed Drain Current ^a		I_{DM}	101	A
Linear Derating Factor			2.5	W/°C
Single Pulse Avalanche Energy ^b		E_{AS}	596	mJ
Maximum Power Dissipation		P_D	313	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	$T_J = 125$ °C	dV/dt	70	V/ns
Reverse Diode dV/dt ^d			16	
Soldering Recommendations (Peak temperature) ^c	for 10 s		300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 6.5$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.4	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.84	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 16.5\text{ A}$	-	0.090	0.105	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 30\text{ V}, I_D = 16.5\text{ A}$	-	11.5	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1.0\text{ MHz}$	-	4040	-	pF
Output Capacitance	C_{oss}		-	123	-	
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$	-	121	-	pF
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	501	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 16.5\text{ A}, V_{DS} = 520\text{ V}$	-	115	173	nC
Gate-Source Charge	Q_{gs}		-	29	-	
Gate-Drain Charge	Q_{gd}		-	49	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 16.5\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$	-	35	70	ns
Rise Time	t_r		-	67	100	
Turn-Off Delay Time	$t_{d(off)}$		-	103	155	
Fall Time	t_f		-	60	90	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$	0.25	0.50	1.0	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	32.4	A
Pulsed Diode Forward Current	I_{SM}		-	-	101	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 16.5\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 16.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$	-	605	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	11	-	μC
Reverse Recovery Current	I_{RRM}		-	28	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

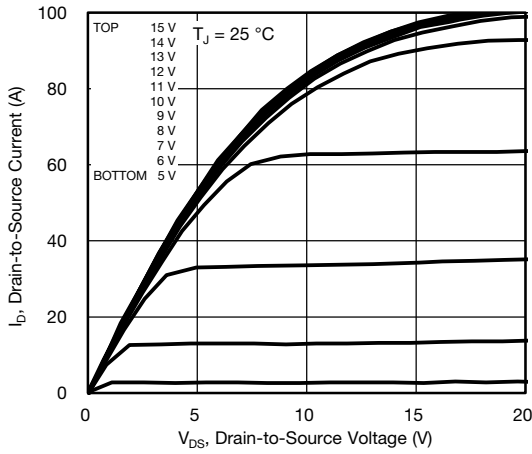


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

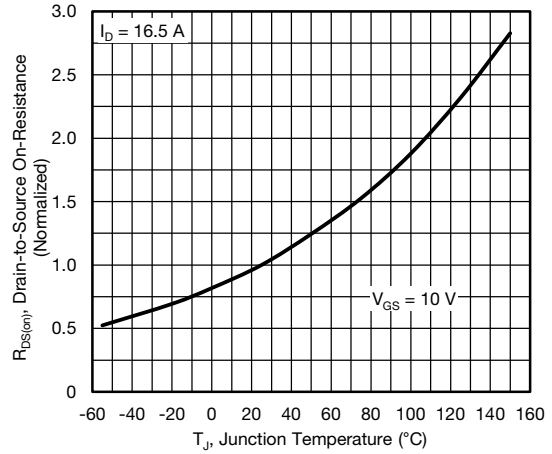


Fig. 4 - Normalized On-Resistance vs. Temperature

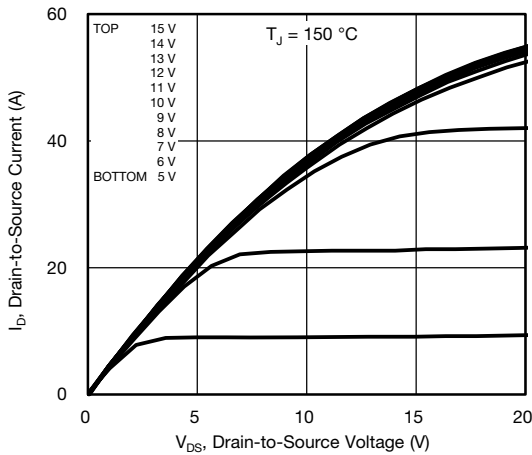


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

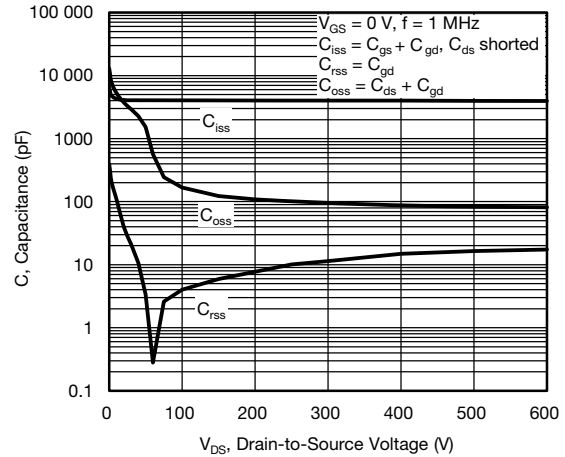


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

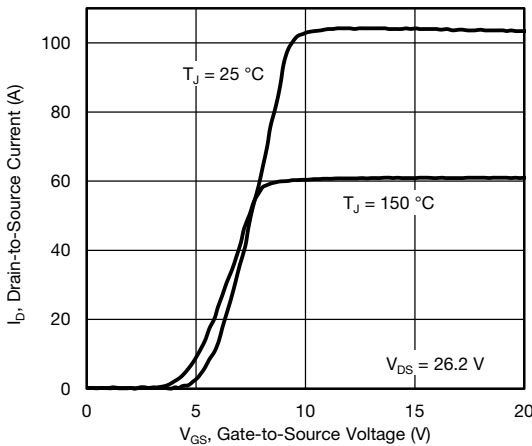


Fig. 3 - Typical Transfer Characteristics

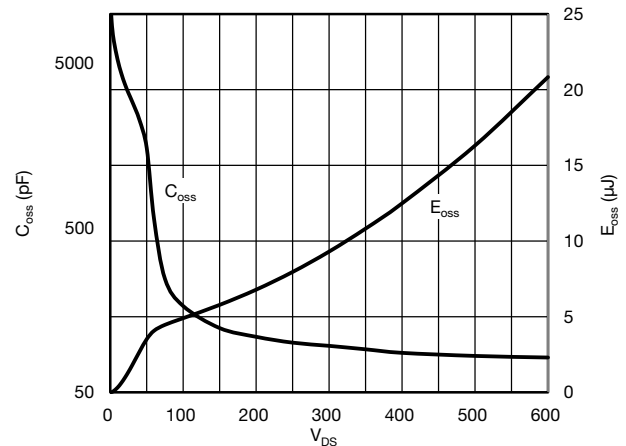


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

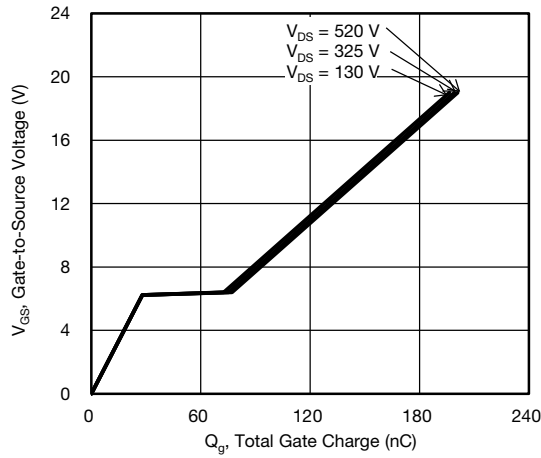


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

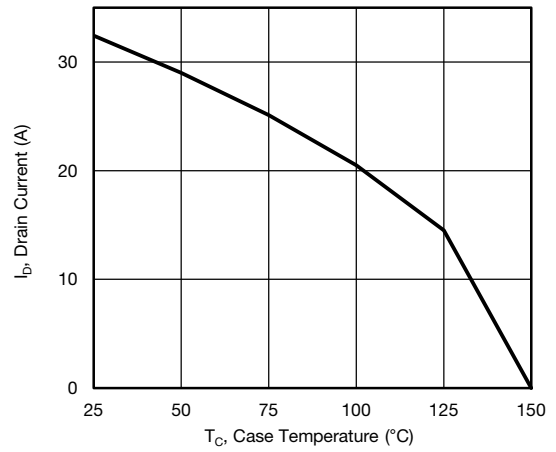


Fig. 10 - Maximum Drain Current vs. Case Temperature

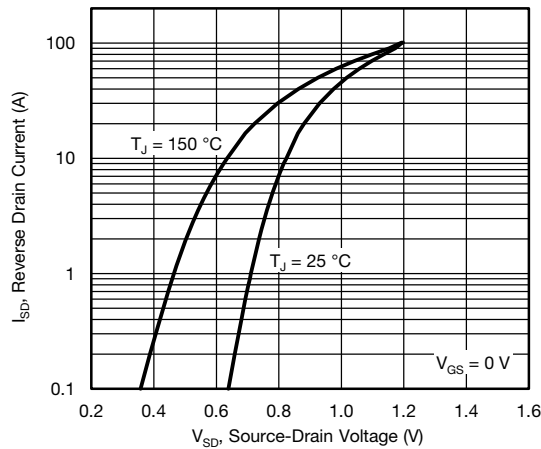


Fig. 8 - Typical Source-Drain Diode Forward Voltage

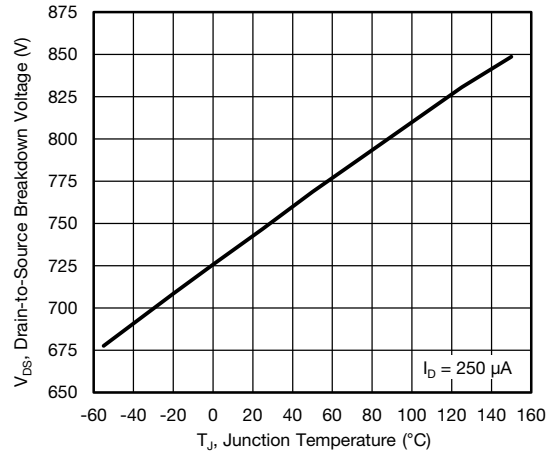


Fig. 11 - Temperature vs. Drain-to-Source Voltage

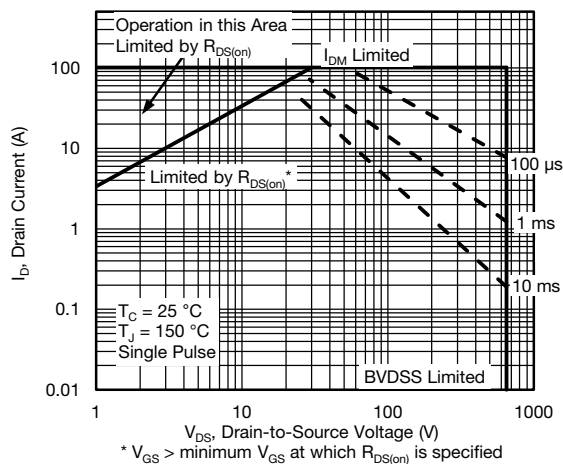


Fig. 9 - Maximum Safe Operating Area

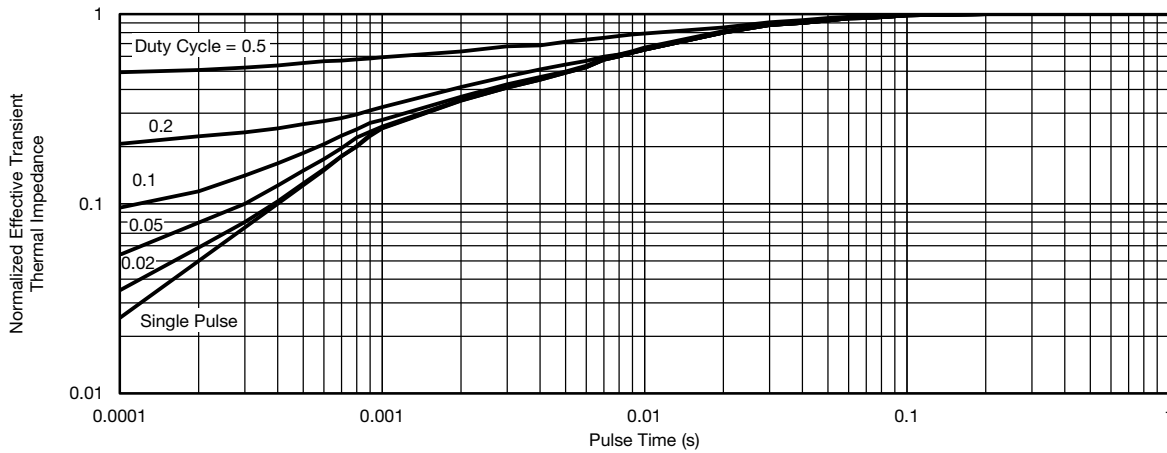


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

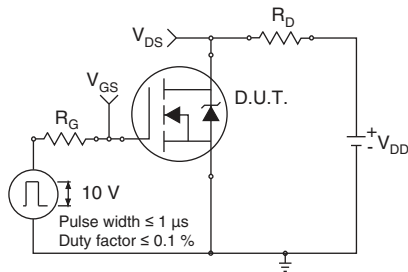


Fig. 13 - Switching Time Test Circuit

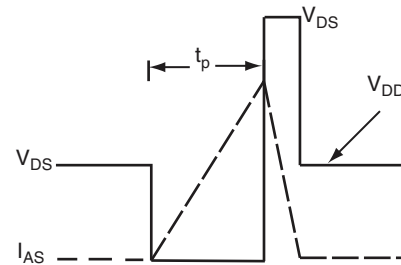


Fig. 16 - Unclamped Inductive Waveforms

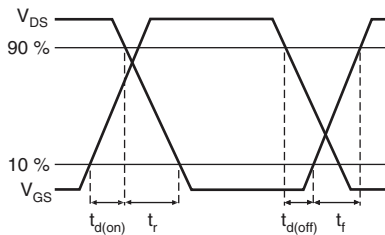


Fig. 14 - Switching Time Waveforms

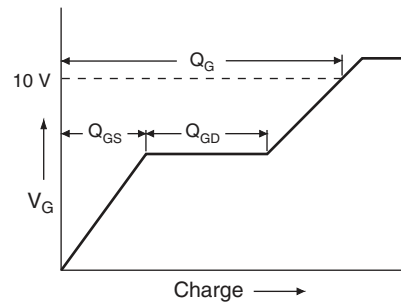


Fig. 17 - Basic Gate Charge Waveform

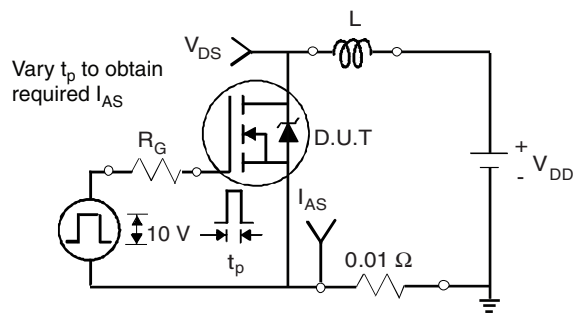


Fig. 15 - Unclamped Inductive Test Circuit

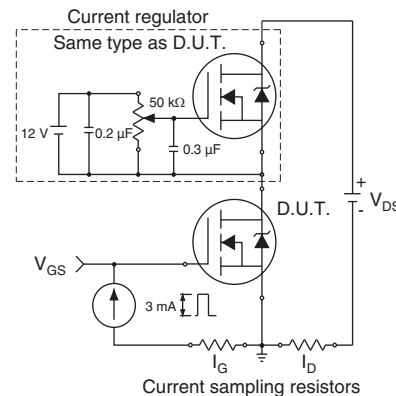


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91716.



VERSION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
 DWG: 5971

- Notes**
- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
 - (2) Contour of slot optional
 - (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
 - (4) Thermal pad contour optional with dimensions D1 and E1
 - (5) Lead finish uncontrolled in L1
 - (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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