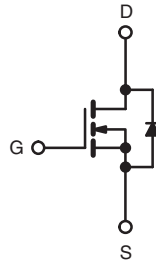
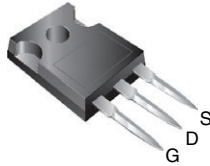


Power MOSFET

TO-247


N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Full bridge
- PFC boost

PRODUCT SUMMARY	
V_{DS} (V)	500
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.27
Q_g (max.) (nC)	105
Q_{gs} (nC)	26
Q_{gd} (nC)	42
Configuration	Single

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP460APbF


ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	500	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	20	A
		$T_C = 100\text{ }^\circ\text{C}$	13	
Pulsed drain current ^a	I_{DM}	80		
Linear derating factor		2.2	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b	E_{AS}	960	mJ	
Repetitive avalanche current ^a	I_{AR}	20	A	
Repetitive avalanche energy ^a	E_{AR}	28	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	280	W
Peak diode recovery dV/dt ^c	dV/dt		3.8	V/ns
Operating junction and storage temperature range	T_J, T_{stg}		-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature)	for 10 s		300 ^d	
Mounting torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 4.3\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 20\text{ A}$ (see fig. 12)
- $I_{SD} \leq 20\text{ A}$, $dI/dt \leq 125\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case



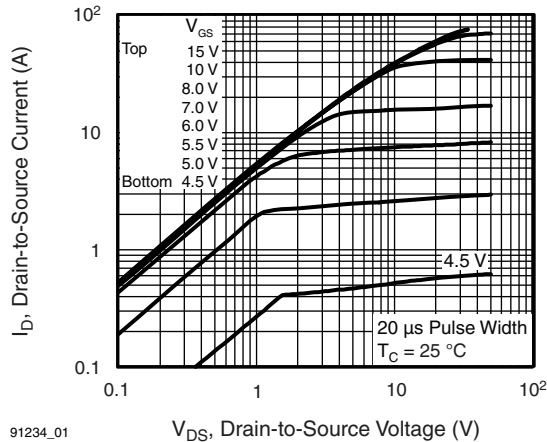
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.24	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.45	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.61	-	V/°C	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}^b$	-	-	0.27	Ω	
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 12\text{ A}^b$	11	-	-	S	
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	3100	-	pF	
Output capacitance	C_{oss}		-	480	-		
Reverse transfer capacitance	C_{rss}		-	18	-		
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	4430	pF	
			$V_{DS} = 400\text{ V}$, $f = 1.0\text{ MHz}$	-	130		
			$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	140		
Effective output capacitance	$C_{oss\text{ eff.}}$		-	-	-		
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	105	nC
Gate-source charge	Q_{gs}			-	-	26	
Gate-drain charge	Q_{gd}			-	-	42	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.3\text{ }\Omega$, $R_D = 13\text{ }\Omega$, see fig. 10 ^b	-	18	-	ns	
Rise time	t_r		-	55	-		
Turn-off delay time	$t_{d(off)}$		-	45	-		
Fall time	t_f		-	39	-		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p-n junction diode	-	-	20	A	
Pulsed diode forward current ^a	I_{SM}		-	-	80		
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 20\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.8	V	
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}^b$	-	480	710	ns	
Body diode reverse recovery charge	Q_{rr}		-	5.0	7.5	μC	
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

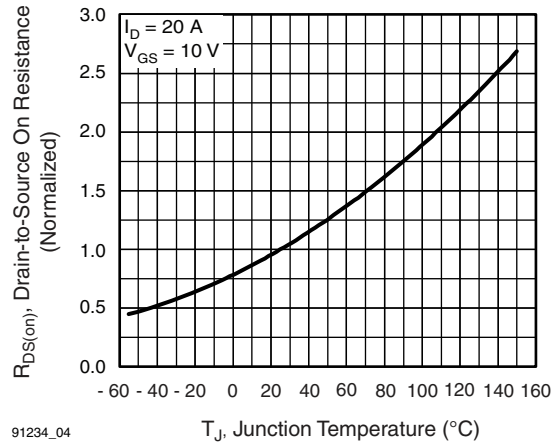
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0% to 80% V_{DS}

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



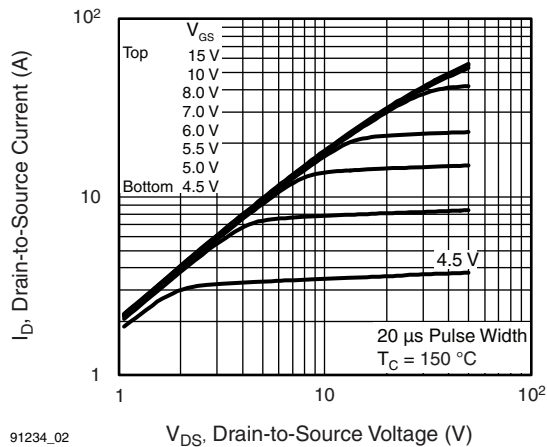
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Fig. 1 - Typical Output Characteristics



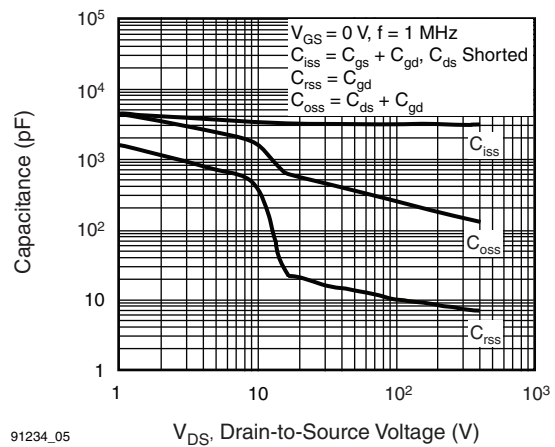
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Fig. 4 - Normalized On-Resistance vs. Temperature



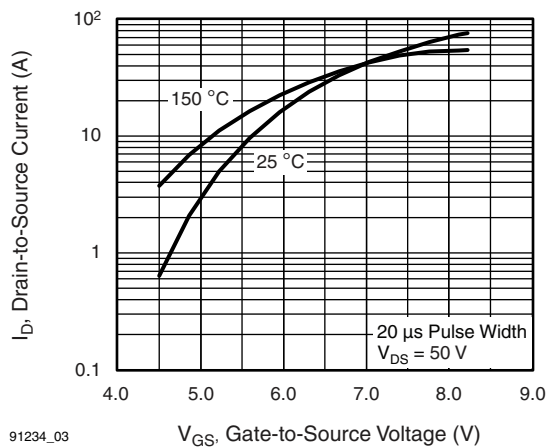
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Fig. 2 - Typical Output Characteristics



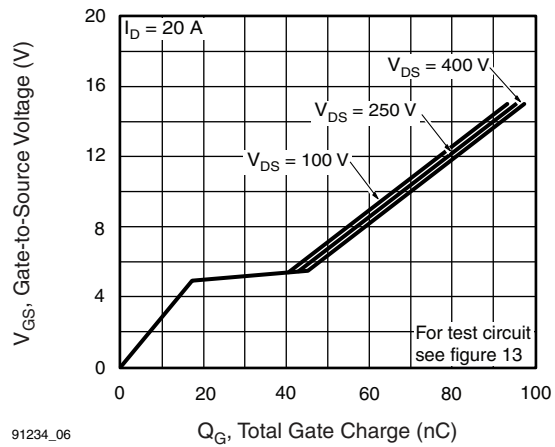
91234_05

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



91234_03

Fig. 3 - Typical Transfer Characteristics



91234_06

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

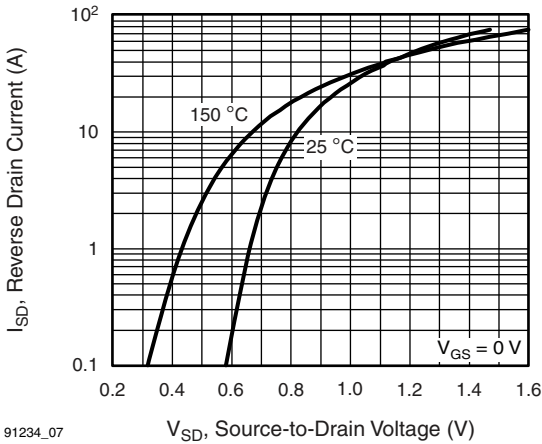


Fig. 7 - Typical Source-Drain Diode Forward Voltage

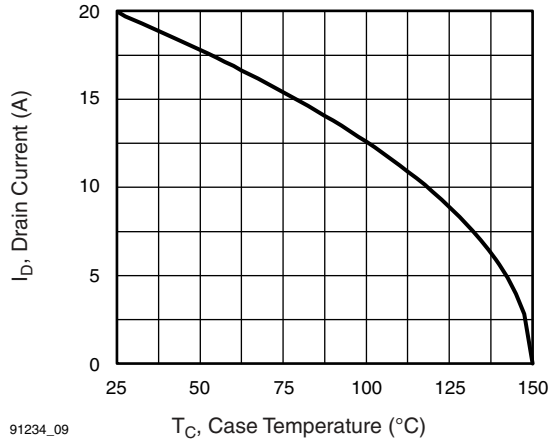


Fig. 9 - Maximum Drain Current vs. Case Temperature

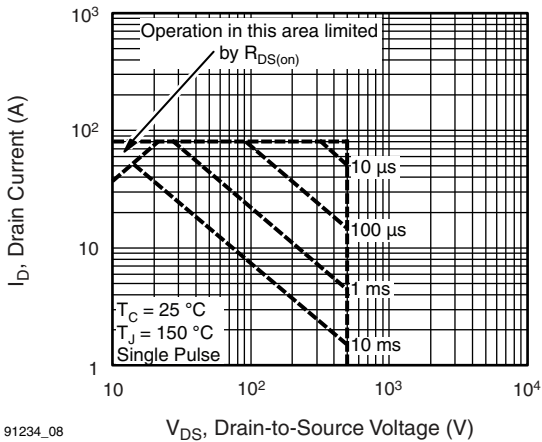


Fig. 8 - Maximum Safe Operating Area

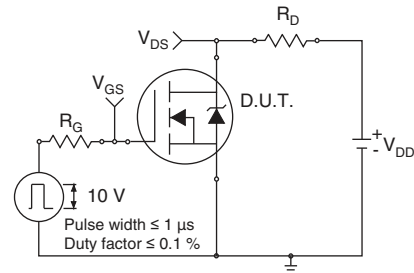


Fig. 10 - Switching Time Test Circuit

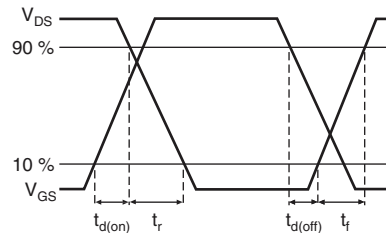


Fig. 11 - Switching Time Waveforms

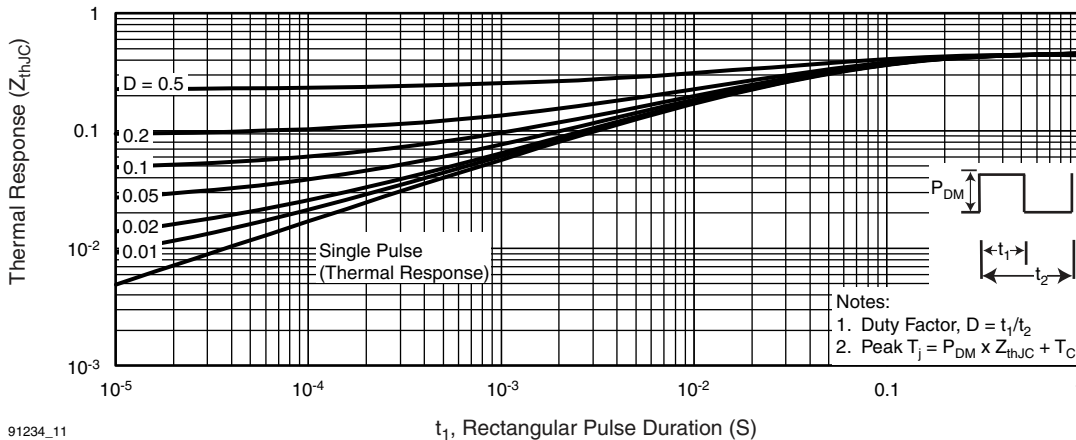


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

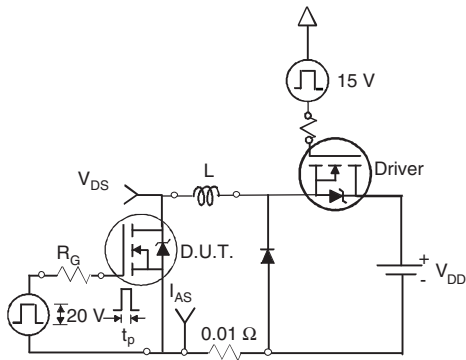


Fig. 13 - Unclamped Inductive Test Circuit

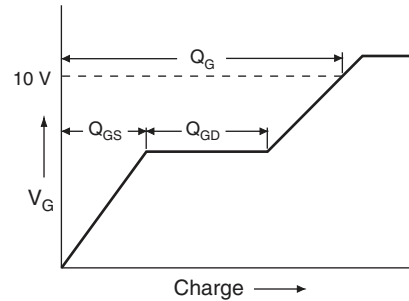


Fig. 16 - Basic Gate Charge Waveform

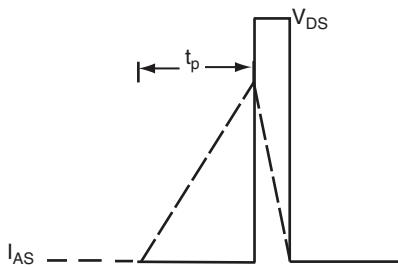


Fig. 14 - Unclamped Inductive Waveforms

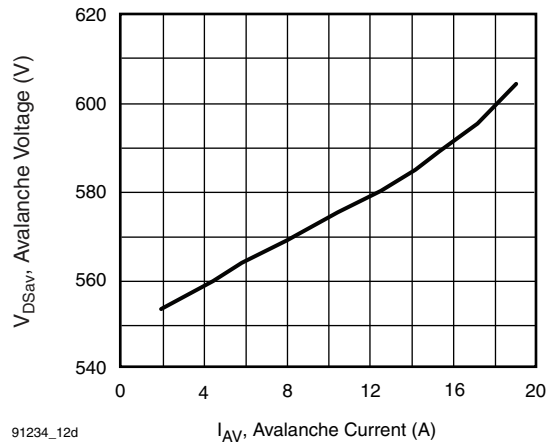


Fig. 17 - Typical Drain-to-Source Voltage vs. Avalanche Current

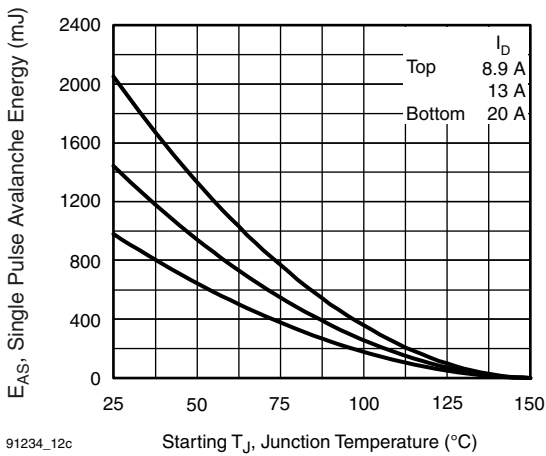


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

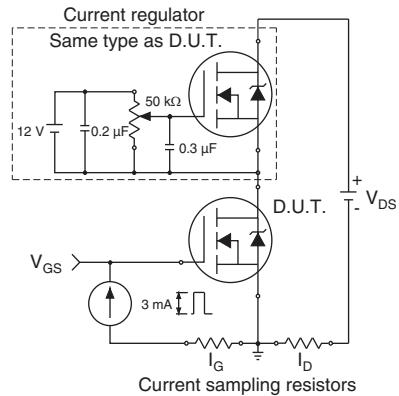
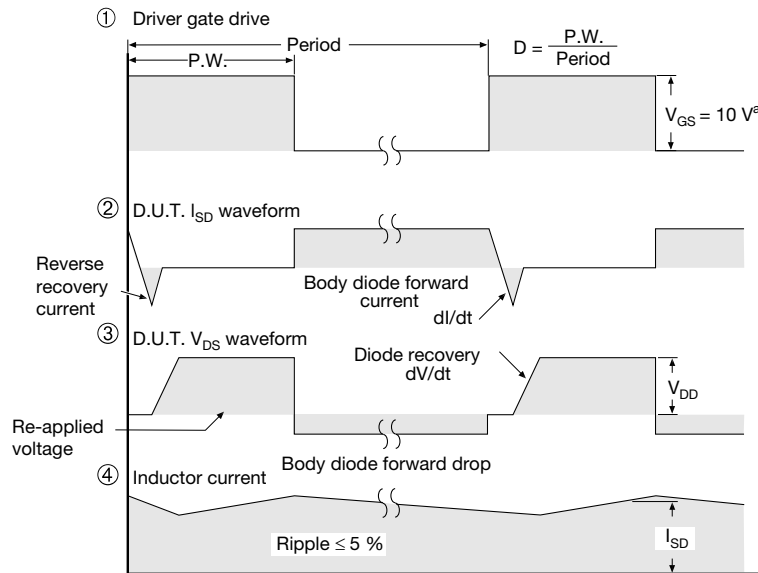
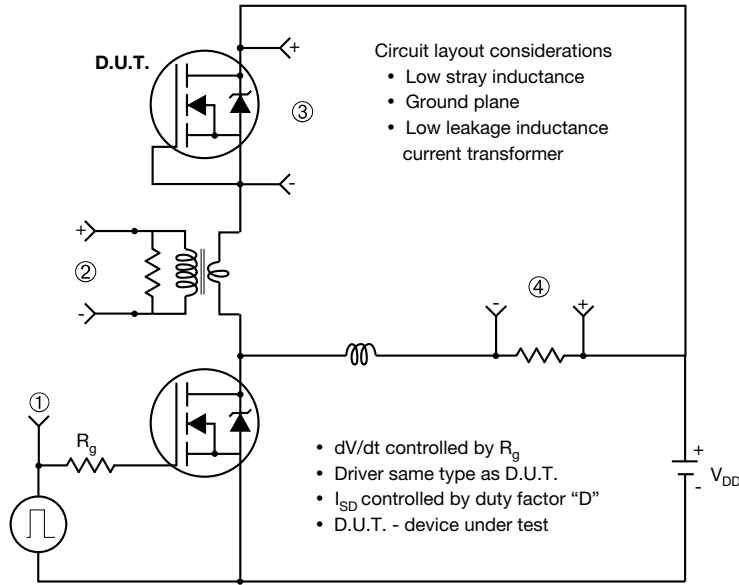


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

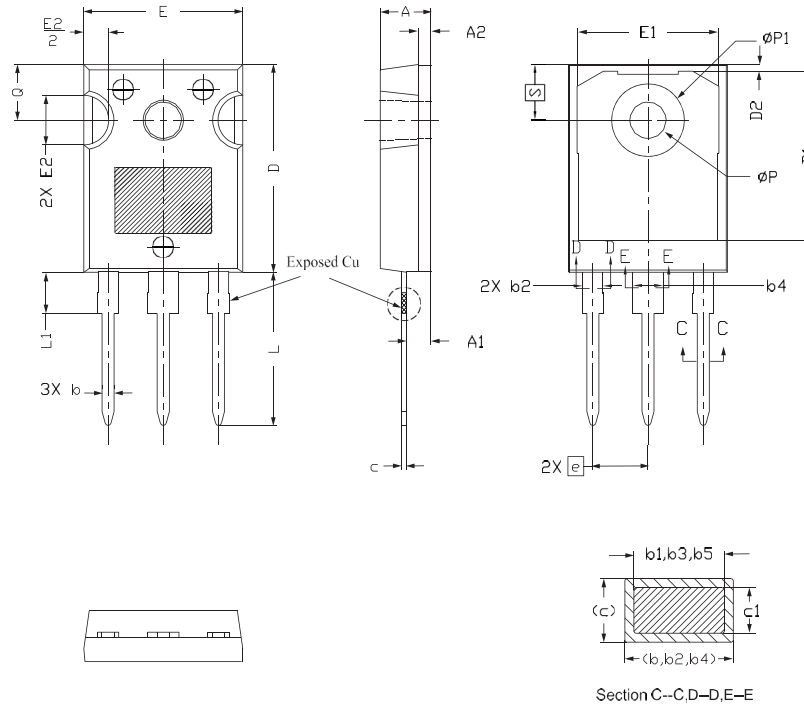
Fig. 19 - For N-Channel

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TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



DIM.	MILLIMETERS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

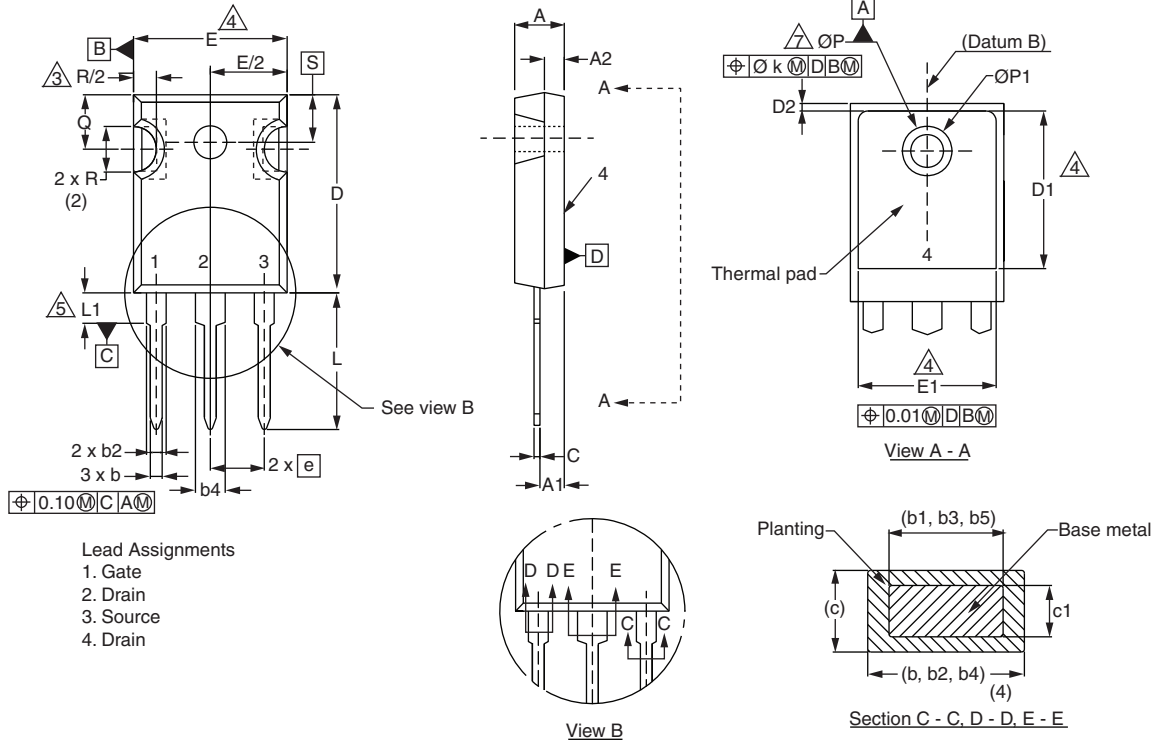
DIM.	MILLIMETERS			NOTES
	MIN.	NOM.	MAX.	
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



VERSION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

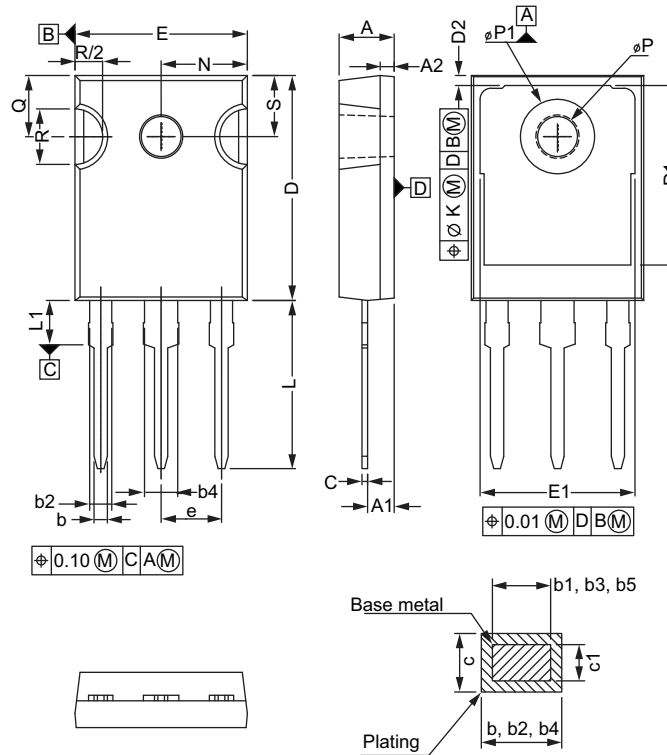
DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
 DWG: 5971

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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