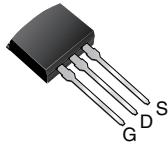
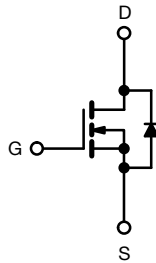
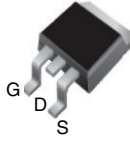


Power MOSFET

 I²PAK (TO-262)

 D²PAK (TO-2)


N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Two transistor forward
- Half bridge and full bridge

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ max. (Ω)	$V_{GS} = 10$ V	1.40
Q_g max. (nC)	24	
Q_{gs} (nC)	6.3	
Q_{gd} (nC)	11	
Configuration	Single	

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF830AS-GE3	SiHF830ASTRL-GE3 ^a	SiHF830AL-GE3 ^a
Lead (Pb)-free	IRF830ASPbF	IRF830ASTRLPbF ^a	IRF830ALPbF

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	500	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current	I_D	V_{GS} at 10 V	A	
		$T_C = 25$ °C		5.0
		$T_C = 100$ °C	3.2	
Pulsed Drain Current ^{a, e}	I_{DM}	20		
Linear Derating Factor		0.59	W/°C	
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	230	mJ	
Avalanche Current	I_{AR}	5.0	A	
Repetitive Avalanche Energy ^a	E_{AR}	7.4	mJ	
Maximum Power Dissipation	P_D	$T_A = 25$ °C	3.1	W
		$T_C = 25$ °C	74	
Peak Diode Recovery dV/dt , ^e	dV/dt	5.3	V/ns	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C	
Soldering Recommendations (Peak temperature) ^d	for 10 s	300		

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25$ °C, $L = 18$ mH, $R_g = 25$ Ω , $I_{AS} = 5.0$ A (see fig. 12)
- $I_{SD} \leq 5.0$ A, $dI/dt \leq 370$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
- 1.6 mm from case
- Uses SiHF830A data and test conditions



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

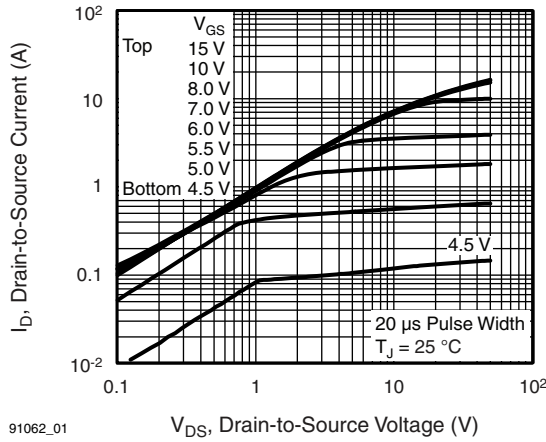
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d	-	0.60	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	-	4.5	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C	-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 3.0 A ^b	-	-	1.4	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 3.0 A ^d	2.8	-	-	S
Dynamic						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^d	-	620	-	pF
Output Capacitance	C _{oss}		-	93	-	
Reverse Transfer Capacitance	C _{rss}		-	4.3	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	886	-
			V _{DS} = 400 V, f = 1.0 MHz	-	27	-
Effective Output Capacitance	C _{oss eff.}	V _{DS} = 0 V to 400 V ^{c, d}	-	39	-	
Total Gate Charge	Q _g	V _{GS} = 10 V, I _D = 5.0 A, V _{DS} = 400 V, see fig. 6 and 13 ^{b, d}	-	-	24	nC
Gate-Source Charge	Q _{gs}		-	-	6.3	
Gate-Drain Charge	Q _{gd}		-	-	11	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 5.0 A, R _g = 14 Ω, R _D = 49 Ω, see fig. 10 ^{b, d}	-	10	-	ns
Rise Time	t _r		-	21	-	
Turn-Off Delay Time	t _{d(off)}		-	21	-	
Fall Time	t _f		-	15	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain	1.7	-	10.7	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.0	A
Pulsed Diode Forward Current ^a	I _{SM}		-	-	20	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 5.0 A, V _{GS} = 0 V ^b	-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 5.0 A, dI/dt = 100 A/μs ^{b, d}	-	430	650	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	2.0	3.0	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
- c. C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}
- d. Uses SiHF830A data and test conditions

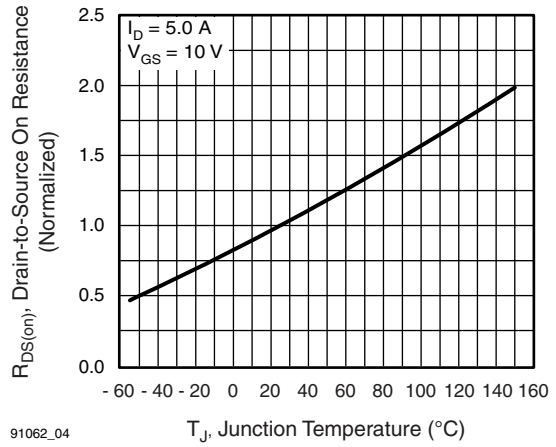


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



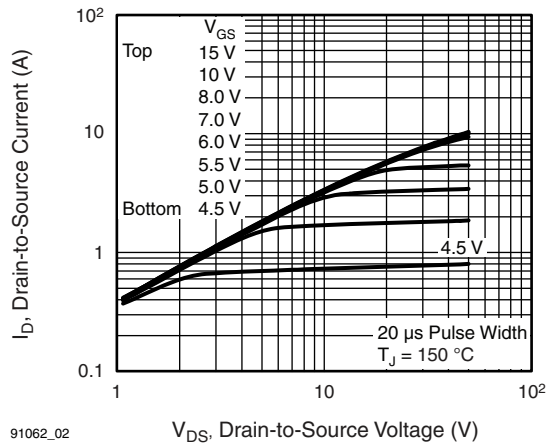
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Fig. 1 - Typical Output Characteristics



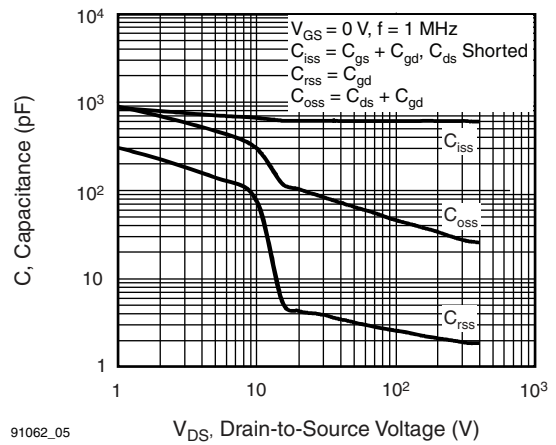
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Fig. 4 - Normalized On-Resistance vs. Temperature



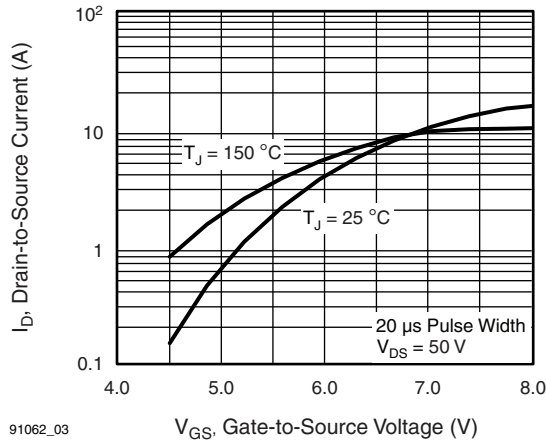
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Fig. 2 - Typical Output Characteristics



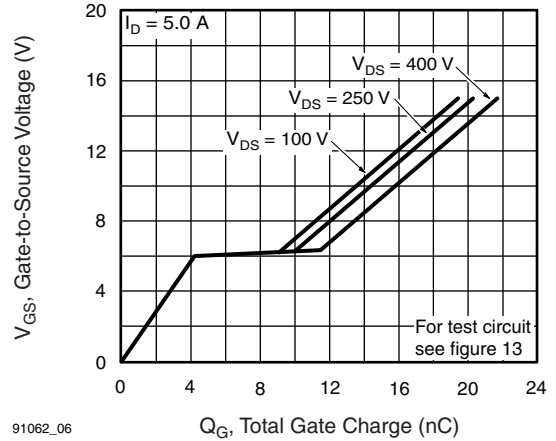
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



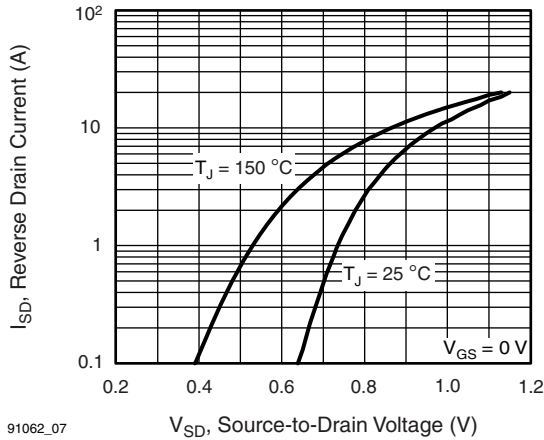
91062_03

Fig. 3 - Typical Transfer Characteristics



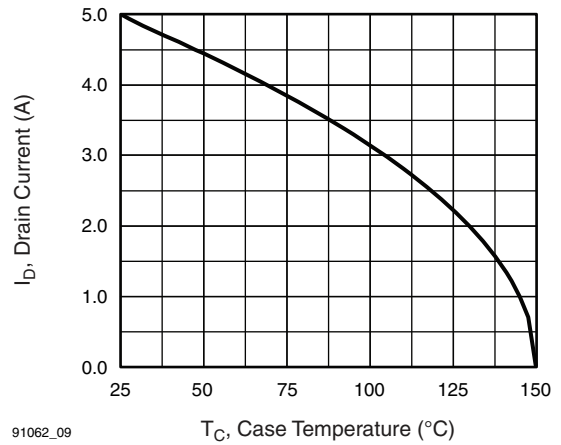
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



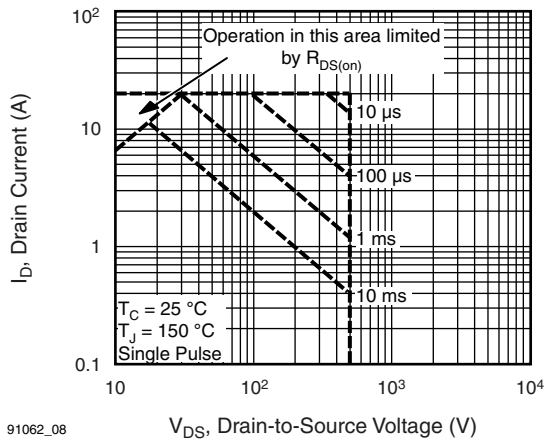
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



91062_09

Fig. 9 - Maximum Drain Current vs. Case Temperature



91062_08

Fig. 8 - Maximum Safe Operating Area

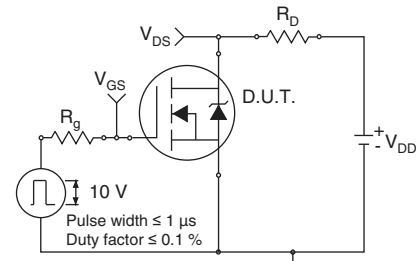


Fig. 10a - Switching Time Test Circuit

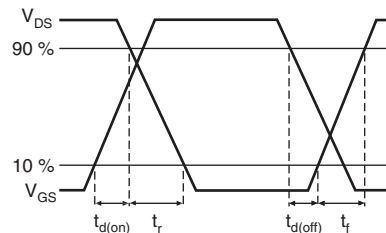
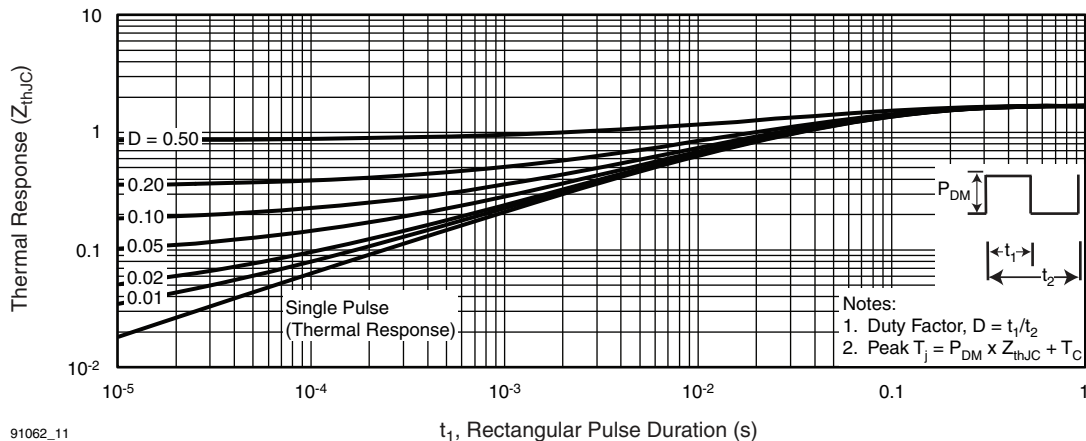


Fig. 10b - Switching Time Waveforms



91062_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

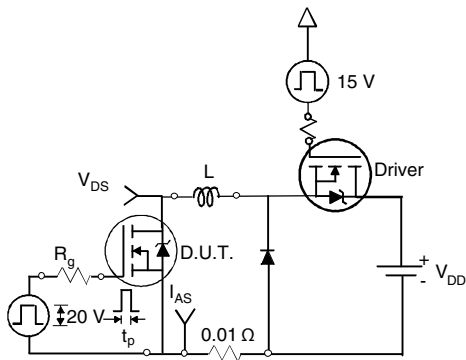


Fig. 12a - Unclamped Inductive Test Circuit

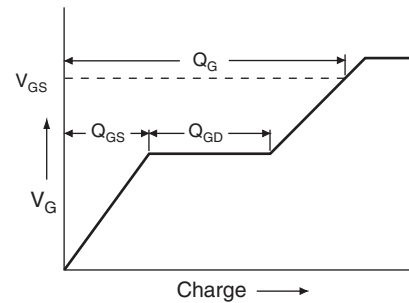


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

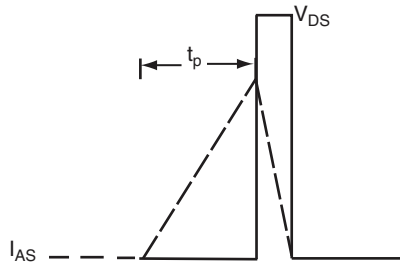


Fig. 12b - Unclamped Inductive Waveforms

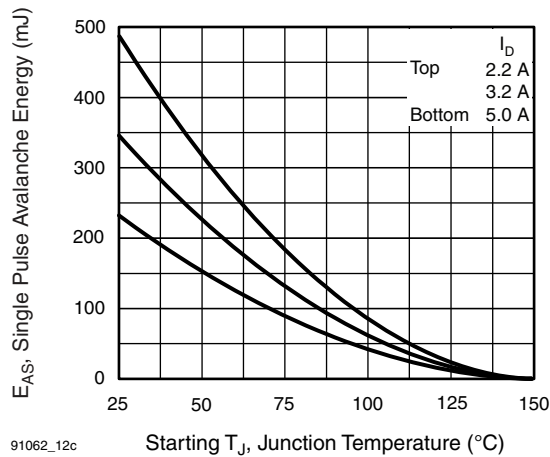


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

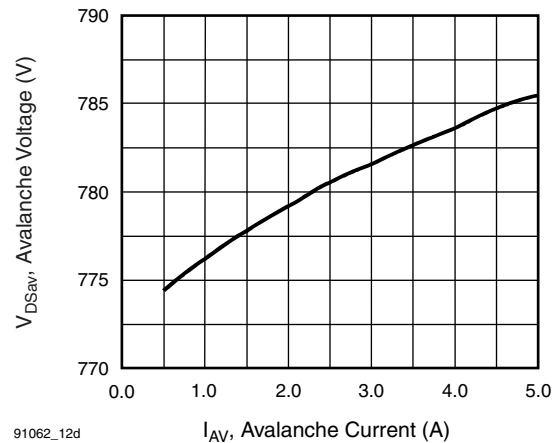


Fig. 12d - Basic Gate Charge Waveform

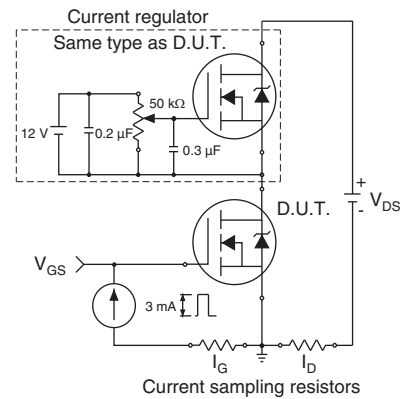
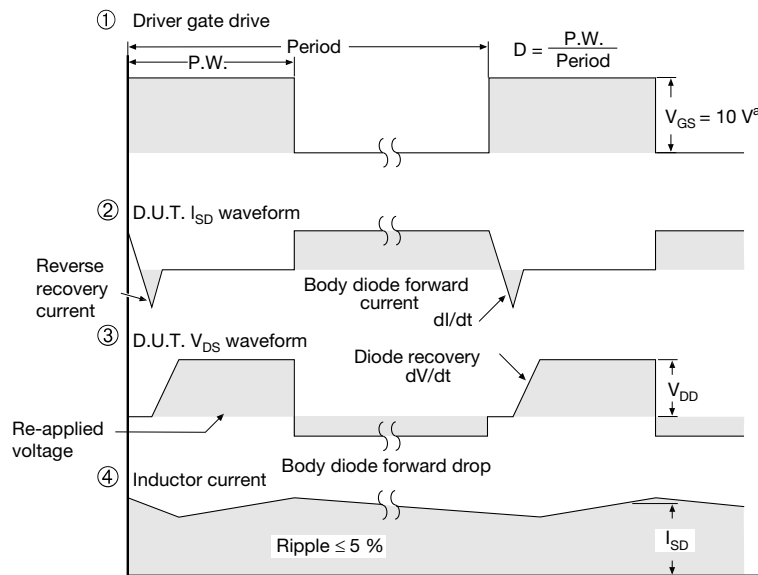
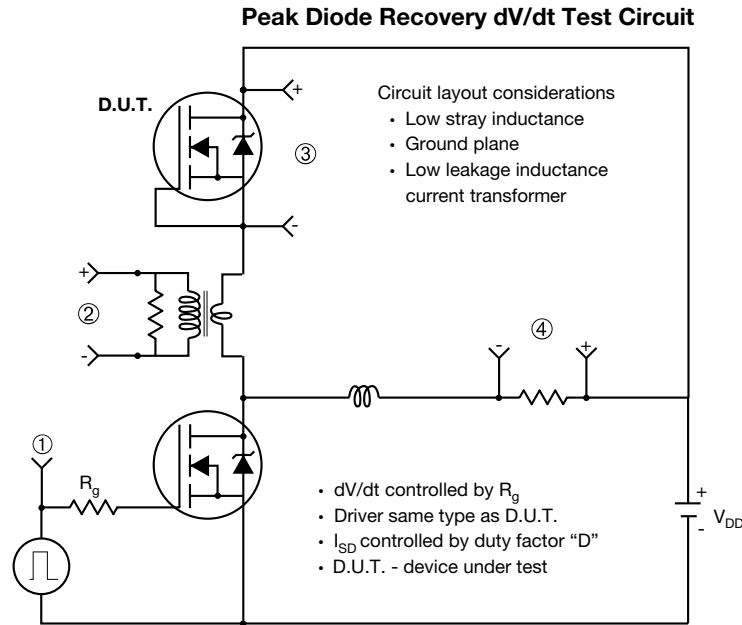


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

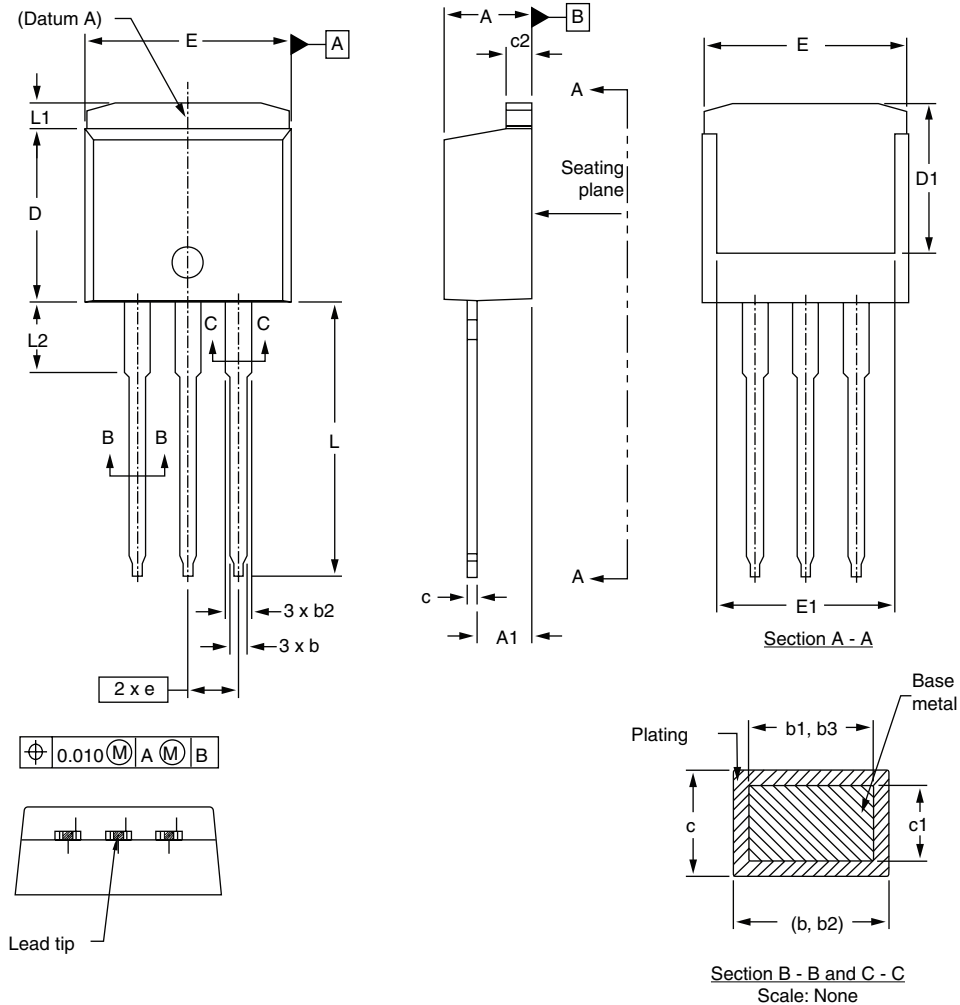
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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