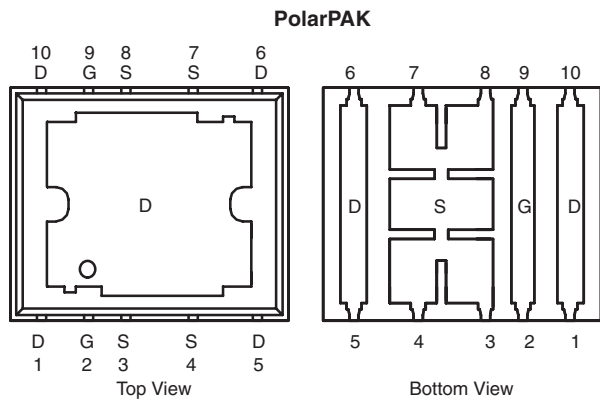




# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) <sup>e</sup>	I <sub>D</sub> (A) <sup>a</sup>		Q <sub>g</sub> (Typ.)
		Silicon Limit	Package Limit	
30	0.0032 at V <sub>GS</sub> = 10 V	134	50	23 nC
	0.0041 at V <sub>GS</sub> = 4.5 V	119	50	

Package Drawing  
[www.vishay.com/doc?68797](http://www.vishay.com/doc?68797)



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE862DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	134 (Silicon Limit)	A
		T <sub>C</sub> = 70 °C	50 <sup>a</sup> (Package Limit)	
		T <sub>A</sub> = 25 °C	50 <sup>a</sup>	
		T <sub>A</sub> = 70 °C	30 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	100		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	50 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	4.3 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	40		
Avalanche Energy	E <sub>AS</sub>	80	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	104	W
		T <sub>C</sub> = 70 °C	66	
		T <sub>A</sub> = 25 °C	5.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	3.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

## FEATURES

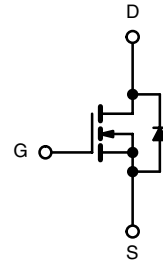
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Gen III Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK<sup>®</sup> Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
  - Die Not Exposed
  - Same Layout Regardless of Die Size ≤ 100 V
- Low Q<sub>gd</sub>/Q<sub>gs</sub> Ratio Helps Prevent Shoot-Through
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS directive 2002/95/EC



RoHS  
COMPLIANT  
HALOGEN  
FREE  
Available

## APPLICATIONS

- VRM
- DC/DC Conversion
- Synchronous Rectification
- POL



N-Channel MOSFET  
For Related Documents  
[www.vishay.com/ppg?65026](http://www.vishay.com/ppg?65026)

**THERMAL RESISTANCE RATINGS**

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	$R_{thJC}$ (Drain)	1	1.2	
Maximum Junction-to-Case (Source) <sup>a, c</sup>		$R_{thJC}$ (Source)	2.8	3.4	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.  
b. Maximum under Steady State conditions is 68 °C/W.  
c. Measured at source pin (on the side of the package).

**SPECIFICATIONS  $T_J = 25$  °C, unless otherwise noted**

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ $\mu$ A		31		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	1.2	1.65	2.2	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30$ V, $V_{GS} = 0$ V			1	$\mu$ A
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	25			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 20$ A		0.0026	0.0032	$\Omega$
		$V_{GS} = 4.5$ V, $I_D = 20$ A		0.0034	0.0038	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10$ V, $I_D = 20$ A		90		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz		3100		pF
Output Capacitance	$C_{oss}$			610		
Reverse Transfer Capacitance	$C_{rss}$			215		
Total Gate Charge	$Q_g$	$V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 20$ A		48	75	nC
		$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A		23	35	
Gate-Source Charge	$Q_{gs}$			8		
Gate-Drain Charge	$Q_{gd}$		6.8			
Gate Resistance	$R_g$	$f = 1$ MHz	0.3	1.4	2.8	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.5$ $\Omega$ $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ $\Omega$		30	45	ns
Rise Time	$t_r$			20	30	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	$t_f$			15	25	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.5$ $\Omega$ $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$		12	20	
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	$t_f$			15	25	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C			50	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				100	
Body Diode Voltage	$V_{SD}$	$I_S = 10$ A		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C		40	60	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			40	60	nC
Reverse Recovery Fall Time	$t_a$			21		ns
Reverse Recovery Rise Time	$t_b$			19		

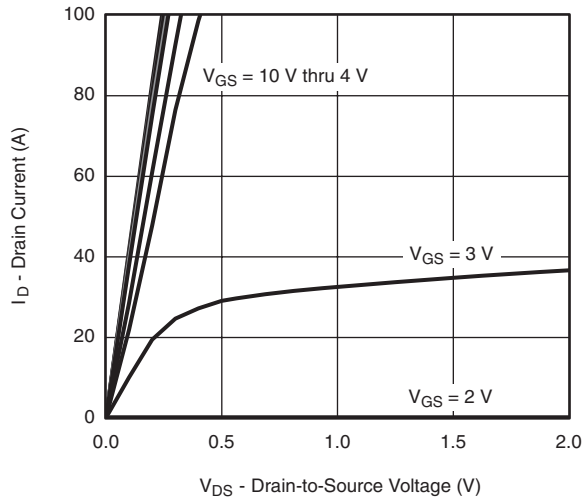
Notes:

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.  
b. Guaranteed by design, not subject to production testing.

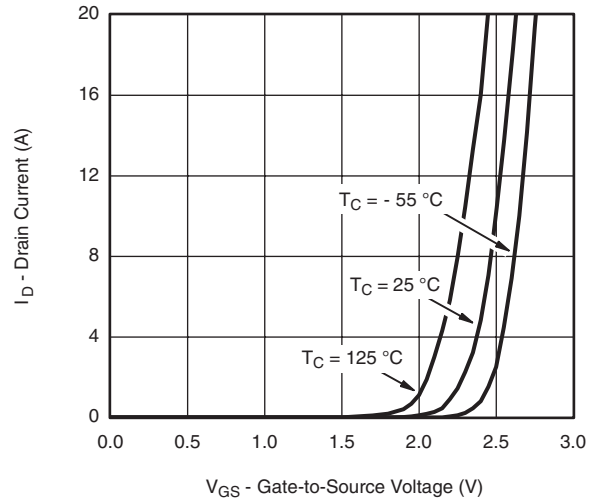
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



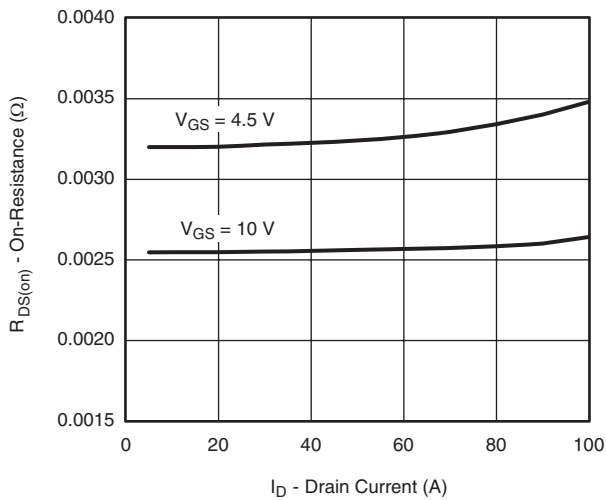
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



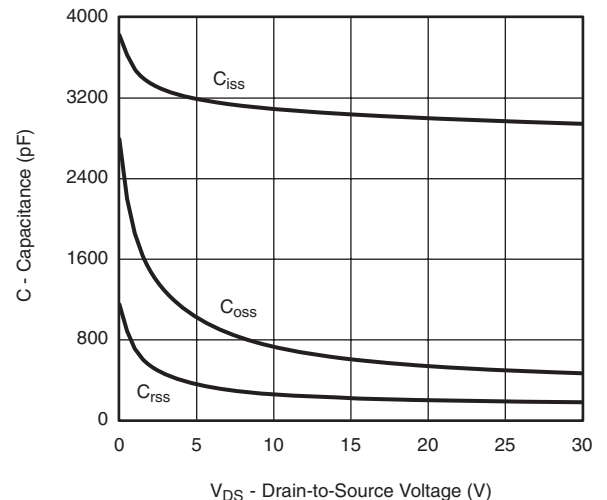
**Output Characteristics**



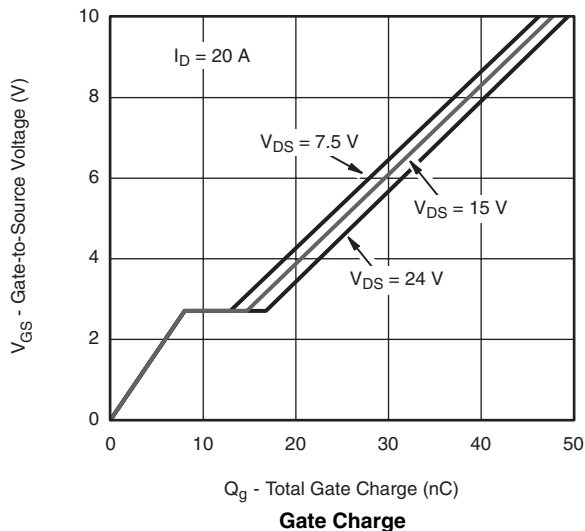
**Transfer Characteristics**



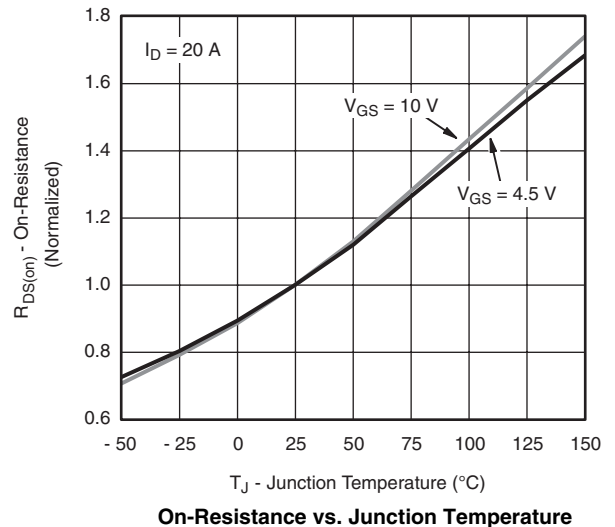
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



**Gate Charge**



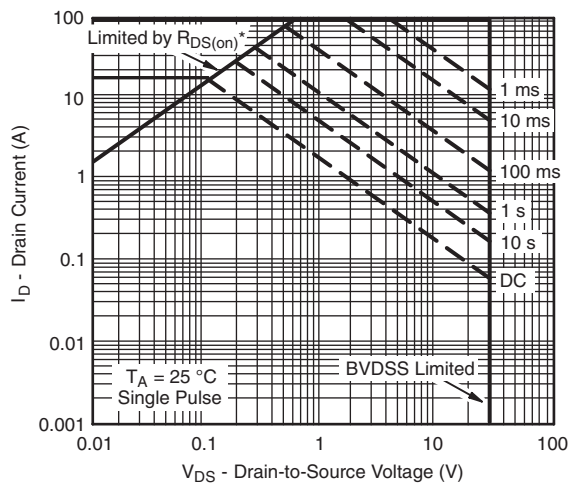
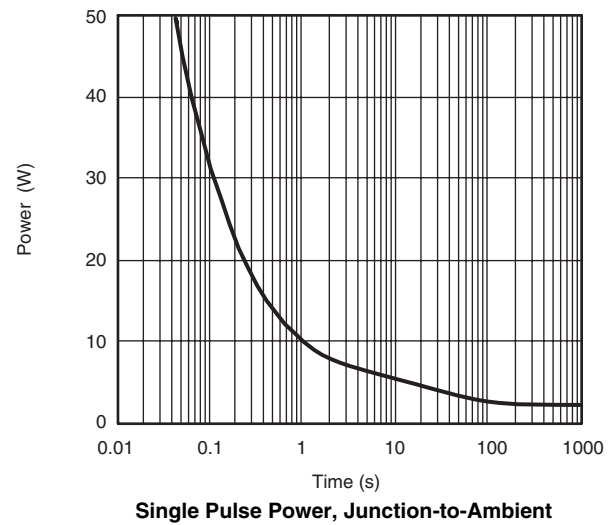
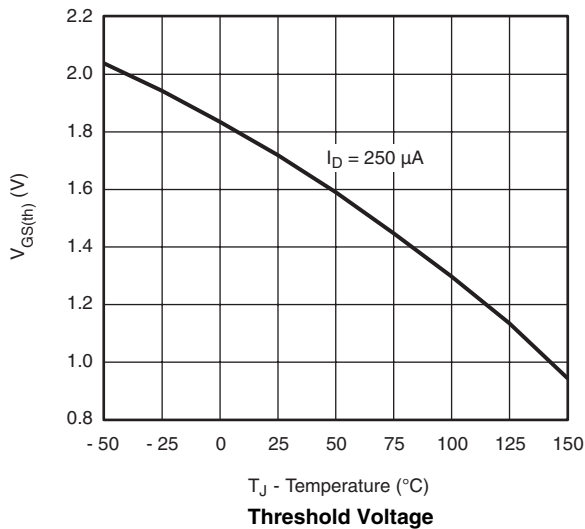
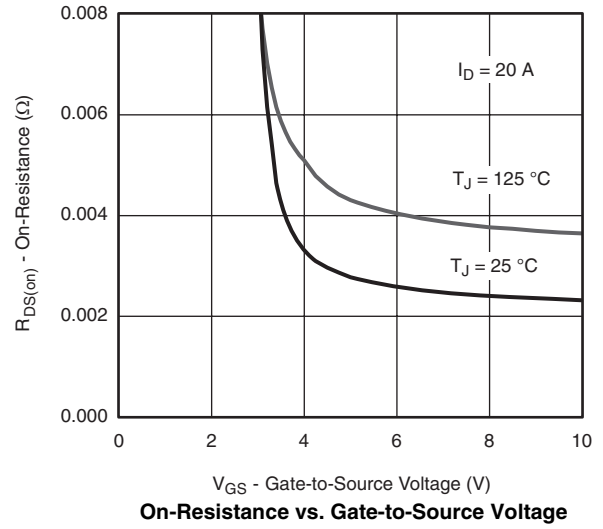
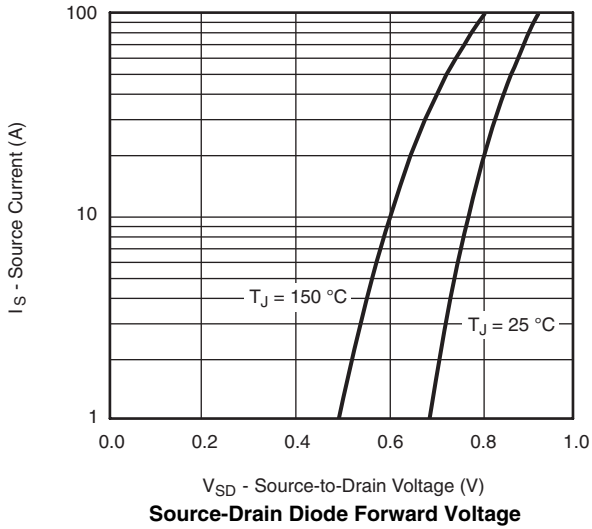
**On-Resistance vs. Junction Temperature**

# SiE862DF

Vishay Siliconix



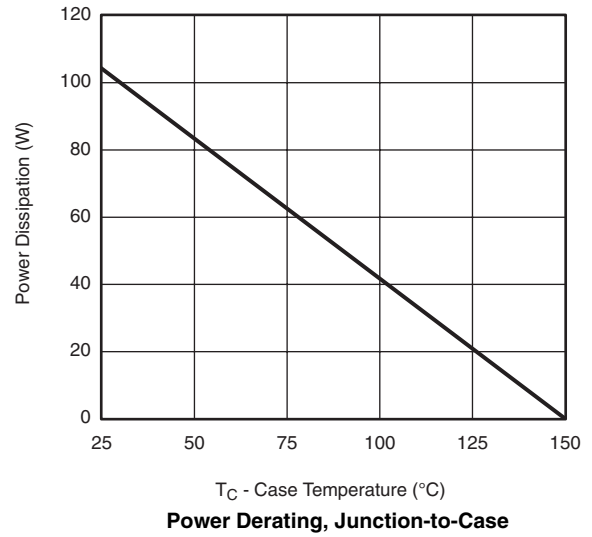
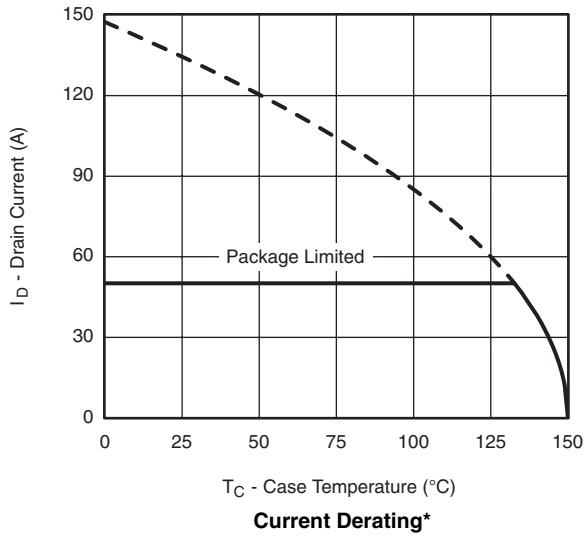
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



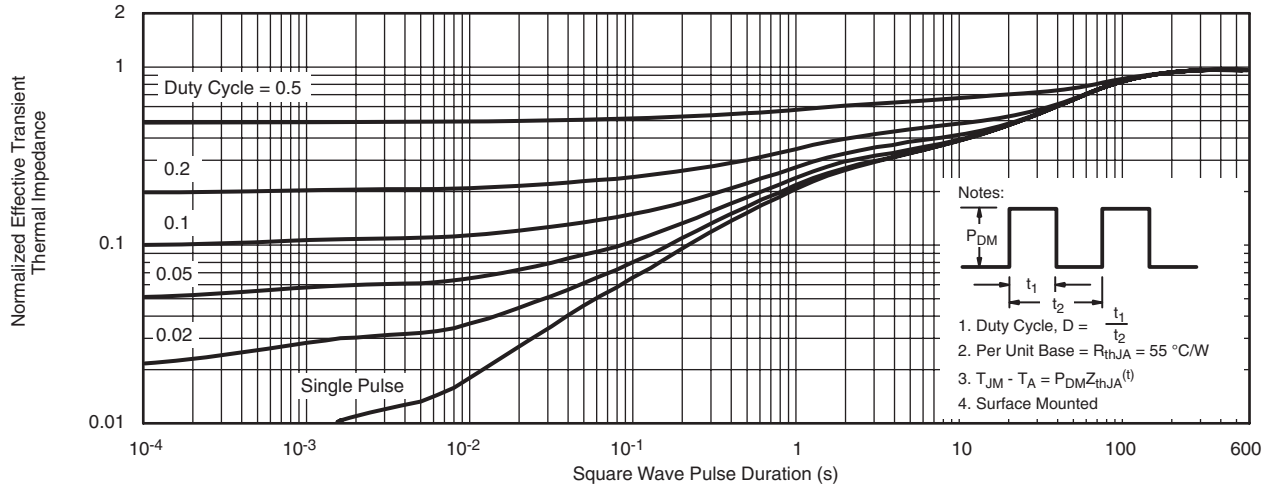
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# SiE862DF

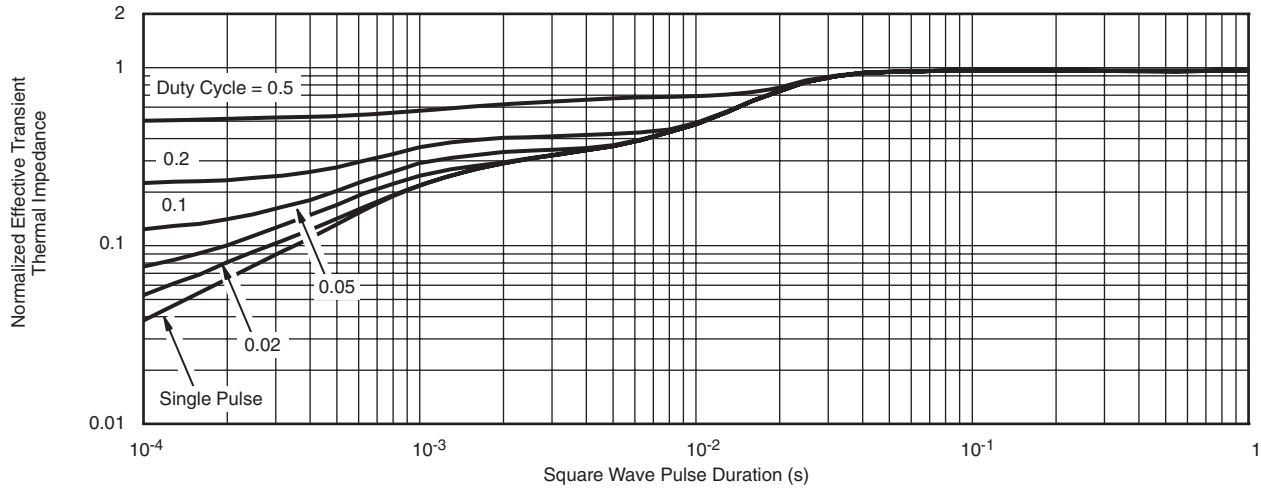
Vishay Siliconix



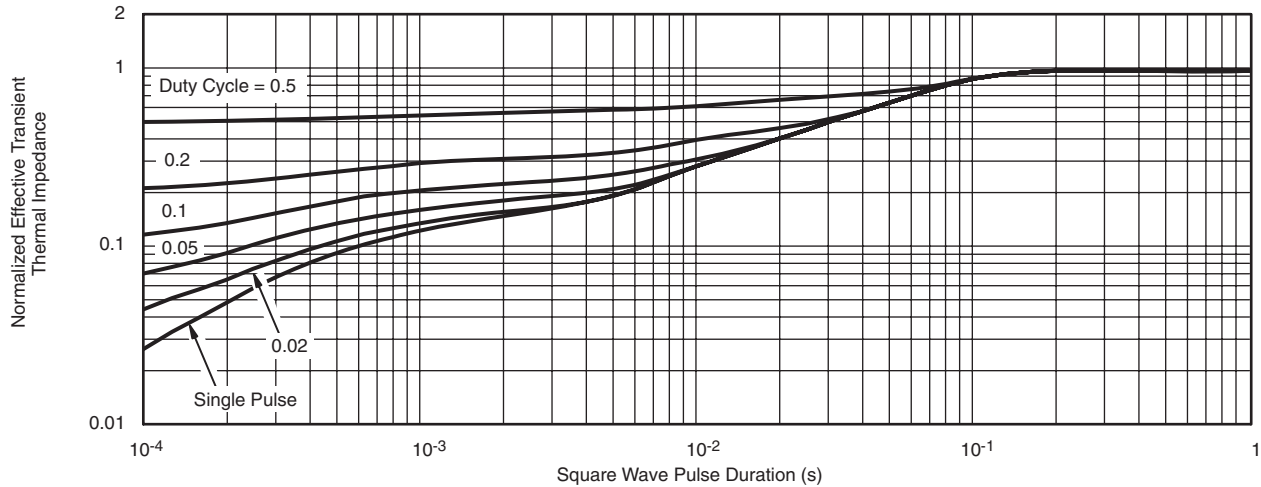
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



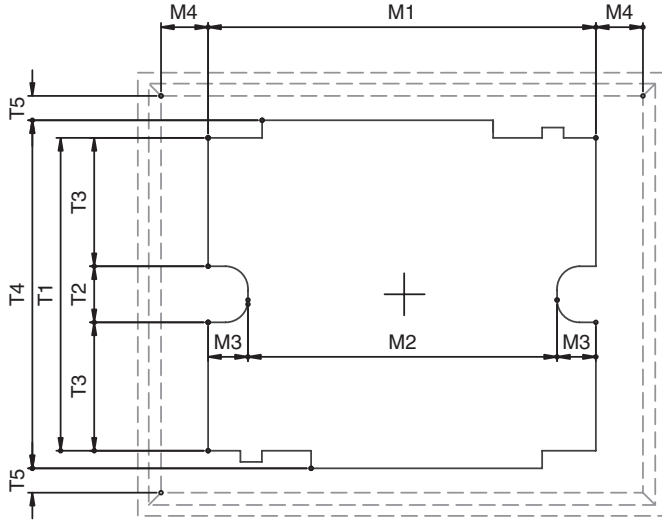
Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)



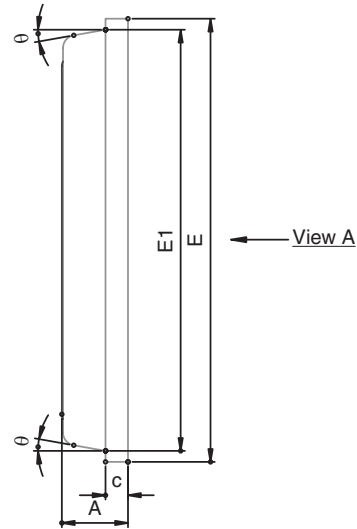
Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?65026](http://www.vishay.com/ppg?65026).

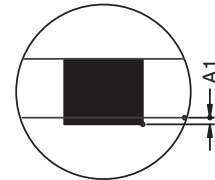
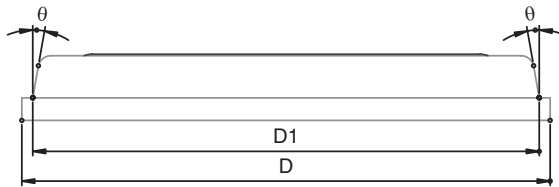
## POLARPAK™ OPTION U



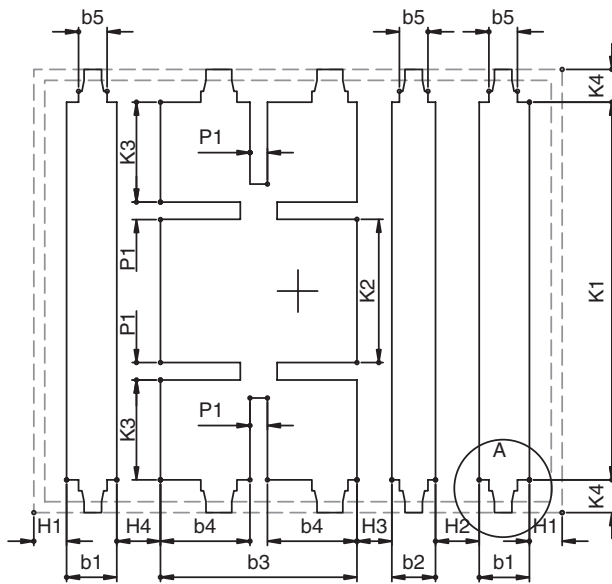
(Top View)



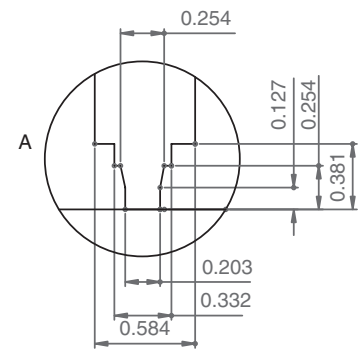
View A



DETAIL Z



View A  
(Bottom View)



# Package Information

Vishay Siliconix



DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	-	0.05	0.000	-	0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6.00	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23	-	-	0.009	-	-
H2	0.45	-	0.56	0.018	-	0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45	-	0.56	0.018	-	0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.62	1.67	1.72	0.064	0.066	0.068
K3	1.16	-	-	0.046	-	-
K4	0.24	-	-	0.009	-	-
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22	-	-	0.009	-	-
M4	0.05	-	-	0.002	-	-
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20	-	-	0.047	-	-
T4	3.90	-	-	0.153	-	-
T5	0	0.18	0.36	0.000	0.007	0.014
θ	0°	10°	12°	0°	10°	12°

ECN: T-08441-Rev. A, 11-Aug-08  
DWG: 5966

## Notes

Millimeters govern over inches.



## RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S  
 Dimensions in mm/(Inches)  
 No External Traces within Broken Lines  
 Dot indicates Gate Pin (Part Marking)



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