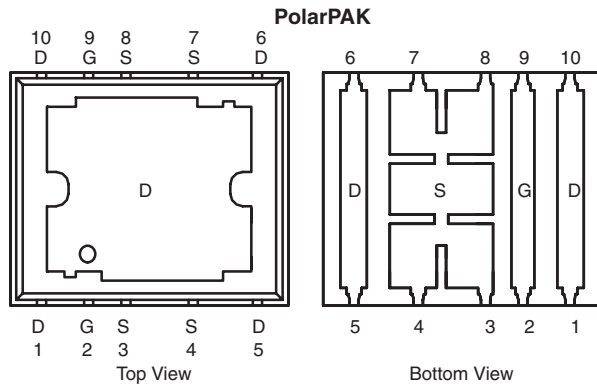




N-Channel 30-V (D-S) MOSFET

| PRODUCT SUMMARY | | | | |
|---------------------|--------------------------------------|--------------------|-----------------|-----------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) ^e | I _D (A) | | Q _g (Typ.) |
| | | Silicon Limit | Package Limit | |
| 30 | 0.0021 at V _{GS} = 10 V | 178 | 60 ^a | 34 nC |
| | 0.0028 at V _{GS} = 4.5 V | 154 | 60 ^a | |

Package Drawing
www.vishay.com/doc?68796



Top surface is connected to pins 1, 5, 6, and 10
Ordering Information: SiE860DF-T1-E3 (Lead (Pb)-free)
 SiE860DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

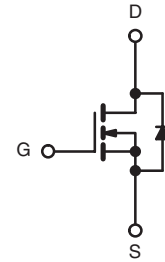
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Gen III Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC



APPLICATIONS

- VRM, POL
- DC/DC Conversion
- Synchronous Rectification
- Server



N-Channel MOSFET
 For Related Documents
www.vishay.com/ppg?68786

| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | |
|---|-----------------------------------|------------------------|---------------------------------|----|
| Parameter | Symbol | Limit | Unit | |
| Drain-Source Voltage | V _{DS} | 30 | | V |
| Gate-Source Voltage | V _{GS} | ± 20 | | |
| Continuous Drain Current (T _J = 150 °C) | I _D | T _C = 25 °C | 178 (Silicon Limit) | A |
| | | T _C = 70 °C | 60 ^a (Package Limit) | |
| | | T _A = 25 °C | 60 ^a | |
| | | T _A = 70 °C | 38 ^{b, c} | |
| Pulsed Drain Current | I _{DM} | 80 | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | 60 ^a | |
| | | T _A = 25 °C | 4.3 ^{b, c} | |
| Single Pulse Avalanche Current | I _{AS} | 50 | | |
| Avalanche Energy | E _{AS} | 125 | | mJ |
| Maximum Power Dissipation | P _D | T _C = 25 °C | 104 | W |
| | | T _C = 70 °C | 66 | |
| | | T _A = 25 °C | 5.2 ^{b, c} | |
| | | T _A = 70 °C | 3.3 ^{b, c} | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 150 | | °C |
| Soldering Recommendations (Peak Temperature) ^{d, e} | | 260 | | |

Notes:

- Package limited at 60 A.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (www.vishay.com/ppg?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

| Parameter | | Symbol | Typical | Maximum | Unit |
|---|---------------|---------------------|---------|---------|------|
| Maximum Junction-to-Ambient ^{a, b} | $t \leq 10$ s | R_{thJA} | 20 | 24 | °C/W |
| Maximum Junction-to-Case (Drain Top) | Steady State | R_{thJC} (Drain) | 0.9 | 1.1 | |
| Maximum Junction-to-Case (Source) ^{a, c} | | R_{thJC} (Source) | 2.7 | 3.3 | |

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
 b. Maximum under Steady State conditions is 68 °C/W.
 c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|--|-------------------------|--|-------|--------|-----------|----------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0$ V, $I_D = 250$ μ A | 30 | | | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D = 250$ μ A | | 30 | | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | - 6.1 | | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250$ μ A | 1.0 | | 2.5 | V |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0$ V, $V_{GS} = \pm 20$ V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 30$ V, $V_{GS} = 0$ V | | | 1 | μ A |
| | | $V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55$ °C | | | 10 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \geq 5$ V, $V_{GS} = 10$ V | 25 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10$ V, $I_D = 21.7$ A | | 0.0017 | 0.0021 | Ω |
| | | $V_{GS} = 4.5$ V, $I_D = 19$ A | | 0.0023 | 0.0028 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15$ V, $I_D = 21.7$ A | | 110 | | S |
| Dynamic^b | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz | | 4500 | | pF |
| Output Capacitance | C_{oss} | | 850 | | | |
| Reverse Transfer Capacitance | C_{rss} | | 300 | | | |
| Total Gate Charge | Q_g | $V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 20$ A | | 70 | 105 | nC |
| | | $V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A | | 34 | 51 | |
| Gate-Source Charge | Q_{gs} | | 14 | | | |
| Gate-Drain Charge | Q_{gd} | | 9 | | | |
| Gate Resistance | R_g | $f = 1$ MHz | | 0.9 | 1.8 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 15$ V, $R_L = 1.5$ Ω $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω | | 35 | 55 | ns |
| Rise Time | t_r | | 20 | 30 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 50 | 75 | | |
| Fall Time | t_f | | 30 | 45 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 15$ V, $R_L = 1.5$ Ω $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω | | 16 | 25 | |
| Rise Time | t_r | | 10 | 15 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 40 | 30 | | |
| Fall Time | t_f | | 10 | 15 | | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25$ °C | | | 60 | A |
| Pulse Diode Forward Current ^a | I_{SM} | | | | 80 | |
| Body Diode Voltage | V_{SD} | $I_S = 10$ A | | 0.8 | 1.2 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $I_F = 10$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C | | 35 | 55 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 30 | 45 | nC |
| Reverse Recovery Fall Time | t_a | | | 21 | | ns |
| Reverse Recovery Rise Time | t_b | | | 14 | | |

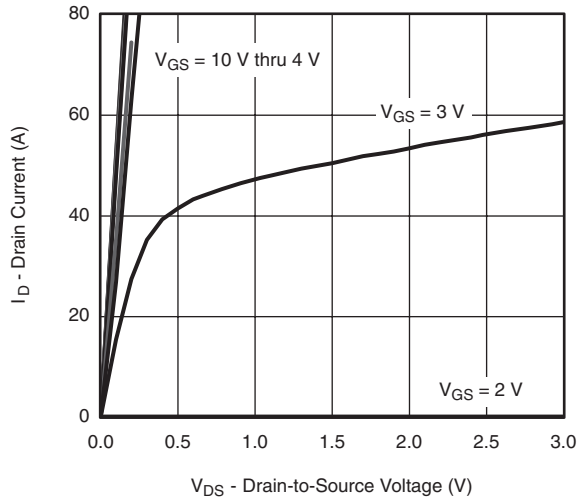
Notes:

- a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
 b. Guaranteed by design, not subject to production testing.

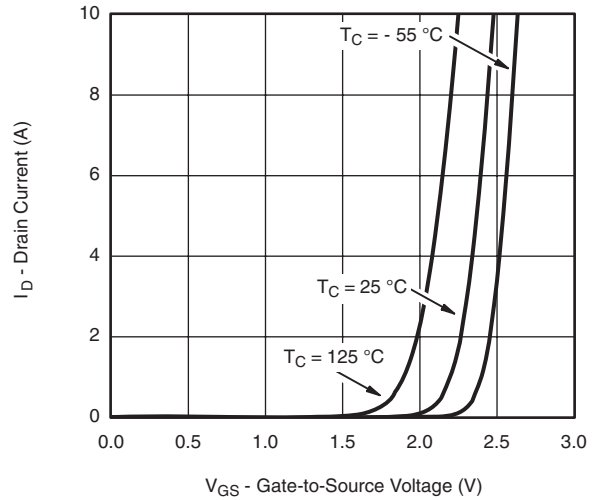
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



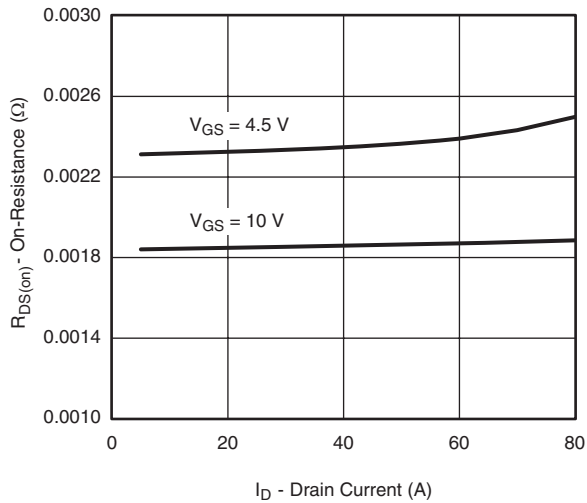
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



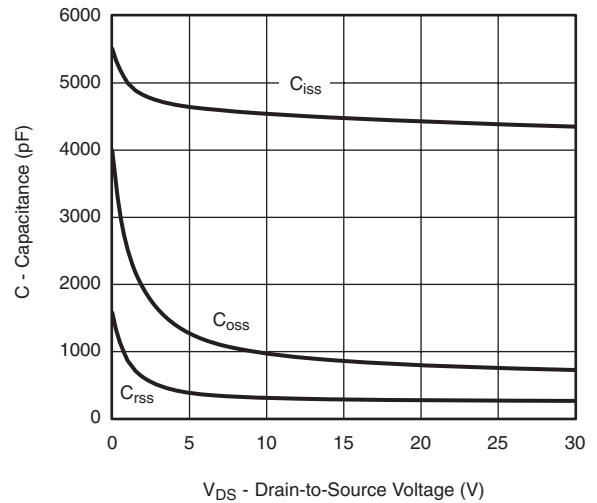
Output Characteristics



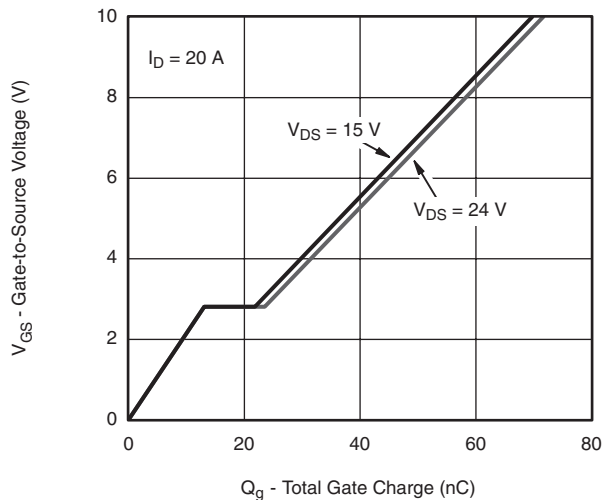
Transfer Characteristics



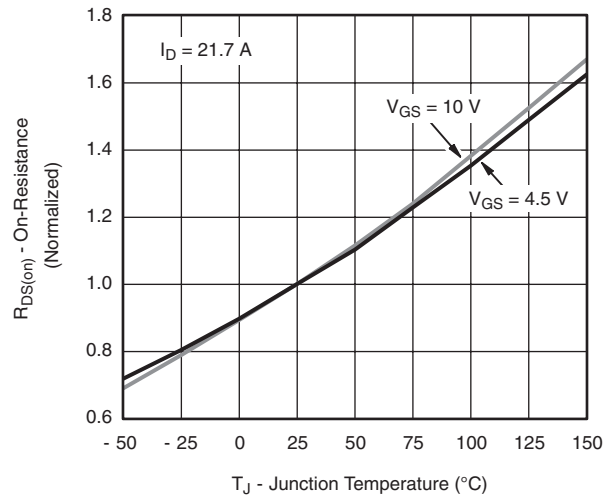
On-Resistance vs. Drain Current



Capacitance



Gate Charge



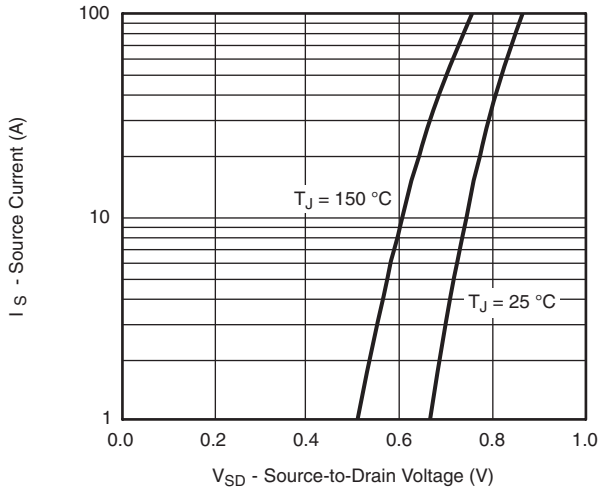
On-Resistance vs. Junction Temperature

SiE860DF

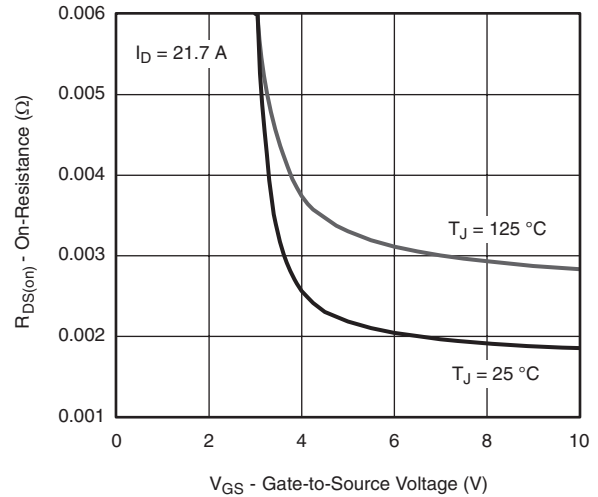
Vishay Siliconix



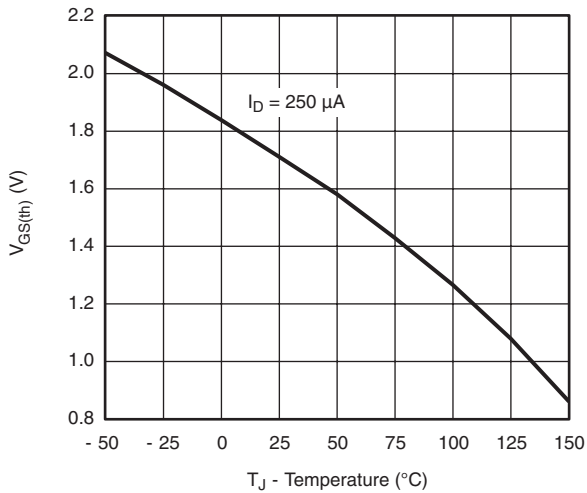
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



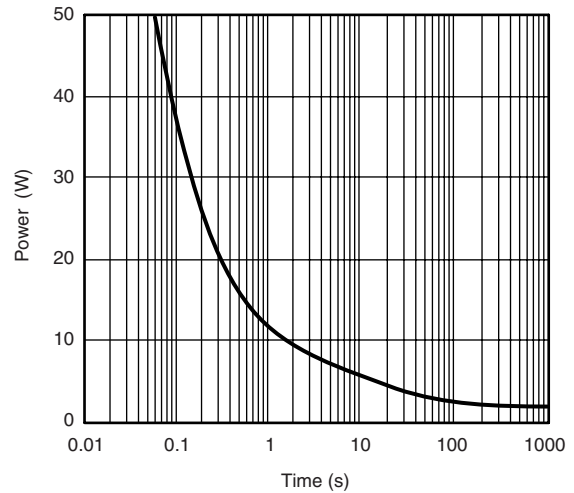
Source-Drain Diode Forward Voltage



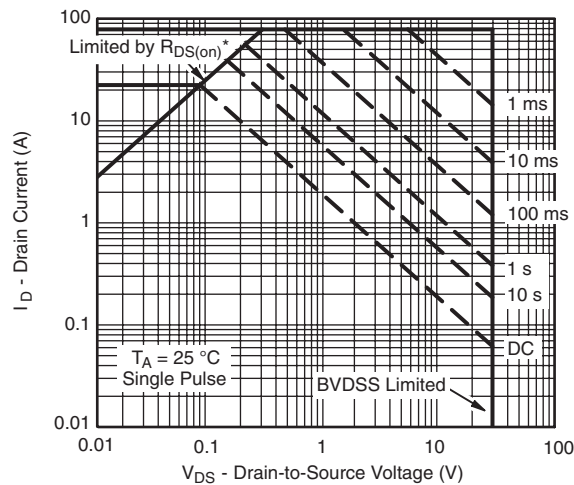
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

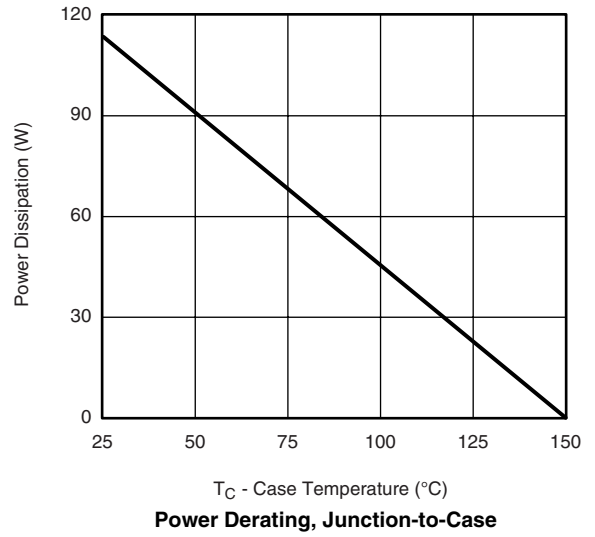
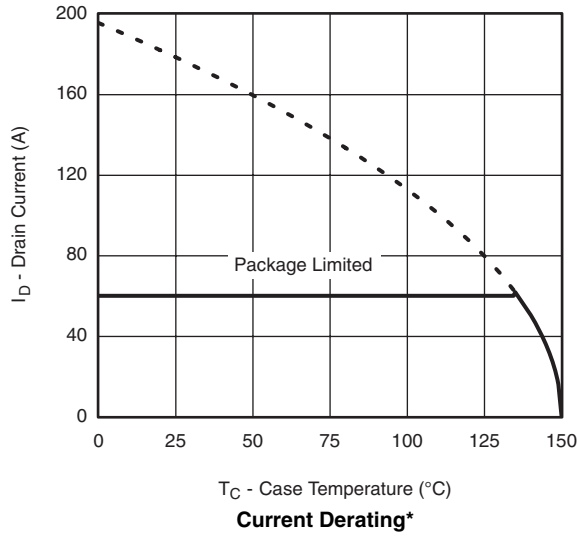


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



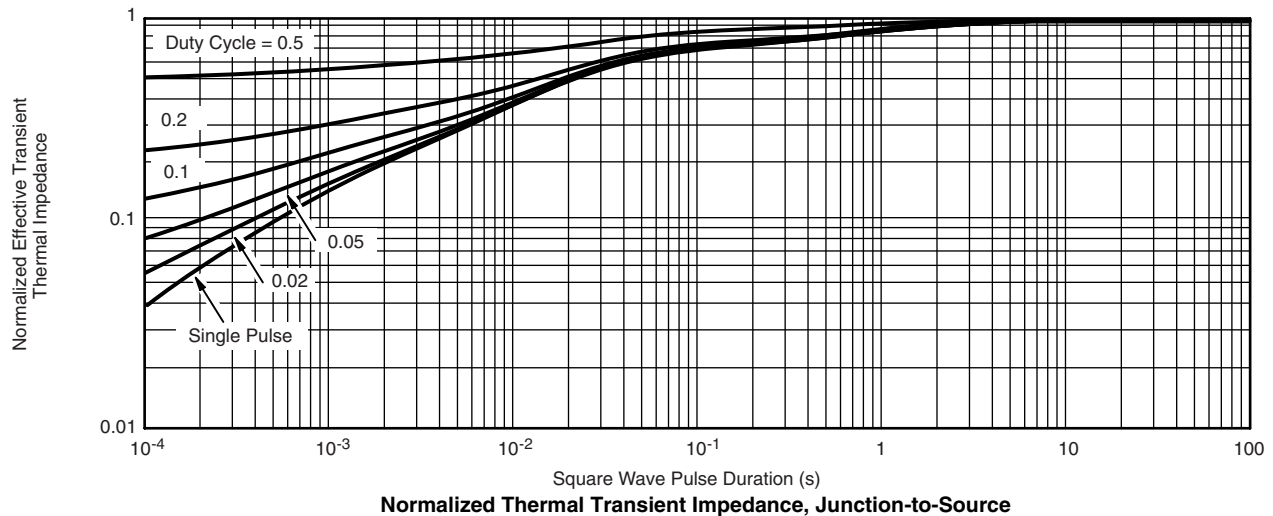
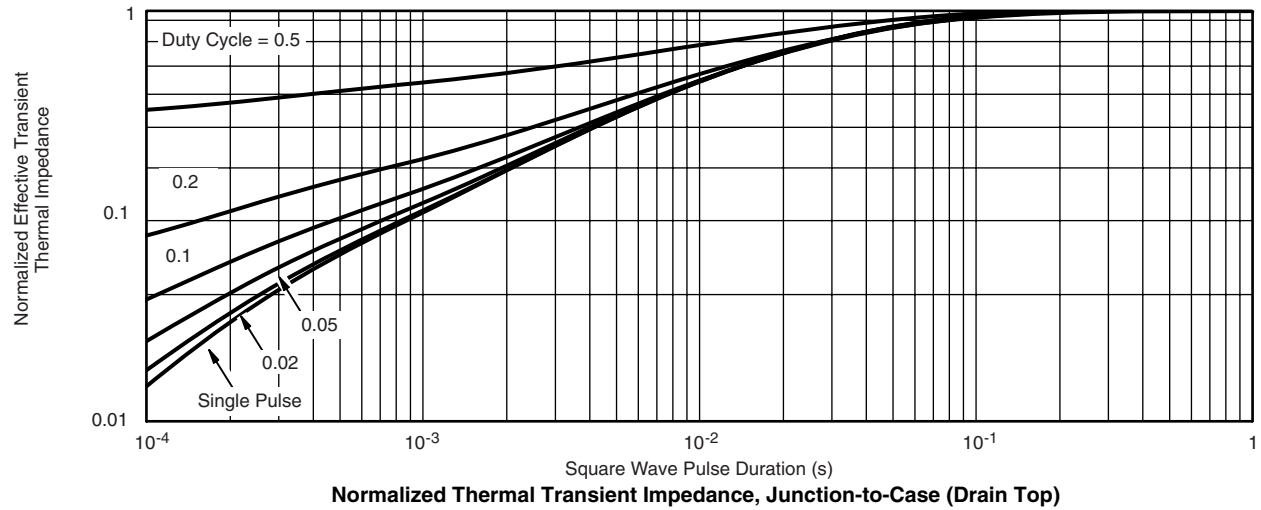
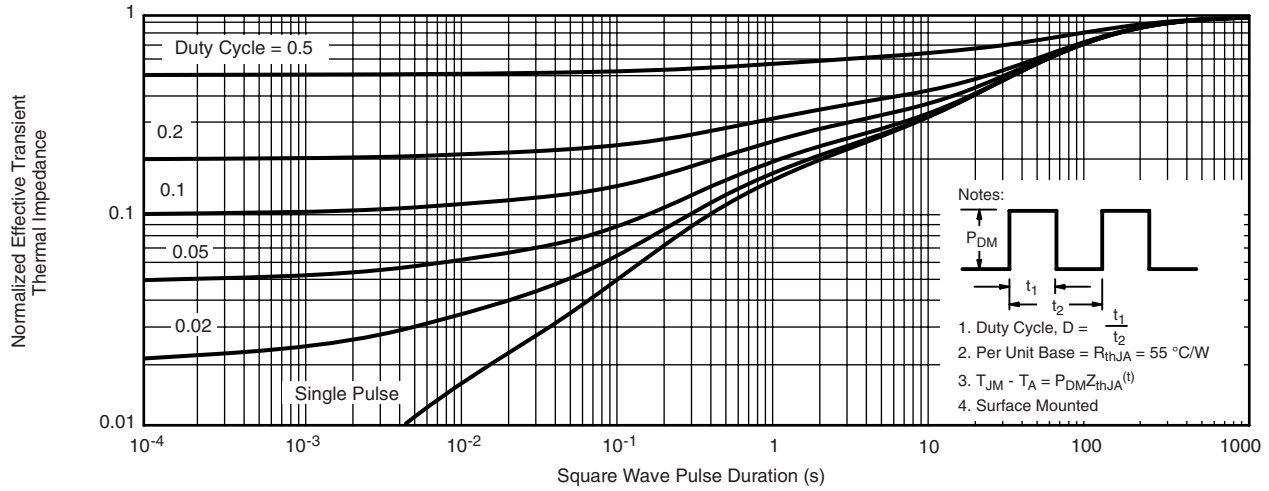
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiE860DF

Vishay Siliconix

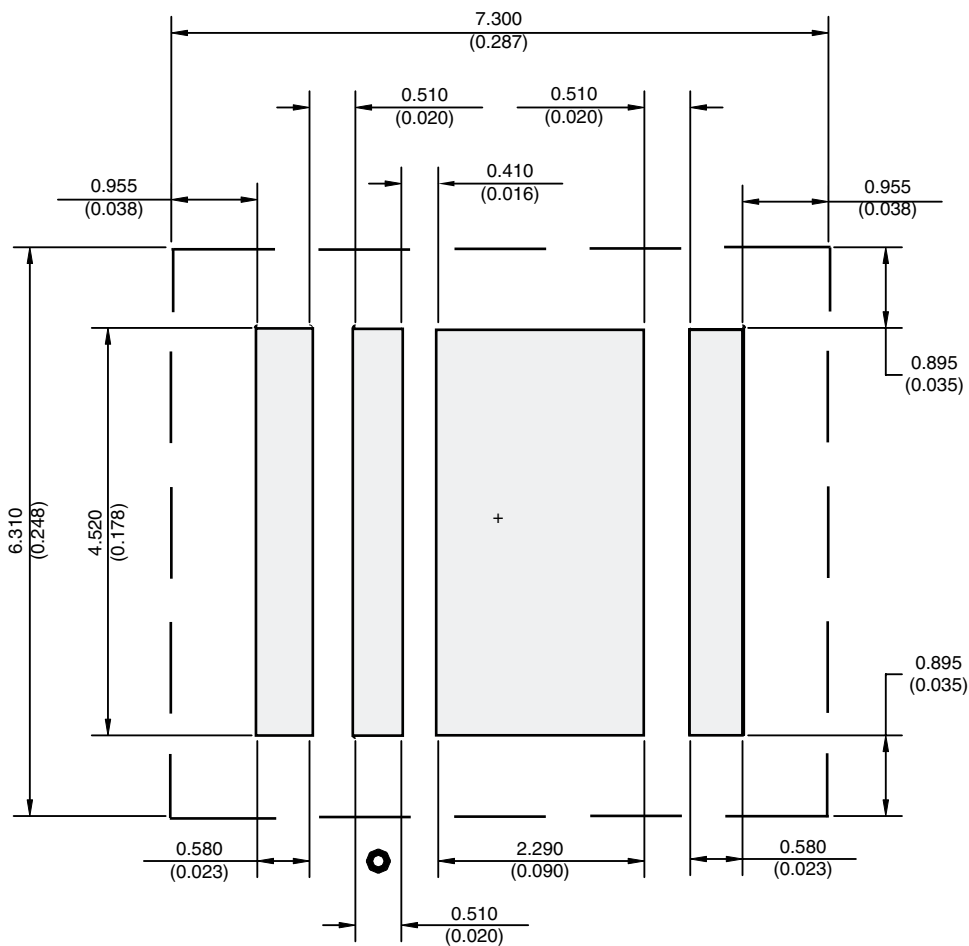


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68786.

RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S
 Dimensions in mm/(Inches)
 No External Traces within Broken Lines
 Dot indicates Gate Pin (Part Marking)



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