

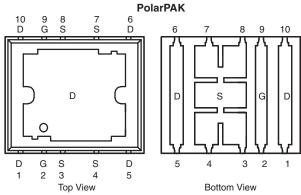
Vishay Siliconix

## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) I <sub>D</sub> (A) <sup>e</sup>		Q <sub>g</sub> (Typ.)			
30	0.007 at V <sub>GS</sub> = 10 V	44.5	13.1 nC			
	0.010 at $V_{GS}$ = 4.5 V	37.3	13.1110			

Package Drawing

www.vishay.com/doc?72945



### **FEATURES**

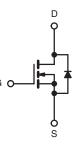
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Gen II Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK<sup>®</sup> Package for Double-Sided Cooling



- COMPLIANT HALOGEN FREE ailable
- Leadframe-Based New Encapsulated Package - Die Not Exposed
  - Same Layout Regardless of Die Size
- Low Q<sub>ad</sub>/Q<sub>as</sub> Ratio Helps Prevent Shoot-Through
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS directive 2002/95/EC

#### APPLICATIONS

- VRM, POL
- DC/DC Conversion
- Server
- **High-Side Switch**



N-Channel MOSFET For Related Documents www.vishay.com/ppg?69988

Top surface is connected to pins 1, 5, 6, and 10 Ordering Information: SiE844DF-T1-E3 (Lead (Pb)-free)

SiE844DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### ABSOLUTE MAXIMUM RATINGS T<sub>A</sub> = 25 °C, unless otherwise noted Parameter Symbol Limit Unit Drain-Source Voltage V<sub>DS</sub> 30 v Gate-Source Voltage V<sub>GS</sub> ± 20 T<sub>C</sub> = 25 °C 44.5 T<sub>C</sub> = 70 °C 35.6 Continuous Drain Current (T<sub>J</sub> = 150 °C) $I_D$ T<sub>A</sub> = 25 °C 20.3<sup>a, b</sup> T<sub>A</sub> = 70 °C 16.3<sup>a, b</sup> А Pulsed Drain Current Ī<sub>DM</sub> 60 T<sub>C</sub> = 25 °C 20.8 Continuous Source-Drain Diode Current Is T<sub>A</sub> = 25 °C 4.3<sup>a, b</sup> Single Pulse Avalanche Current IAS 25 L = 0.1 mHAvalanche Energy EAS 31 mJ T<sub>C</sub> = 25 °C 25 $T_{\rm C} = 70 \ ^{\circ}{\rm C}$ 16 $P_D$ W Maximum Power Dissipation $T_A = 25 \circ C$ 5.2<sup>a, b</sup> T<sub>A</sub> = 70 °C 3.3<sup>a, b</sup> Operating Junction and Storage Temperature Range T<sub>J</sub>, T<sub>stg</sub> - 55 to 150 °C Soldering Recommendations (Peak Temperature)<sup>c, d</sup> 260 Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. See Solder Profile (www.vishay.com/ppg?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Based on  $T_C = 25$  °C.

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THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient <sup>a, b</sup>	t ≤ 10 s	R <sub>thJA</sub>	20	24					
Maximum Junction-to-Case (Drain Top)	Steady State	R <sub>thJC</sub> (Drain)	4	5	°C/W				
Maximum Junction-to-Case (Source) <sup>a, c</sup>	Sleady Slale	R <sub>thJC</sub> (Source)	5.5	7					

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 68 °C/W.

c. Measured at source pin (on the side of the package).

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	-						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			30		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1		3	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	- μΑ	
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 V$ , $V_{GS} = 10 V$	25			Α	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12.1 A		0.0058	0.007	Ω	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.7 A		0.0081	0.010		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 12.1 A		65		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			2150		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		320			
Reverse Transfer Capacitance	C <sub>rss</sub>			120	<u>+</u>		
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		29	44	nC	
		$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		13.1	20		
Gate-Source Charge	Q <sub>gs</sub>			6			
Gate-Drain Charge	Q <sub>gd</sub>			3.1			
Gate Resistance	Ř <sub>g</sub>	f = 1 MHz		1.2	1.8	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			25	40		
Rise Time	tr	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		10	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	${ m I}_{ m D}\cong$ 10 A, ${ m V}_{ m GEN}$ = 4.5 V, ${ m R}_{ m q}$ = 1 $\Omega$		25	40		
Fall Time	t <sub>f</sub>	Ű		10	15		
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	ns	
Rise Time	tr	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		10	15	115	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ 10 A, $V_{GEN}$ = 10 V, $R_q$ = 1 $\Omega$		25	40	-	
Fall Time	t <sub>f</sub>	C C		10	15		
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	T <sub>C</sub> = 25 °C			20.8	Τ.	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				60	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			30	45	ns	
dy Diode Beyerse Becovery Charge Que			24	36	nC		
Reverse Recovery Fall Time	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 \text{ °C}$			16			
Reverse Recovery Rise Time	t <sub>b</sub>			14		ns	

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

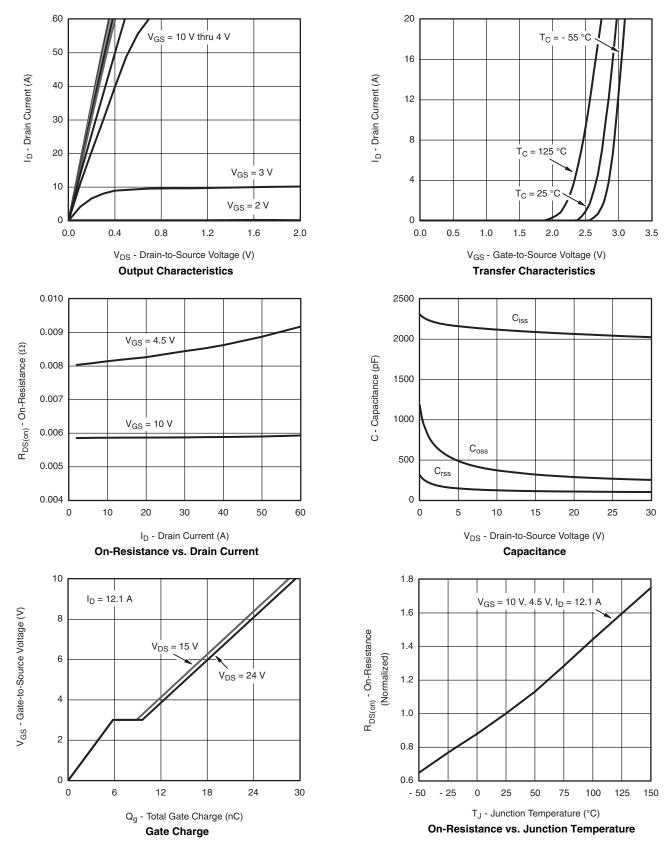
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

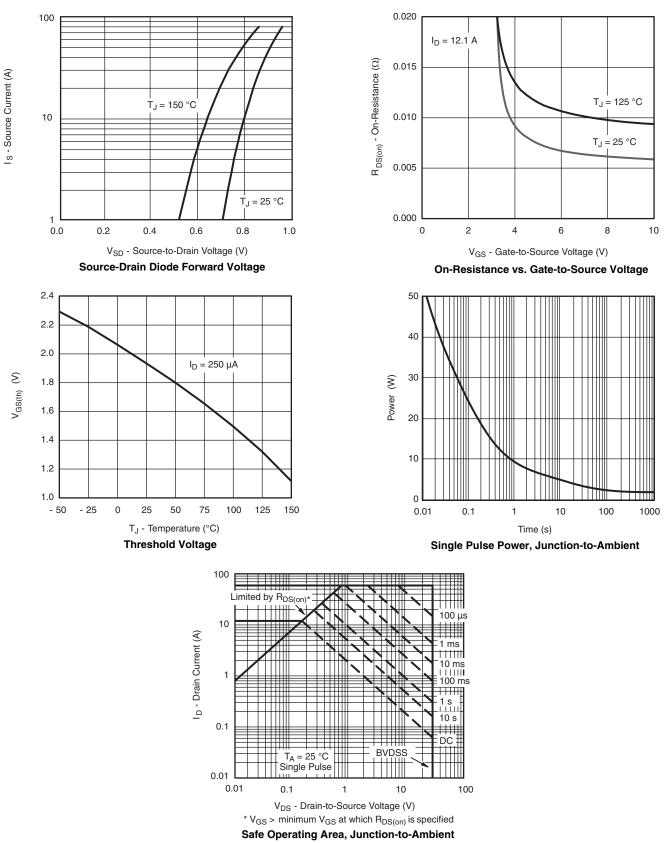


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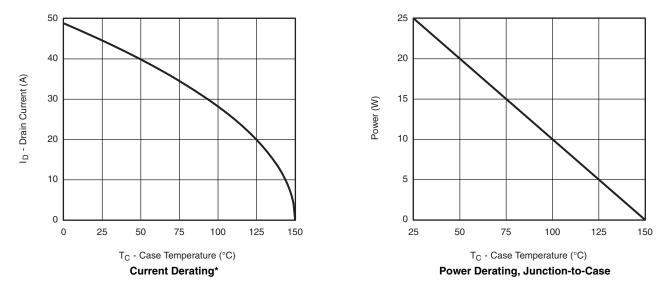
#### **New Product**



# SiE844DF

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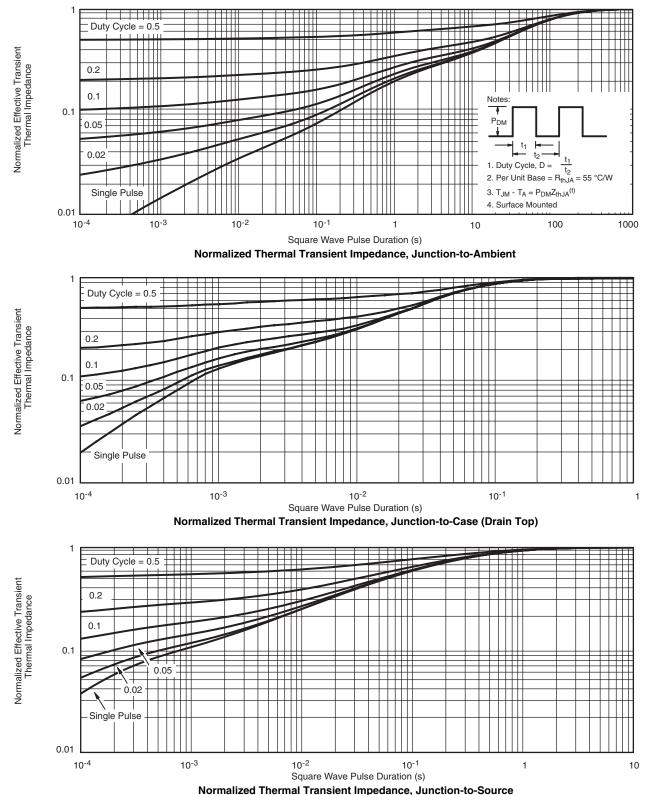


\* The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?69988">www.vishay.com/ppg?69988</a>.



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