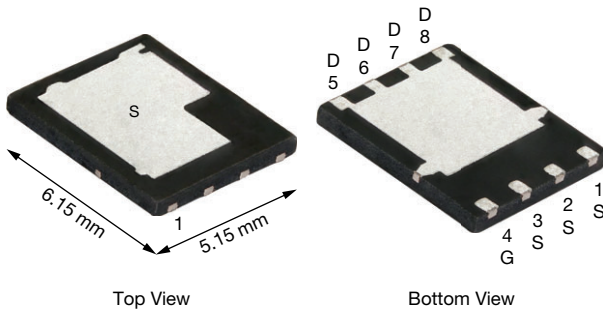


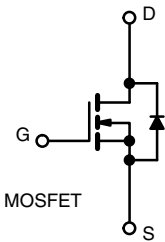
## N-Channel 60 V (D-S) 175 °C MOSFET

**PowerPAK® SO-8DC**

**FEATURES**

- TrenchFET® Gen IV power MOSFET
- Very low  $R_{DS} - Q_g$  figure of merit (FOM)
- Tuned for the lowest  $R_{DS} - Q_{oss}$  FOM
- 100 %  $R_g$  and UIS tested
- Top side cooling feature provides additional venue for thermal transfer
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**
**APPLICATIONS**

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Solar micro inverter
- Motor drive switch
- Battery and load switch
- Industrial



N-Channel MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00174
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0021
$Q_g$ typ. (nC)	51
$I_D$ (A) <sup>a</sup>	227
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK® SO-8DC
Lead (Pb)-free and halogen-free	SiDR626EP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	60	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	227	A
	$T_C = 70$ °C		190	
	$T_A = 25$ °C		50.8 <sup>b, c</sup>	
	$T_A = 70$ °C		42.5 <sup>b, c</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)		$I_{DM}$	400	
Continuous source-drain diode current	$T_C = 25$ °C	$I_S$	136	
	$T_A = 25$ °C		6.8 <sup>b, c</sup>	
Single pulse avalanche current	L = 0.1 mH	$I_{AS}$	50	
Single pulse avalanche energy		$E_{AS}$	125	mJ
Maximum power dissipation	$T_C = 25$ °C	$P_D$	150	W
	$T_C = 70$ °C		105	
	$T_A = 25$ °C		7.5 <sup>b, c</sup>	
	$T_A = 70$ °C		5.25 <sup>b, c</sup>	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>			260	

**Notes**

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction to ambient <sup>a</sup>	$t \leq 10$ s	$R_{thJA}$	15	20	°C/W	
Maximum junction to case (drain)	Steady state	$R_{thJC}$	0.8	1		
Maximum junction to case (source)	Steady state	$R_{thJC}$	1.1	1.4		

**Notes**

a. Surface mounted on 1" x 1" FR4 board

SPECIFICATIONS ( $T_J = 25$ °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	60	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10$ mA	-	33	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250$ $\mu$ A	-	-8.8	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	-	-	100	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 60$ V, $V_{GS} = 0$ V	-	-	1	$\mu$ A
		$V_{DS} = 60$ V, $V_{GS} = 0$ V, $T_J = 70$ °C	-	-	15	
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 20$ A	-	0.00145	0.00174	$\Omega$
		$V_{GS} = 7.5$ V, $I_D = 20$ A	-	0.00175	0.0021	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15$ V, $I_D = 20$ A	-	78	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 30$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	5130	-	pF
Output capacitance	$C_{oss}$		-	1190	-	
Reverse transfer capacitance	$C_{rss}$		-	39	-	
Total gate charge	$Q_g$	$V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_D = 20$ A	-	68	102	nC
		$V_{DS} = 30$ V, $V_{GS} = 7.5$ V, $I_D = 20$ A	-	51	77	
Gate-source charge	$Q_{gs}$		-	25	-	
Gate-drain charge	$Q_{gd}$		-	7.4	-	
Output charge	$Q_{oss}$		$V_{DS} = 30$ V, $V_{GS} = 0$ V	-	71	
Gate resistance	$R_g$	$f = 1$ MHz	0.2	0.62	1.1	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30$ V, $R_L = 1.5$ $\Omega$ , $I_D \cong 20$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$	-	20	40	ns
Rise time	$t_r$		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	35	70	
Fall time	$t_f$		-	7	14	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30$ V, $R_L = 1.5$ $\Omega$ , $I_D \cong 20$ A, $V_{GEN} = 7.5$ V, $R_g = 1$ $\Omega$	-	24	48	
Rise time	$t_r$		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	$t_f$		-	10	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	-	-	136	A
Pulse diode forward current	$I_{SM}$		-	-	400	
Body diode voltage	$V_{SD}$	$I_S = 5$ A, $V_{GS} = 0$ V	-	0.74	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 20$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C	-	45	90	ns
Body diode reverse recovery charge	$Q_{rr}$		-	45	90	nC
Reverse recovery fall time	$t_a$		-	21	-	ns
Reverse recovery rise time	$t_b$		-	24	-	

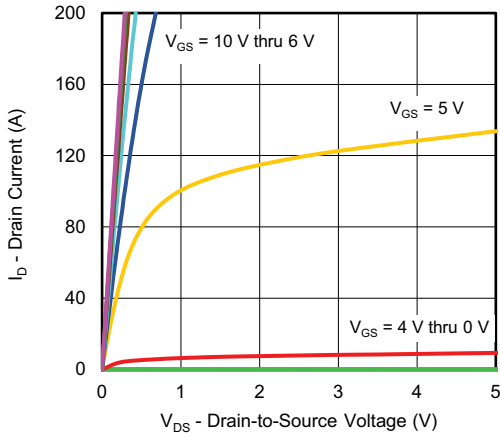
**Notes**

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %  
b. Guaranteed by design, not subject to production testing

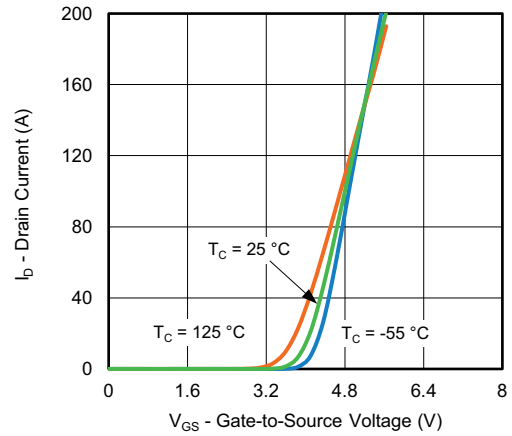
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



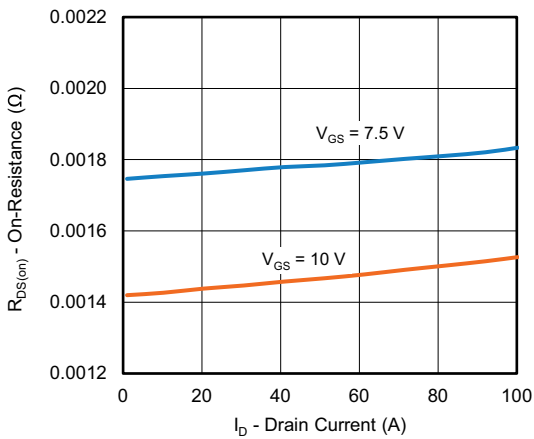
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



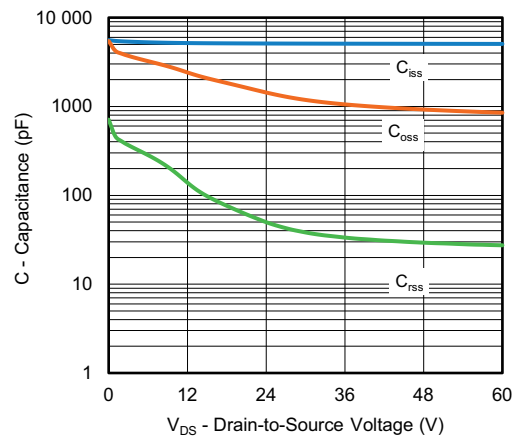
Output Characteristics



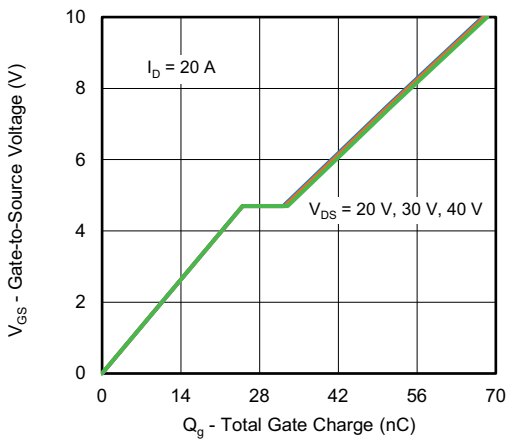
Transfer Characteristics



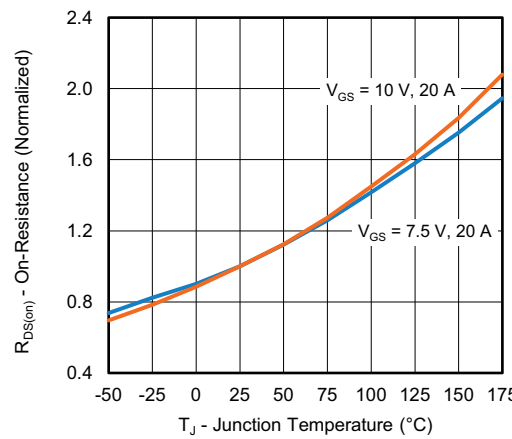
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



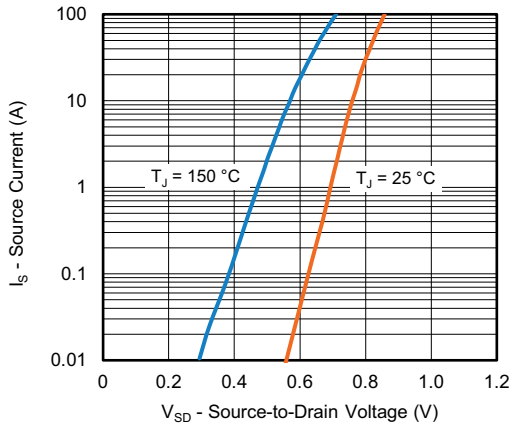
Gate Charge



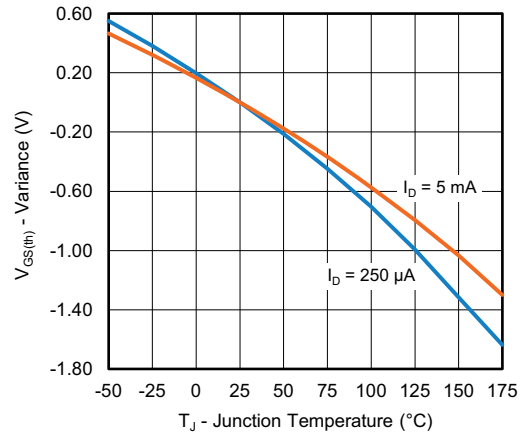
On-Resistance vs. Junction Temperature



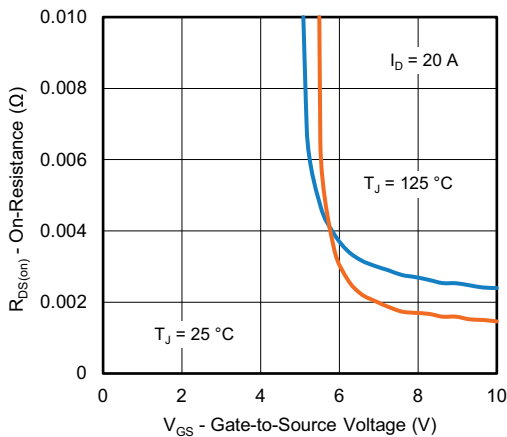
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



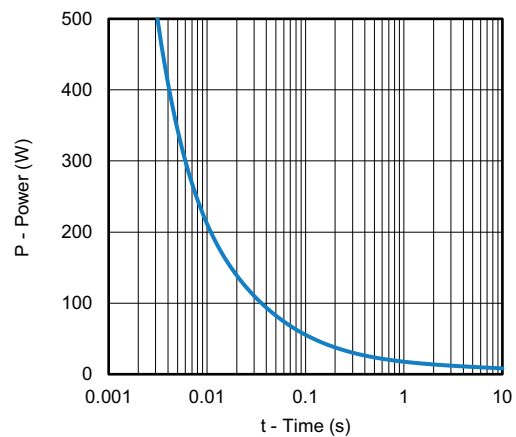
Source-Drain Diode Forward Voltage



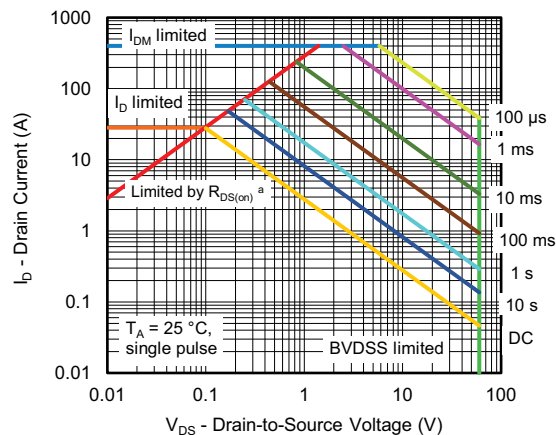
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



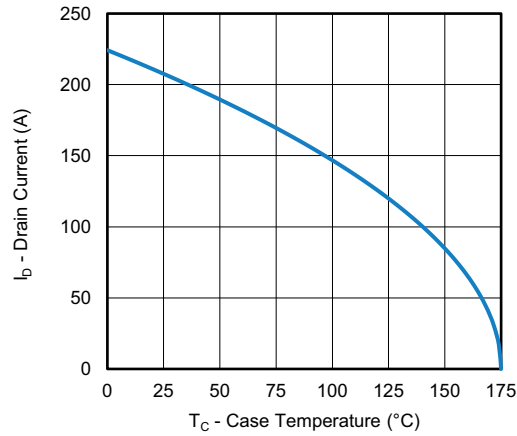
Safe Operating Area, Junction-to-Ambient

Note

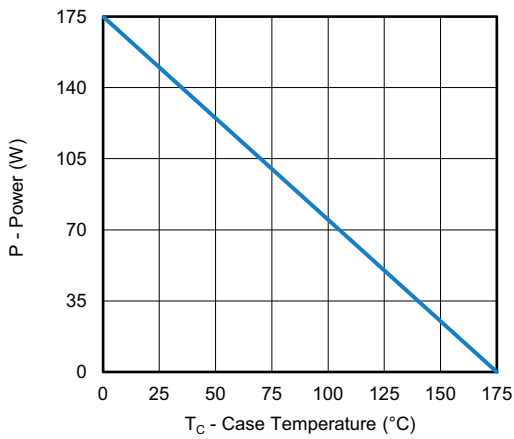
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



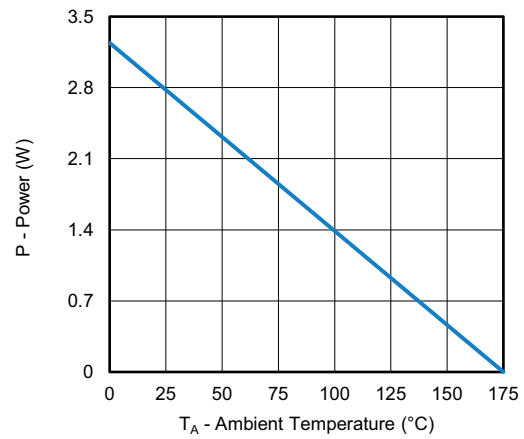
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



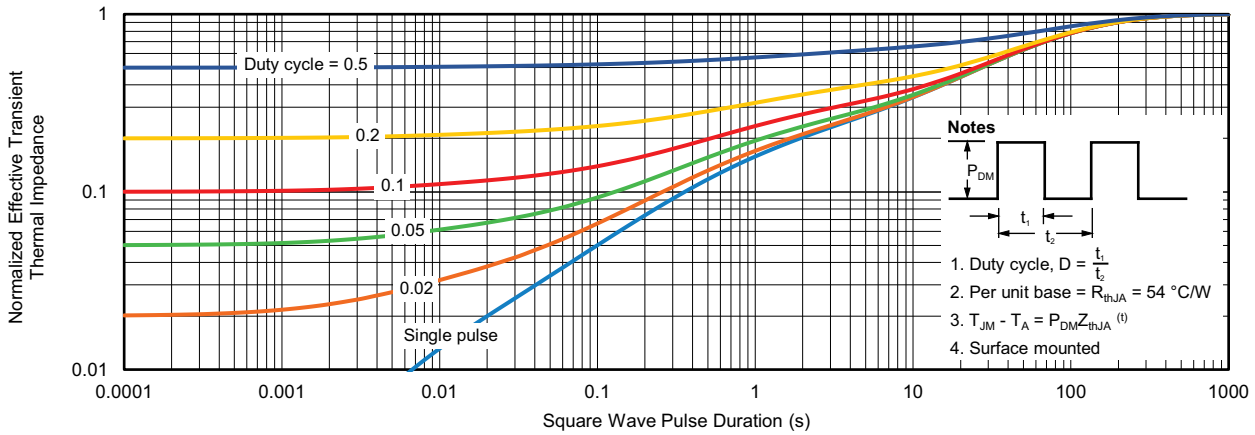
**Power, Junction-to-Ambient**

**Note**

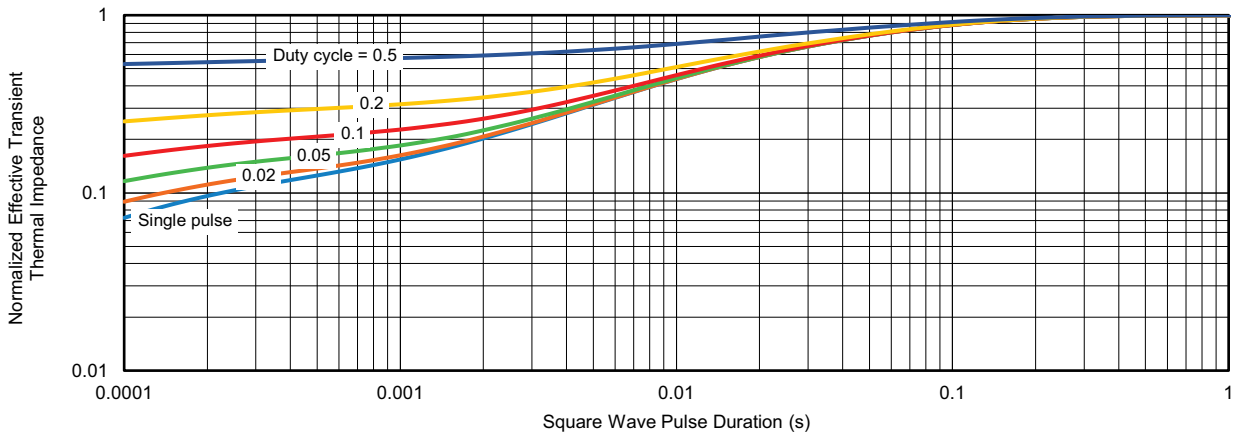
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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