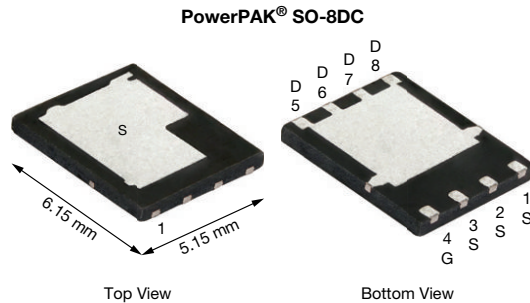


## N-Channel 60 V (D-S) MOSFET



### FEATURES

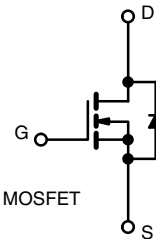
- TrenchFET® Gen IV power MOSFET
- Very low  $R_{DS(on)}$  -  $Q_g$  figure-of-merit (FOM)
- Tuned for the lowest  $R_{DS(on)}$  -  $Q_{oss}$  FOM
- 100 %  $R_g$  and UIS tested
- Top side cooling feature provides additional venue for thermal transfer
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Solar micro inverter
- Motor drive switch
- Battery and load switch
- Industrial



N-Channel MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0017
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0020
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 6$ V	0.0026
$Q_g$ typ. (nC)	52
$I_D$ (A) <sup>a, g</sup>	100
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR626DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	60	V
Gate-source voltage		$V_{GS}$	$\pm 20$	V
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	100 <sup>a</sup>	A
	$T_C = 70$ °C		100 <sup>a</sup>	
	$T_A = 25$ °C		42.8 <sup>b, c</sup>	
	$T_A = 70$ °C		34.2 <sup>b, c</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)		$I_{DM}$	200	A
Continuous source-drain diode current	$T_C = 25$ °C	$I_S$	100 <sup>a</sup>	A
	$T_A = 25$ °C		5.6 <sup>b, c</sup>	
Single pulse avalanche current	L = 0.1 mH	$I_{AS}$	50	mJ
Single pulse avalanche energy		$E_{AS}$	125	
Maximum power dissipation	$T_C = 25$ °C	$P_D$	125	W
	$T_C = 70$ °C		80	
	$T_A = 25$ °C		6.25 <sup>b, c</sup>	
	$T_A = 70$ °C		4 <sup>b, c</sup>	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>			260	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$t \leq 10$ s	$R_{thJA}$	15	20	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	0.8	1	
Maximum junction-to-case (source)	Steady state	$R_{thJC}$	1.1	1.4	

#### Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W
- $T_C = 25$  °C



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	35	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-7.4	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	-	3.4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	100	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$	-	-	15	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	40	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	0.0014	0.0017	$\Omega$
		$V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$	-	0.0016	0.0020	
		$V_{GS} = 6\text{ V}, I_D = 10\text{ A}$	-	0.0020	0.0026	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	-	78	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{ISS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	5130	-	$\mu\text{F}$
Output capacitance	$C_{OSS}$		-	992	-	
Reverse transfer capacitance	$C_{RSS}$		-	94	-	
Total gate charge	$Q_g$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	68	102	$\text{nC}$
		$V_{DS} = 30\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 10\text{ A}$	-	52	78	
Gate-source charge	$Q_{gs}$		-	21	-	
Gate-drain charge	$Q_{gd}$		-	8.2	-	
Output charge	$Q_{OSS}$		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	-	68	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.3	0.91	1.6	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 3\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	16	32	$\text{ns}$
Rise time	$t_r$		-	24	48	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	$t_f$		-	11	22	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 3\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 7.5\text{ V}, R_g = 1\text{ }\Omega$	-	19	38	
Rise time	$t_r$		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	27	54	
Fall time	$t_f$		-	12	24	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	100	A
Pulse diode forward current	$I_{SM}$		-	-	200	
Body diode voltage	$V_{SD}$	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	-	0.72	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	54	108	ns
Body diode reverse recovery charge	$Q_{rr}$		-	64	128	nC
Reverse recovery fall time	$t_a$		-	35	-	ns
Reverse recovery rise time	$t_b$		-	29	-	

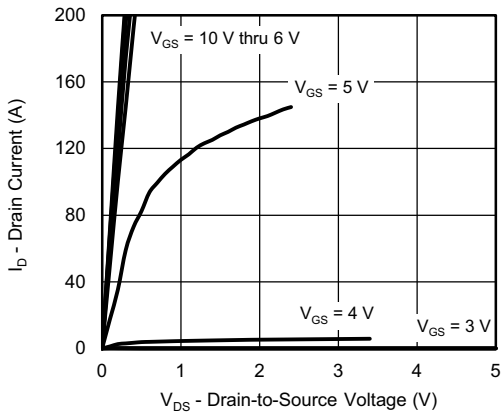
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

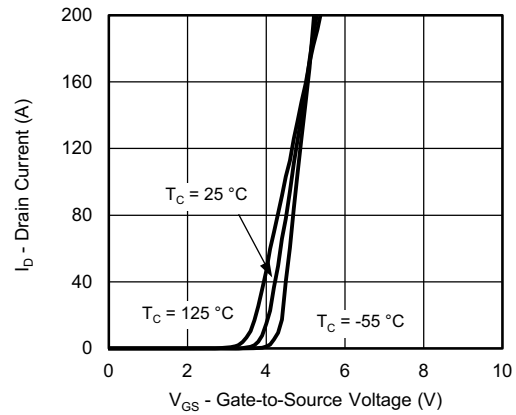
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



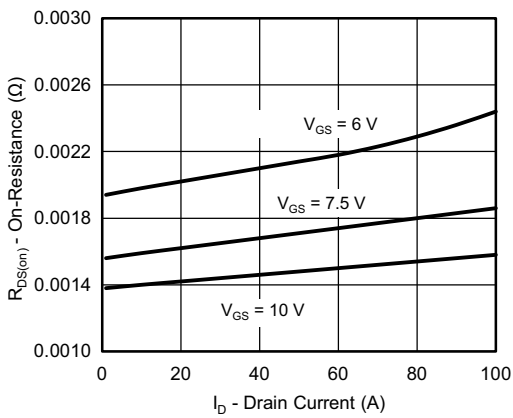
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



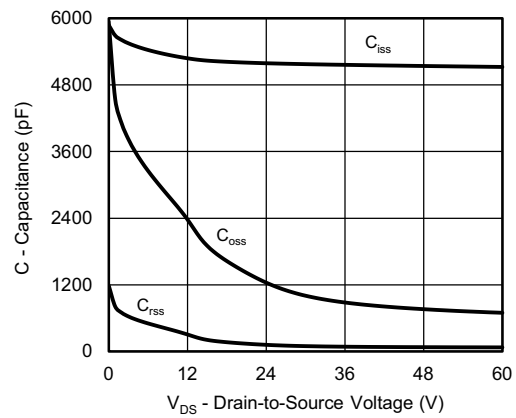
Output Characteristics



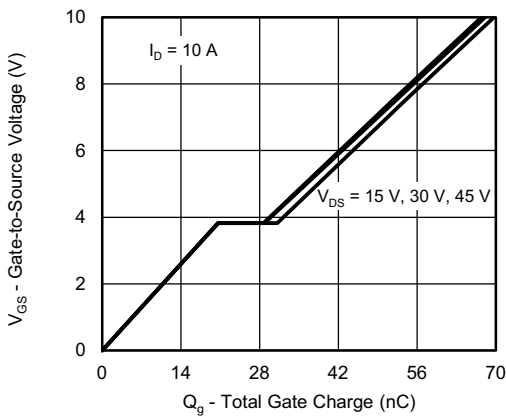
Transfer Characteristics



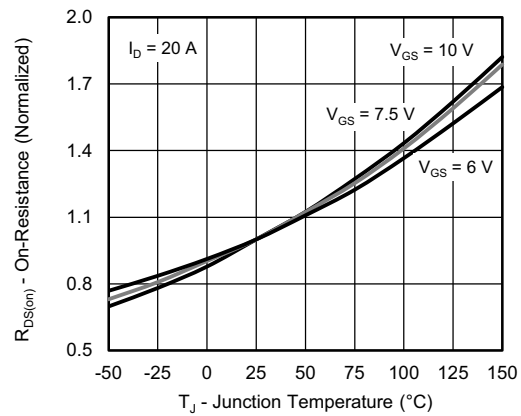
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



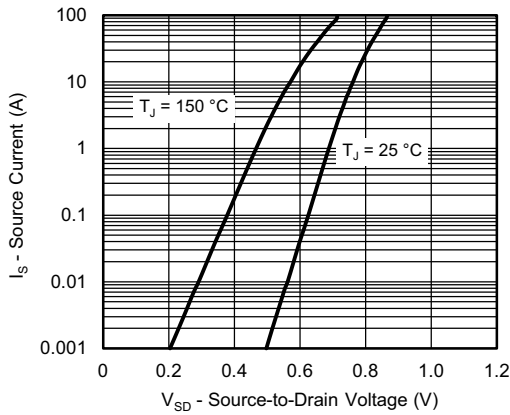
Gate Charge



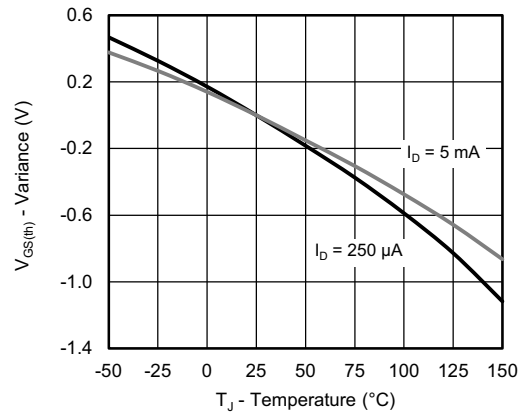
On-Resistance vs. Junction Temperature



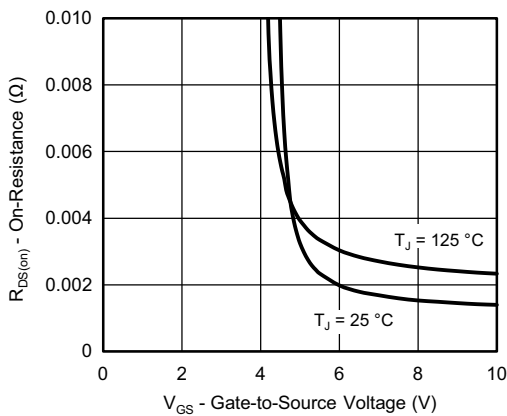
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



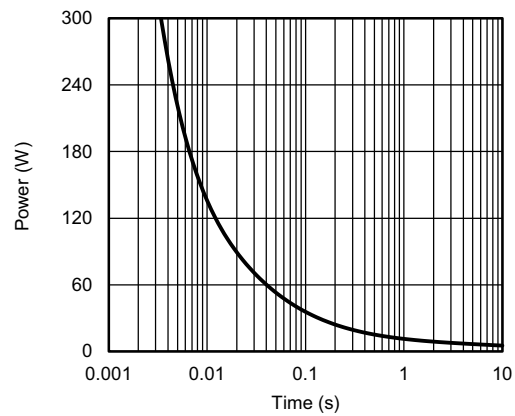
Source-Drain Diode Forward Voltage



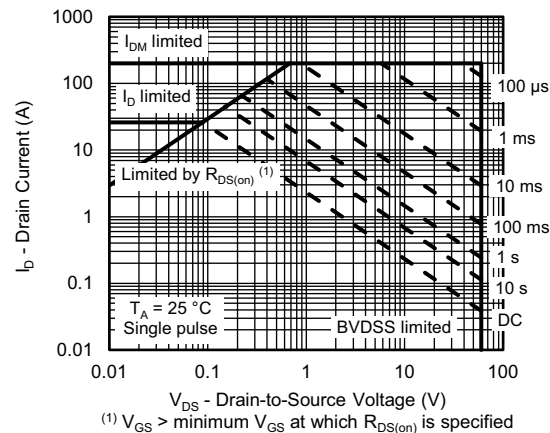
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



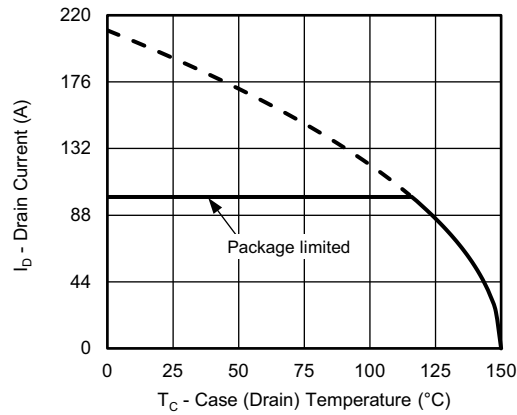
Single Pulse Power, Junction-to-Ambient



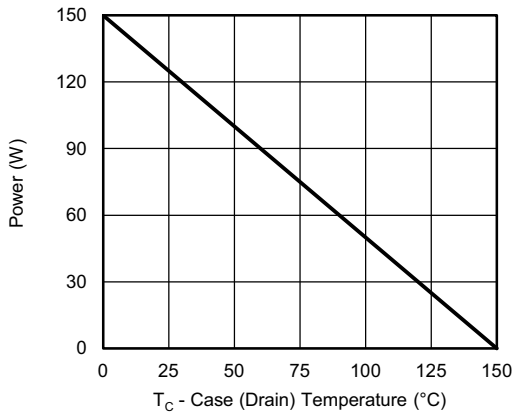
Safe Operating Area, Junction-to-Ambient



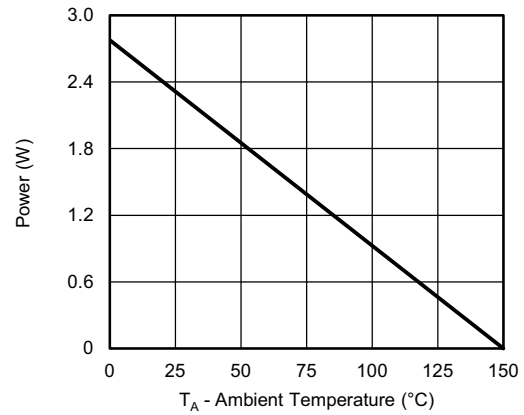
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating <sup>a</sup>



Power, Junction-to-Case



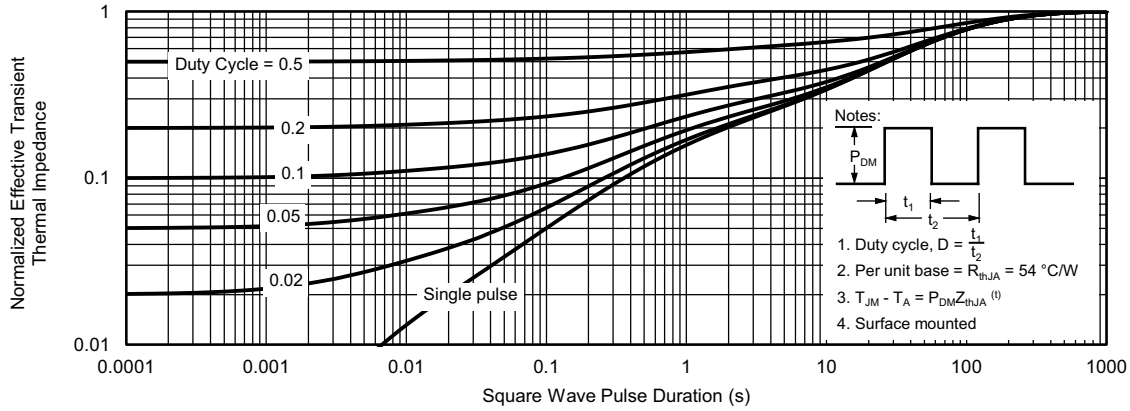
Power, Junction-to-Ambient

Note

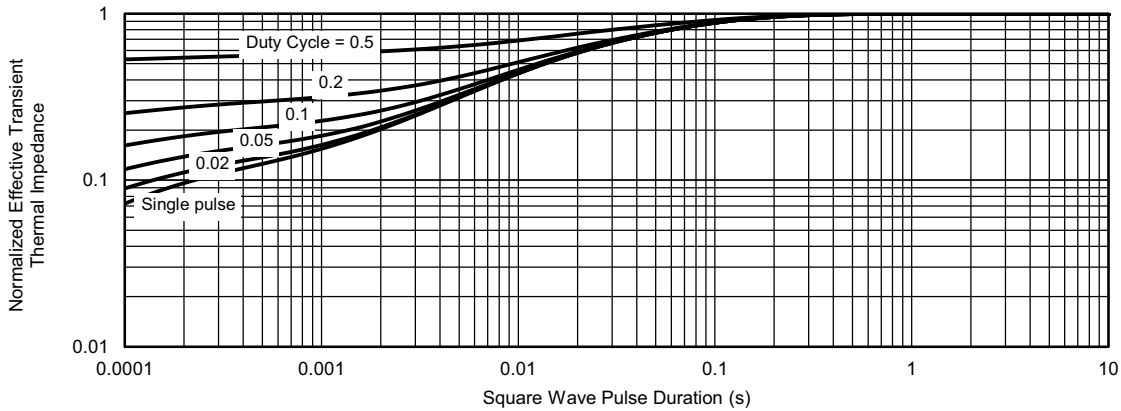
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



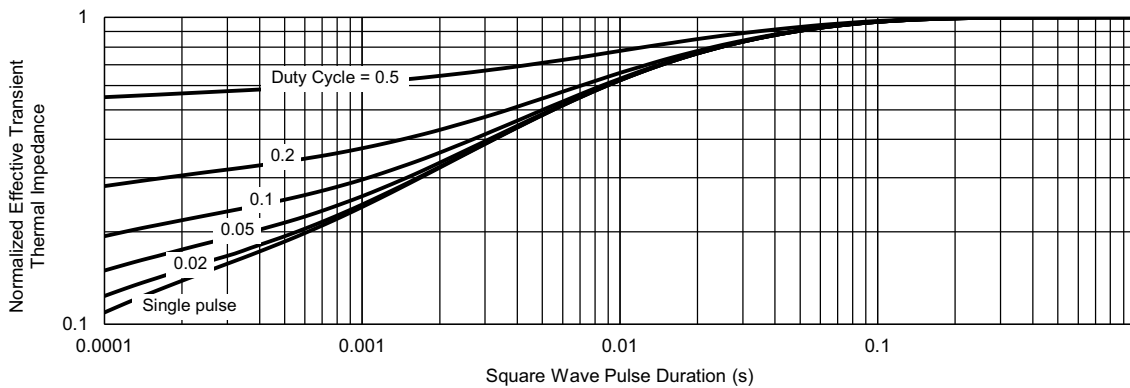
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



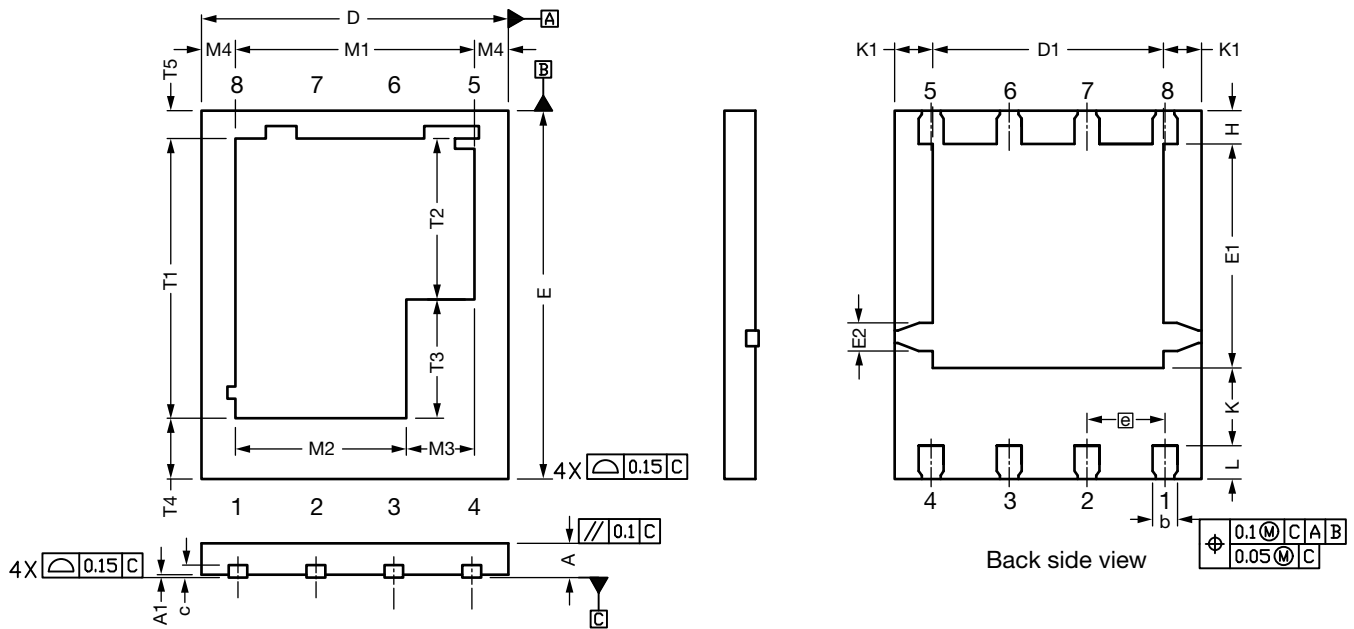
Normalized Thermal Transient Impedance, Junction-to-Case (Drain)



Normalized Thermal Transient Impedance, Junction-to-Case (Source)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?75748](http://www.vishay.com/ppg?75748).

## PowerPAK<sup>®</sup> SO-8 Double Cooling Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.51	0.56	0.61	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.36	0.41	0.46	0.014	0.016	0.018
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.71	3.76	3.81	0.146	0.148	0.150
e	1.27 BSC			0.050 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.60	3.65	3.70	0.142	0.144	0.146
E2	0.46 typ.			0.018 typ.		
H	0.49	0.54	0.59	0.019	0.021	0.023
K	1.22	1.27	1.32	0.048	0.050	0.052
K1	0.64 typ.			0.025 typ.		
L	0.49	0.54	0.59	0.019	0.021	0.023
M1	3.85	3.90	3.95	0.152	0.154	0.156
M2	2.74	2.79	2.84	0.108	0.110	0.112
M3	1.06	1.11	1.16	0.042	0.044	0.046
M4	0.56 typ.			0.022 typ.		
N	8			8		
T1	4.51	4.56	4.61	0.178	0.180	0.182
T2	2.58	2.63	2.68	0.102	0.104	0.106
T3	1.88	1.93	1.98	0.074	0.076	0.078
T4	0.97 typ.			0.038 typ.		
T5	0.48 typ.			0.019 typ.		
ECN: T21-0014-Rev. B, 08-Feb-2021						
DWG: 6048						

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)





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